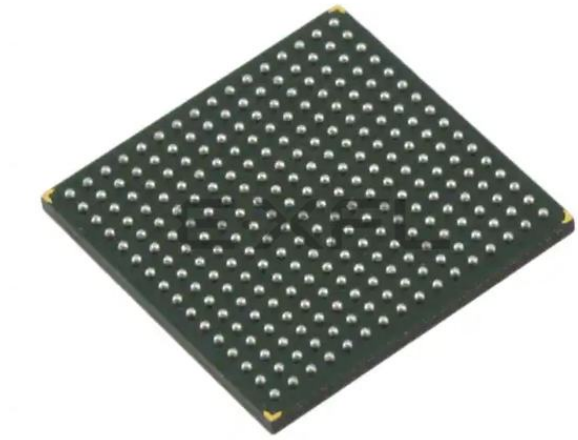

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS32
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	350MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	256-LBGA
Supplier Device Package	256-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32h435-350bci

Pin Description Table

The following table lists the functions of the pins provided on the RC32435. Some of the functions listed may be multiplexed onto the same pin.

The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
Memory and Peripheral Bus		
BDIRN	O	**External Buffer Direction.** Controls the direction of the external data bus buffer for the memory and peripheral bus. If the RC32435 memory and peripheral bus is connected to the A side of a transceiver, such as an IDT74FCT245, then this pin may be directly connected to the direction control (e.g., BDIR) pin of the transceiver.
BOEN	O	**External Buffer Enable.** This signal provides an output enable control for an external buffer on the memory and peripheral data bus.
WEN	O	**Write Enables.** This signal is the memory and peripheral bus write enable signal.
CSN[3:0]	O	**Chip Selects.** These signals are used to select an external device on the memory and peripheral bus.
MADDR[21:0]	O	**Address Bus.** 22-bit memory and peripheral bus address bus. MADDR[25:22] are available as GPIO alternate functions.
MDATA[7:0]	I/O	**Data Bus.** 8-bit memory and peripheral data bus. During a cold reset, these pins function as inputs that are used to load the boot configuration vector.
OEN	O	**Output Enable.** This signal is asserted when data should be driven by an external device on the memory and peripheral bus.
RWN	O	**Read Write.** This signal indicates whether the transaction on the memory and peripheral bus is a read transaction or a write transaction. A high level indicates a read from an external device. A low level indicates a write to an external device.
WAITACKN	I	**Wait or Transfer Acknowledge.** When configured as wait, this signal is asserted during a memory and peripheral bus transaction to extend the bus cycle. When configured as a transfer acknowledge, this signal is asserted during a transaction to signal the completion of the transaction.
DDR Bus		
DDRADDR[13:0]	O	**DDR Address Bus.** 14-bit multiplexed DDR address bus. This bus is used to transfer the addresses to the DDR devices.
DDRBA[1:0]	O	**DDR Bank Address.** These signals are used to transfer the bank address to the DDRs.
DDRCASN	O	**DDR Column Address Strobe.** This signal is asserted during DDR transactions.
DDRCKE	O	**DDR Clock Enable.** The DDR clock enable signal is asserted during normal DDR operation. This signal is negated following a cold reset or during a power down operation.
DDRCKN	O	**DDR Negative DDR clock.** This signal is the negative clock of the differential DDR clock pair.

Table 1 Pin Description (Part 1 of 6)

Signal	Type	Name/Description
EJTAG_TMS	I	**EJTAG Mode**. The value on this signal controls the test mode select of the EJTAG Controller. When using the JTAG boundary scan, this pin should be left disconnected (since there is an internal pull-up) or driven high.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic, JTAG TAP Controller, and the EJTAG Debug TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board 3) clock JTAG_TCK while holding EJTAG_TMS and/or JTAG_TMS high.
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic, JTAG Controller, or the EJTAG Controller. JTAG_TCK is independent of the system and the processor clock with a nominal 50% duty cycle.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic, JTAG Controller, or the EJTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic, JTAG Controller, or the EJTAG Controller.
System		
CLK	I	**Master Clock.** This is the master clock input. The processor frequency is a multiple of this clock frequency. This clock is used as the system clock for all memory and peripheral bus operations.
EXTBCV	I	**Load External Boot Configuration Vector.** When this pin is asserted (i.e., high) the boot configuration vector is loaded from an externally supplied value during a cold reset. When this pin is negated, the boot configuration vector is taken from the NVRAM located on-chip.
EXTCLK	O	**External Clock.** This clock is used for all memory and peripheral bus operations.
COLDRSTN	I	**Cold Reset.** The assertion of this signal initiates a cold reset. This causes the processor state to be initialized, boot configuration to be loaded, and the internal PLL to lock onto the master clock (CLK).
RSTN	I/O	**Reset.** The assertion of this bidirectional signal initiates a warm reset. This signal is asserted by the RC32435 during a warm reset.

Table 1 Pin Description (Part 6 of 6)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes[1]
Serial Peripheral Interface	SCK	I/O	LVTTL	High Drive	pull-up	pull-up on board
	SDI	I/O	LVTTL	High Drive	pull-up	pull-up on board
	SDO	I/O	LVTTL	High Drive	pull-up	pull-up on board
I^2C-Bus Interface	SCL	I/O	LVTTL	Low Drive/STI		pull-up on board[2]
	SDA	I/O	LVTTL	Low Drive/STI		pull-up on board[2]
Ethernet Interfaces	MIICL	I	LVTTL	STI	pull-down	
	MIICRS	I	LVTTL	STI	pull-down	
	MIIRXCLK	I	LVTTL	STI	pull-up	
	MIIRXD[3:0]	I	LVTTL	STI	pull-up	
	MIIRXDV	I	LVTTL	STI	pull-down	
	MIIRXER	I	LVTTL	STI	pull-down	
	MIITXCLK	I	LVTTL	STI	pull-up	
	MIITXD[3:0]	O	LVTTL	Low Drive		
	MIITXENP	O	LVTTL	Low Drive		
	MIITXER	O	LVTTL	Low Drive		
	MIIMDC	O	LVTTL	Low Drive		
	MIIMDIO	I/O	LVTTL	Low Drive	pull-up	
EJTAG / JTAG	JTAG_TMS	I	LVTTL	STI	pull-up	
	EJTAG_TMS	I	LVTTL	STI	pull-up	
	JTAG_TRST_N	I	LVTTL	STI	pull-up	
	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDO	O	LVTTL	Low Drive		
	JTAG_TDI	I	LVTTL	STI	pull-up	
System	CLK	I	LVTTL	STI		
	EXTBCV	I	LVTTL	STI	pull-down	
	EXTCLK	O	LVTTL	High Drive		
	COLDRSTN	I	LVTTL	STI		
	RSTN	I/O	LVTTL	Low Drive / STI	pull-up	pull-up on board

Table 2 Pin Characteristics (Part 2 of 2)

1. External pull-up required in most system applications. Some applications may require additional pull-ups not identified in this table.

2. Use a 2.2K pull-up resistor for I2C pins.

System Clock Parameters

(Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 15 and 16.)

Parameter	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Units	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max		
PCLK[1]	Frequency	none	200	266	200	300	200	350	200	400	MHz	See Figure 3.
	Tper		3.8	5.0	3.3	5.0	2.85	5.0	2.5	5.0	ns	
ICLK[2,3,4]	Frequency	none	100	133	100	150	100	175	100	200	MHz	
	Tper		7.5	10.0	6.7	10.0	5.7	10.0	5.0	10.0	ns	
CLK[5]	Frequency	none	25	125	25	125	25	125	25	125	MHz	
	Tper_5a		8.0	40.0	8.0	40.0	8.0	40.0	8.0	40.0	ns	
	Thigh_5a, Tlow_5a		40	60	40	60	40	60	40	60	% of Tper_5a	
	Trise_5a, Tfall_5a		—	3.0	—	3.0	—	3.0	—	3.0	ns	
	Tjitter_5a		—	0.1	—	0.1	—	0.1	—	0.1	ns	

Table 5 Clock Parameters

1. The CPU pipeline clock (PCLK) speed is selected during cold reset by the boot configuration vector (see Table 3). Refer to Chapter 3, Clocking and Initialization, in the RC32435 User Reference Manual for the allowable frequency ranges of CLK and PCLK.
2. ICLK is the internal IPBus clock. It is always equal to PCLK divided by 2. This clock cannot be sampled externally.
3. The ethernet clock (MIIxRXCLK and MIIxTXCLK) frequency must be equal to or less than 1/2 ICLK (MIIxRXCLK and MIIxTXCLK <= 1/2(ICLK)).
4. PCICLK must be equal to or less than two times ICLK (PCICLK <= 2(ICLK)) with a maximum PCICLK of 66 MHz.
5. The input clock (CLK) is input from the external oscillator to the internal PLL.

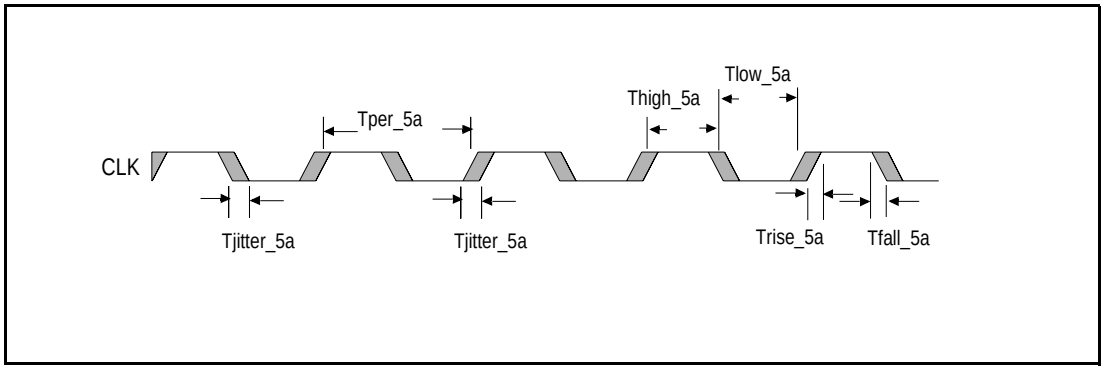
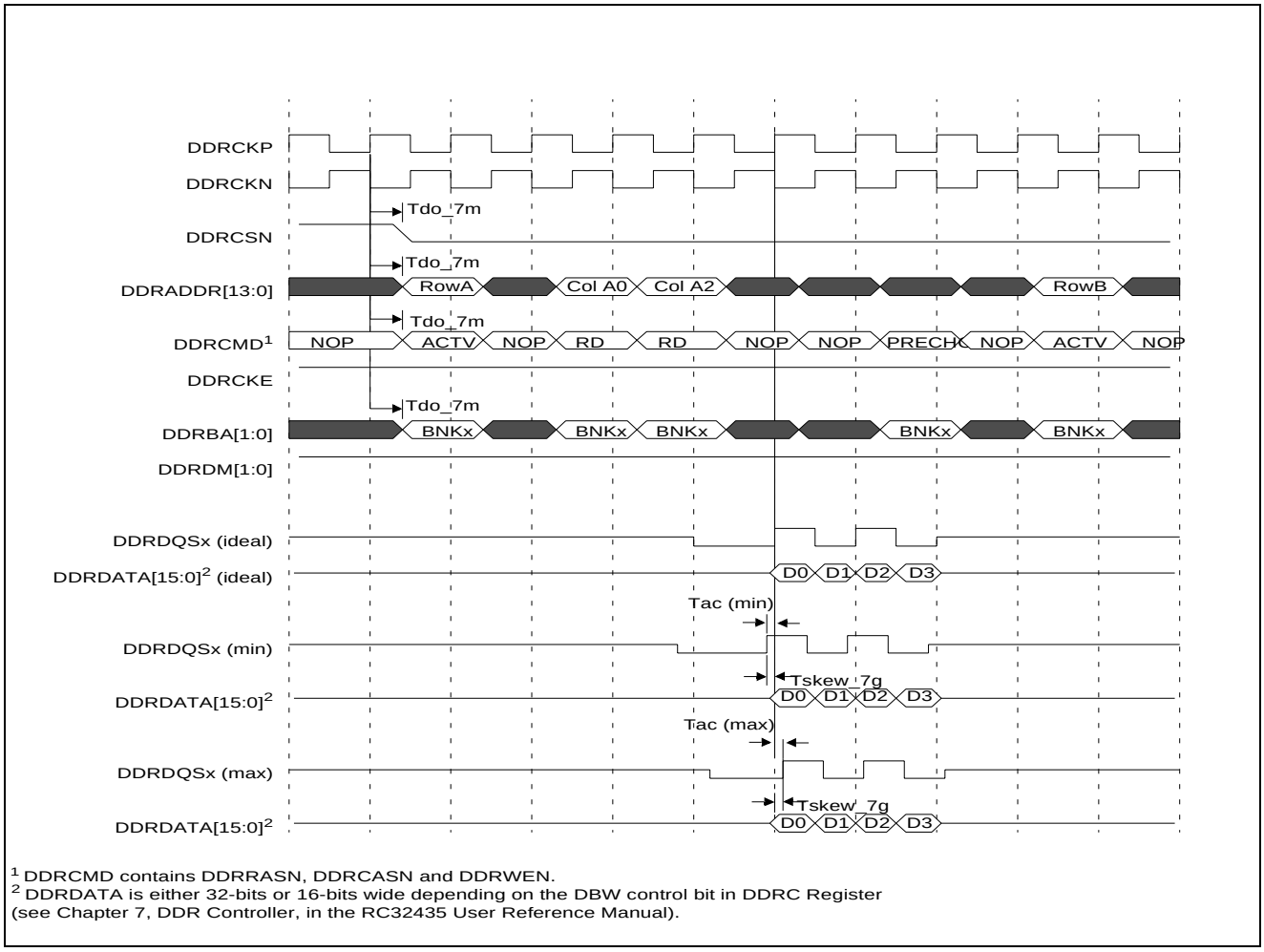


Figure 3 Clock Parameters Waveform



[1] DDRCMD contains DDRRASN, DDRCASN and DDRWEN.
[2] DDRDATA is either 32-bits or 16-bits wide depending on the DBW control bit in DDRC Register (see Chapter 7, DDR Controller, in the RC32435 User Reference Manual).

Figure 6 DDR SDRAM AC Timing Waveform - SDRAM Read Access

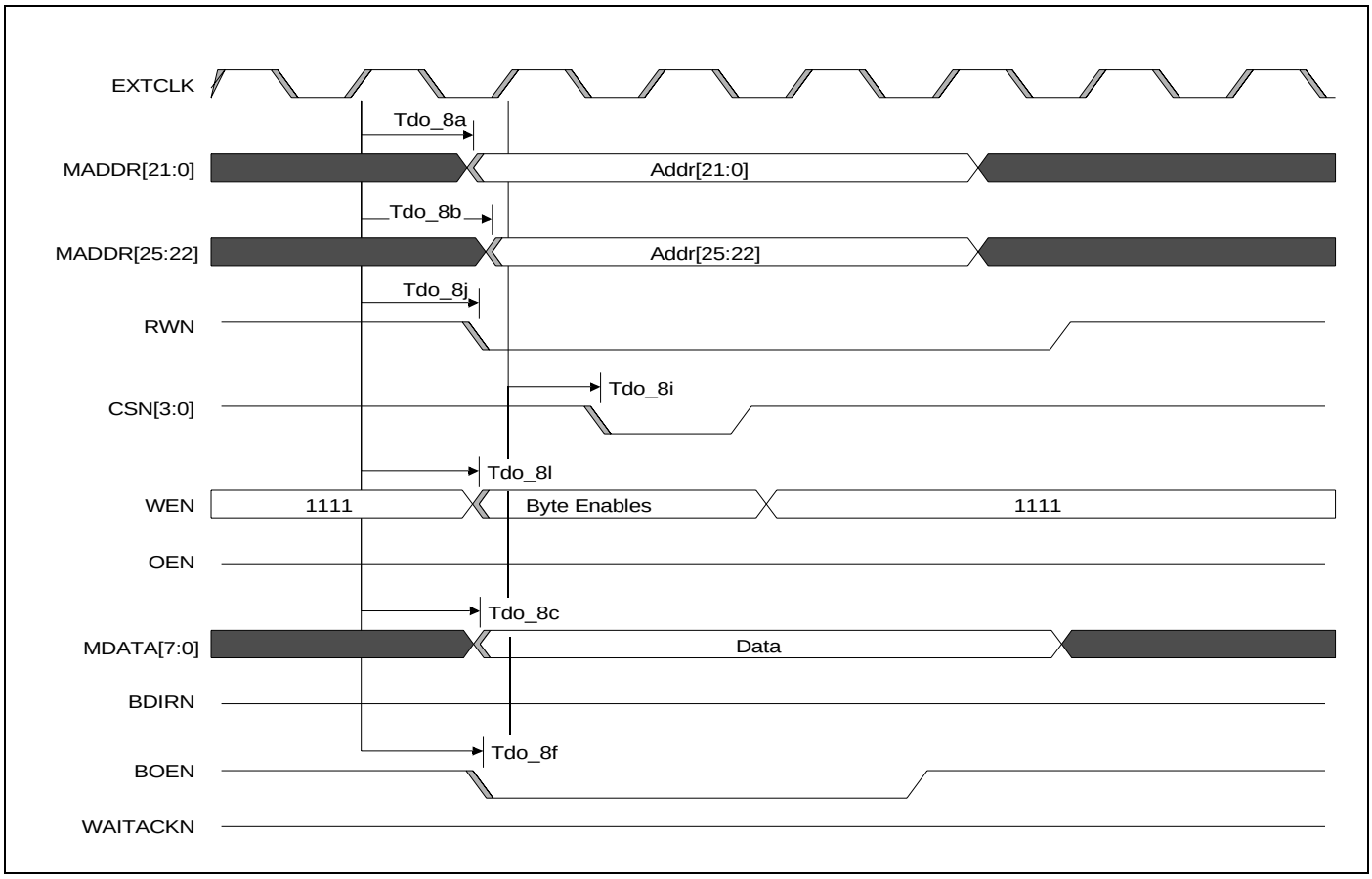


Figure 9 Memory and Peripheral Bus AC Timing Waveform — Write Access

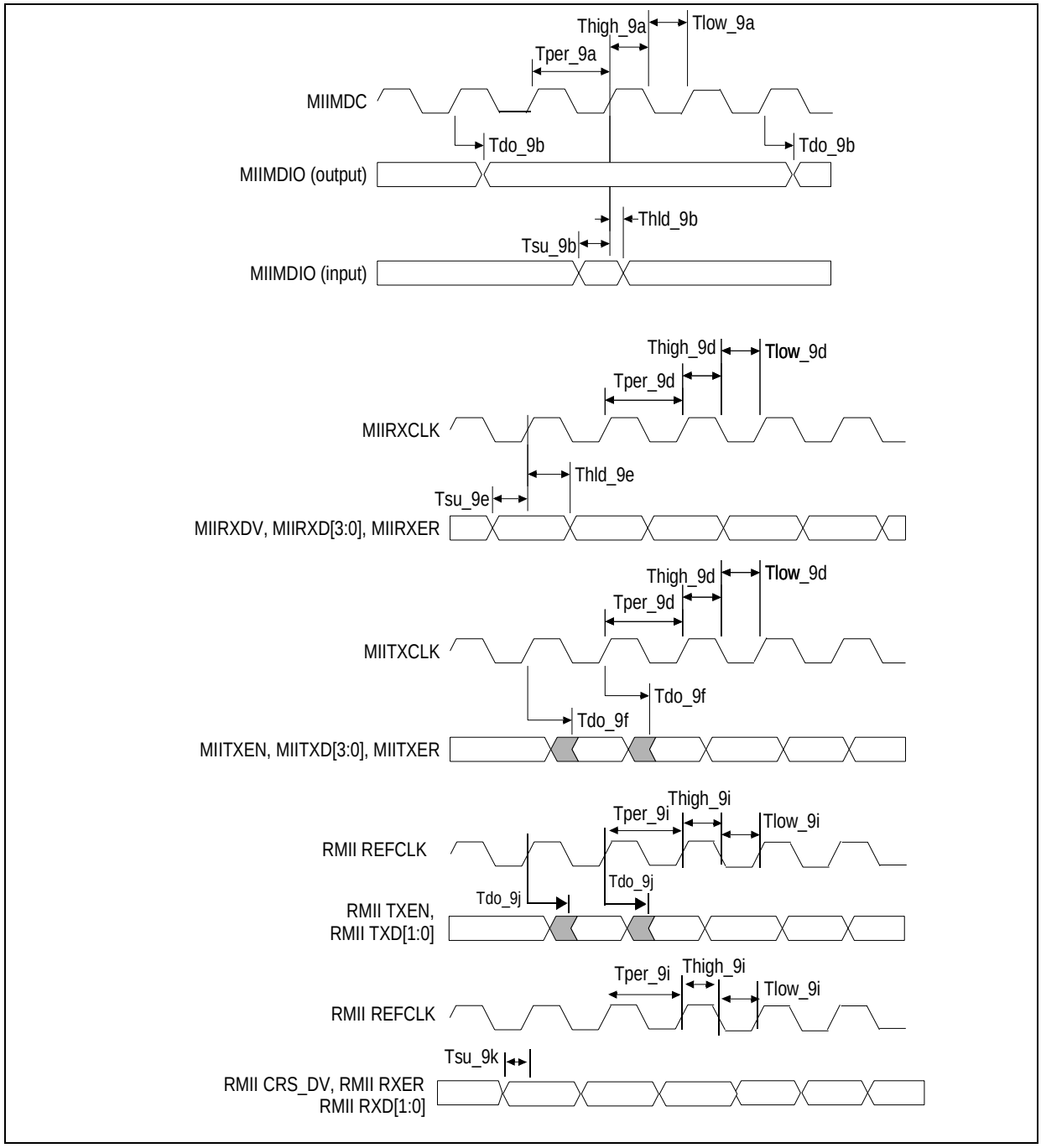


Figure 10 Ethernet AC Timing Waveform

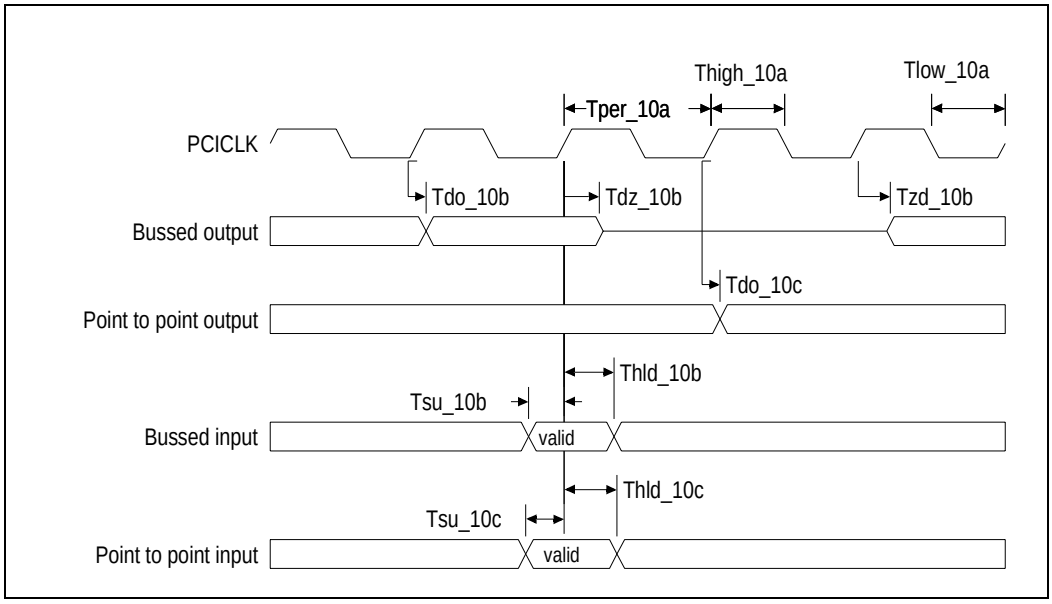
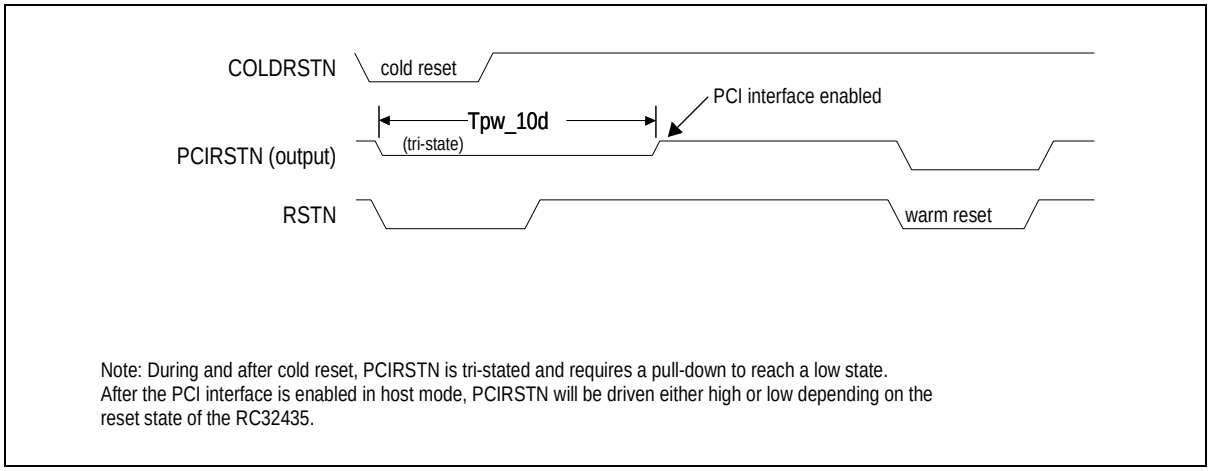


Figure 11 PCI AC Timing Waveform



Note: During and after cold reset, PCIRSTN is tri-stated and requires a pull-down to reach a low state. After the PCI interface is enabled in host mode, PCIRSTN will be driven either high or low depending on the reset state of the RC32435.

Figure 12 PCI AC Timing Waveform — PCI Reset in Host Mode

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
SPI[1]													
SCK	Tper_15a	None	100	166667	100	166667	100	166667	100	166667	ns	SPI	See Figures 16, 17, and 18.
	Thigh_15a, Tlow_15a		40	83353	40	83353	40	83353	40	83353	ns	SPI	
SDI	Tsu_15b	SCK rising or falling	60	—	60	—	60	—	60	—	ns	SPI	See Figures 16, 17, and 18.
	Thld_15b		60	—	60	—	60	—	60	—	ns	SPI	
SDO	Tdo_15c	SCK rising or falling	0	60	0	60	0	60	0	60	ns	SPI	
SCK, SDI, SDO	Tpw_15e	None	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	ns	Bit I/O	

Table 13 SPI AC Timing Characteristics

1. In SPI mode, the SCK period and sampling edge are programmable. In PCI mode, the SCK period is fixed and the sampling edge is rising.

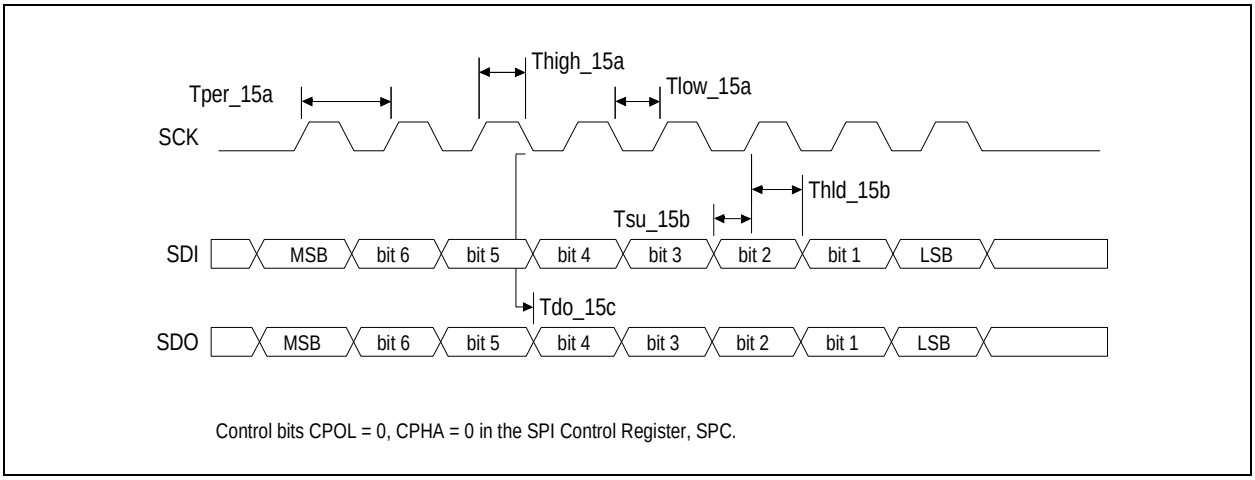


Figure 16 SPI AC Timing Waveform — Clock Polarity 0, Clock Phase 0

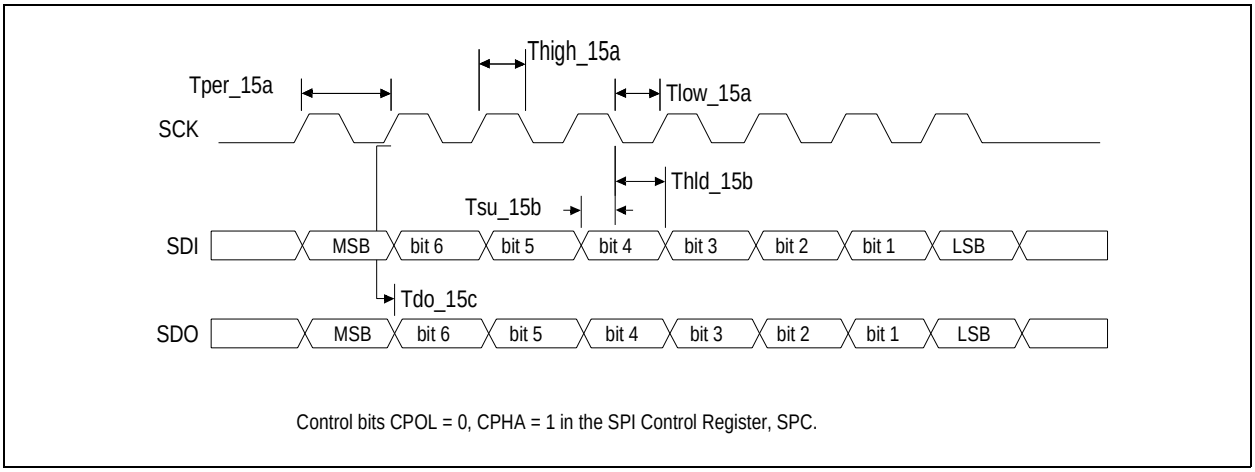


Figure 17 SPI AC Timing Waveform — Clock Polarity 0, Clock Phase 1

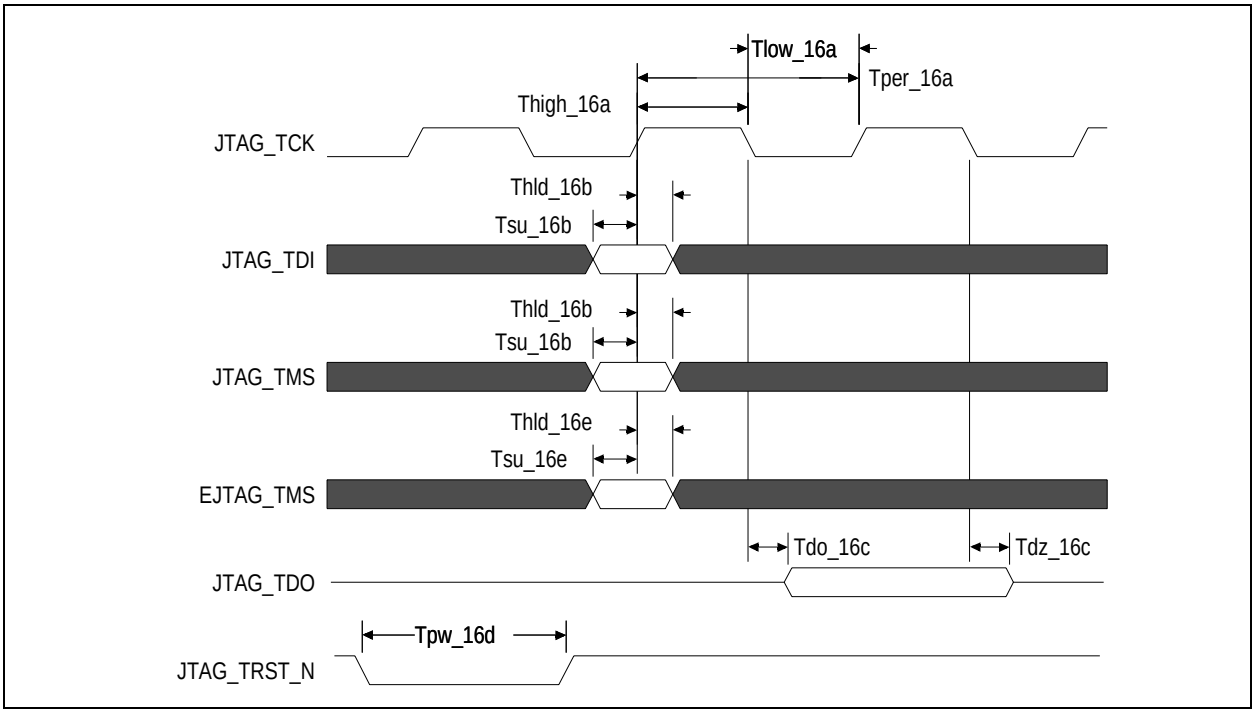


Figure 19 JTAG AC Timing Waveform

The IEEE 1149.1 specification requires that the JTAG and EJTAG TAP controllers be reset at power-up whether or not the interfaces are used for a boundary scan or a probe. Reset can occur through a pull-down resistor on JTAG_TRST_N if the probe is not connected. However, on-chip pull-up resistors are implemented on the RC32435 due to an IEEE 1149.1 requirement. Having on-chip pull-up and external pull-down resistors for the JTAG_TRST_N signal requires special care in the design to ensure that a valid logical level is provided to JTAG_TRST_N, such as using a small external pull-down resistor to ensure this level overrides the on-chip pull-up. An alternative is to use an active power-up reset circuit for JTAG_TRST_N, which drives JTAG_TRST_N low only at power-up and then holds JTAG_TRST_N high afterwards with a pull-up resistor.

Figure 20 shows the electrical connection of the EJTAG probe target system connector.

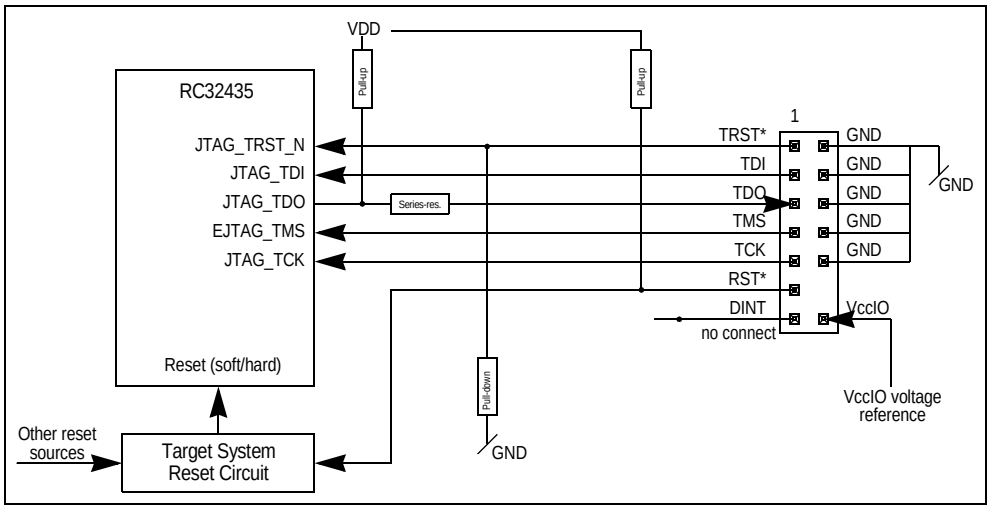


Figure 20 Target System Electrical EJTAG Connection

Power-on Sequence

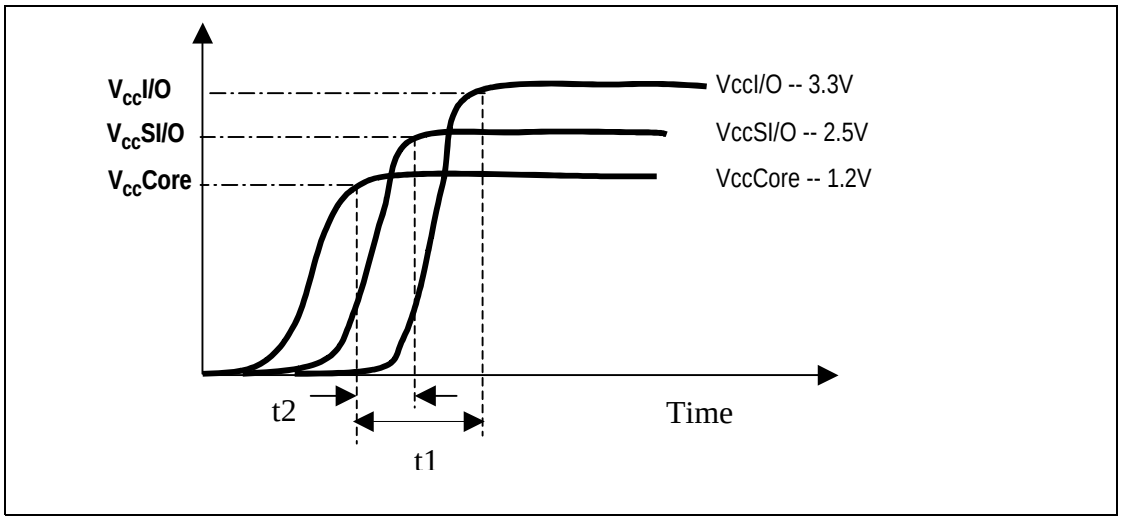
Three power-on sequences are given below. Sequence #1 is recommended because it will prevent I/O conflicts and will also allow the input signals to propagate when the I/O powers are brought up.

Note: The ESD diodes may be damaged if one of the voltages is applied and one of the other voltages is at a ground level.

A. Recommended Sequence

t2 > 0 whenever possible (V_{cc}Core)

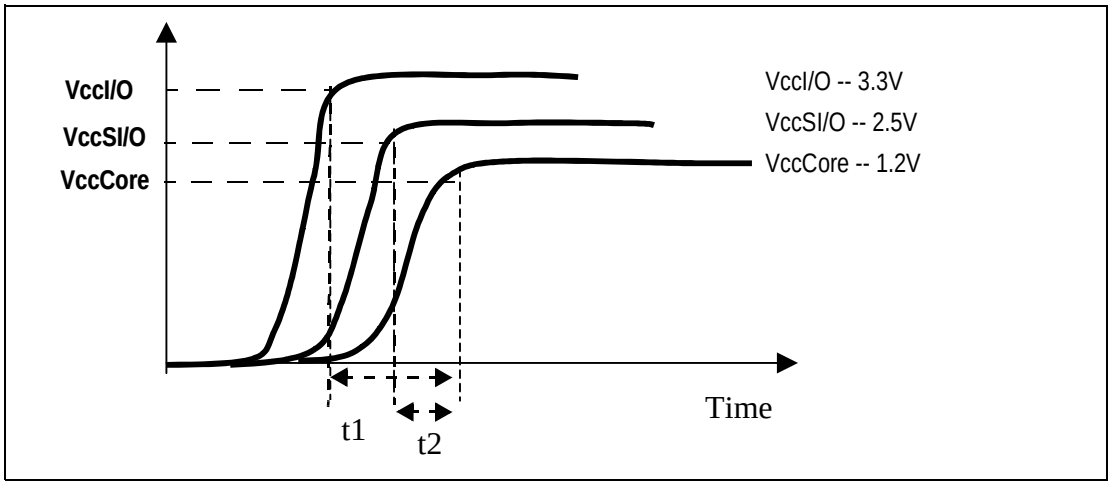
t1 - t2 can be 0 (V_{cc}SI/O followed by V_{cc}I/O)



B. Reverse Voltage Sequence

If sequence A is not feasible, then Sequence B can be used:

t1 <50ms and t2 <50ms to prevent damage.



C. Simultaneous Power-up

VccI/O, VccSI/O, and VccCore can be powered up simultaneously.

Power Consumption

Parameter		266MHz		300MHz		350MHz		400MHz		Unit	Conditions
		Typ.	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**		
I_{CC} I/O		215	270	220	275	225	280	230	285	mA	C_L = 35 pF $T_{ambient}$ = 25°C Max. values use the maximum voltages listed in Table 15. Typical values use the typical voltages listed in that table. Note: For additional information, see Power Considerations for IDT Processors on the IDT web site www.idt.com.
I_{CC} SI/O (DDR)		70	85	75	90	85	100	95	110	mA	
I_{CC} Core, I_{CC} PLL	Normal mode	325	510	350	550	400	610	450	670	mA	
	Standby mode[1]	220	—	240	—	260	—	280	—	mA	
Power Dissipation	Normal mode	1.27	1.82	1.36	1.90	1.45	2.02	1.54	2.15	W	
	Standby mode[1]	0.73	—	0.78	—	0.84	—	0.90	—	W	

Table 17 RC32435 Power Consumption

1. The RC32435 enter Standby mode by executing WAIT instructions. Minimal I/O switching is assumed. On-chip logic outside the CPU core continues to function.

Power Curve

The following graph contains a power curve that shows power consumption at various core frequencies.

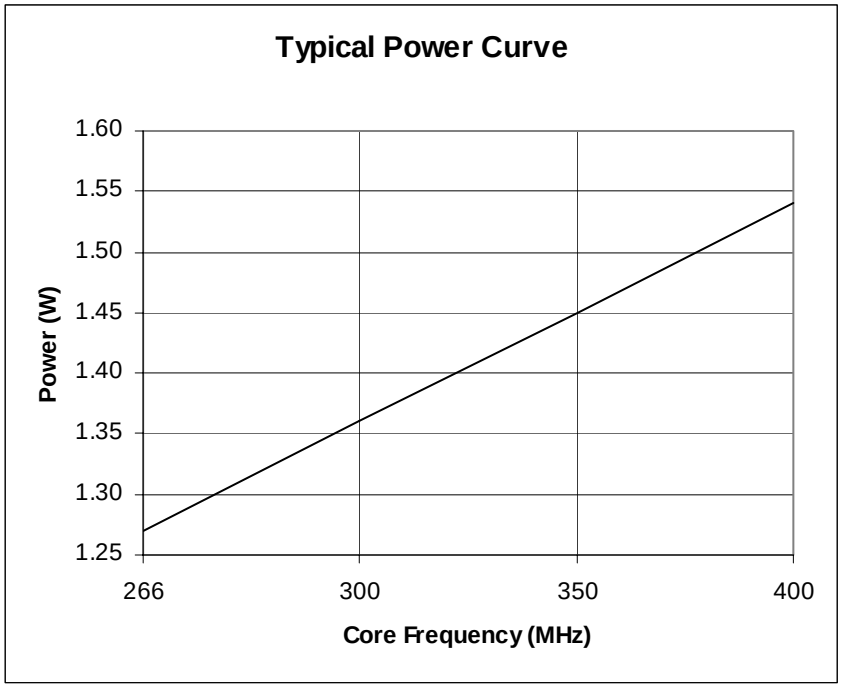


Figure 22 RC32435 Typical Power Usage

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 15.

Note: See Table 2, Pin Characteristics, for a complete I/O listing.

I/O Type	Para-meter	Min.	Typical	Max.	Unit	Conditions
LOW Drive Output	I_{OL}	—	14.0	—	mA	V_{OL} = 0.4V
	I_{OH}	—	-12.0	—	mA	V_{OH} = 1.5V
HIGH Drive Output	I_{OL}	—	41.0	—	mA	V_{OL} = 0.4V
	I_{OH}	—	-42.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}	-0.3	—	0.8	V	—
	V_{IH}	2.0	—	V_{cc}I/O + 0.5	V	—
SSTL_2 (for DDR SDRAM)	I_{OL}	7.6	—	—	mA	V_{OL} = 0.5V
	I_{OH}	-7.6	—	—	mA	V_{OH} = 1.76V
	V_{IL}	-0.3	—	0.5(V_{cc}SI/O) - 0.18	V	
	V_{IH}	0.5(V_{cc}SI/O) + 0.18	—	V_{cc}SI/O + 0.3	V	
PCI	I_{OH}(AC) Switching	-12(V_{cc}I/O)	—	—	mA	0 < V_{OUT} < 0.3(V_{cc}I/O)
		-17.1(V_{cc}I/O - V_{OUT})	—	—	mA	0.3(V_{cc}I/O) < V_{OUT} < 0.9(V_{cc}I/O)
		—	—	-32(V_{cc}I/O)	—	0.7(V_{cc}I/O)
		16(V_{cc}I/O)	—	See Note 1	mA	0.7(V_{cc}I/O) < V_{OUT} < V_{cc}I/O
	I_{OL}(AC) Switching	+16(V_{cc}I/O)	—	—	mA	V_{cc}I/O > V_{OUT} > 0.6(V_{cc}I/O)
		+26.7(V_{OUT})	—	—	mA	0.6(V_{cc}I/O) > V_{OUT} > 0.1(V_{cc}I/O)
		—	—	+38(V_{cc}I/O)	mA	V_{OUT} = 0.18(V_{cc}I/O)
		—	—	See Note 2	mA	0.18(V_{cc}I/O) > V_{OUT} > 0
	V_{IL}	-0.3	—	0.3(V_{cc}I/O)	V	
	V_{IH}	0.5(V_{cc}I/O)	—	5.5	V	
Capacitance	C_{IN}	—	—	10.5	pF	—
Leakage	Inputs	—	—	± 10	µA	Vcc (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/ downs	—	—	± 10	µA	Vcc (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/ downs	—	—	± 80	µA	Vcc (max)

Table 18 DC Electrical Characteristics

Note 1: $I_{OH}(AC)\ max = (98/V_{CC}I/O) * (V_{OUT} - V_{CC}I/O) * (V_{OUT} + 0.4V_{CC}I/O)$

Note 2: $I_{OL}(AC)\ max = (256/V_{CC}I/O) * V_{OUT} * (V_{CC}I/O - V_{OUT})$

Absolute Maximum Ratings

Symbol	Parameter	Min[1]	Max[1]	Unit
V_{CC}I/O	I/O supply except for SSTL_2[2]	-0.6	4.0	V
V_{CC}SI/O (DDR)	I/O supply for SSTL_2[2]	-0.6	4.0	V
V_{CC}Core	Core Supply Voltage	-0.6	2.0	V
V_{CC}PLL	PLL supply (digital)	-0.6	2.0	V
V_{CC}APLL	PLL supply (analog)	-0.6	4.0	V
VinI/O	I/O Input Voltage except for SSTL_2	-0.6	V_{cc}I/O+ 0.5	V
VinSI/O	I/O Input Voltage for SSTL_2	-0.6	V_{cc}SI/O+ 0.5	V
T_a Industrial	Ambient Operating Temperature	-40	+85	°C
T_a Commercial	Ambient Operating Temperature	0	+70	°C
T_s	Storage Temperature	-40	+125	°C

Table 19 Absolute Maximum Ratings

1. Functional and tested operating conditions are given in Table 15. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. SSTL_2 I/Os are used to connect to DDR SDRAM.

RC32435 Alternate Signal Functions

Pin	GPIO	Alternate	Pin	GPIO	Alternate
A7	GPIO[7]	MADDR[25]	J3	GPIO[2]	U0RTSN
A8	GPIO[4]	MADDR[22]	L3	GPIO[8]	CPU
B8	GPIO[5]	MADDR[23]	M1	GPIO[12]	PCIGNTN[5]
C7	GPIO[6]	MADDR[24]	M3	GPIO[11]	PCIREQN[5]
H3	GPIO[0]	U0SOUT	M4	GPIO[9]	PCIREQN[4]
H4	GPIO[1]	U0SINP	P3	GPIO[10]	PCIGNTN[4]
J1	GPIO[3]	U0CTSN	T2	GPIO[13]	PCIMUINTN

Table 21 RC32435 Alternate Signal Functions

RC32435 Power Pins

V_{cc} I/O	V_{cc} DDR	V_{cc} Core	V_{cc} PLL	V_{cc} APLL
E5	E11	E8	B11	C12
E6	E12	E9		
E7	F12	F9		
E10	G12	H5		
F5	K12	H6		
G5	L12	H12		
K5	M11	J5		
K6	M12	J11		
L5		J12		
M5		L8		
M6		M8		
M7		M9		
M10				

Table 22 RC32435 Power Pins

Signal Name	I/O Type	Location	Signal Category
DDRADDR[0]	O	P14	DDR Bus
DDRADDR[1]	O	R16	
DDRADDR[2]	O	P15	
DDRADDR[3]	O	N15	
DDRADDR[4]	O	N14	
DDRADDR[5]	O	N13	
DDRADDR[6]	O	M15	
DDRADDR[7]	O	M16	
DDRADDR[8]	O	L16	
DDRADDR[9]	O	L13	
DDRADDR[10]	O	K15	
DDRADDR[11]	O	K14	
DDRADDR[12]	O	K16	
DDRADDR[13]	O	E15	
DDRBA[0]	O	N16	
DDRBA[1]	O	M14	
DDRCASN	O	L15	
DDRCKE	O	K13	
DDRCKN	O	J13	
DDRCKP	O	J15	
DDRCSN	O	P16	
DDRDATA[0]	I/O	C16	
DDRDATA[1]	I/O	D16	
DDRDATA[2]	I/O	D14	
DDRDATA[3]	I/O	D15	
DDRDATA[4]	I/O	E16	
DDRDATA[5]	I/O	E14	
DDRDATA[6]	I/O	E13	
DDRDATA[7]	I/O	F16	
DDRDATA[8]	I/O	F14	
DDRDATA[9]	I/O	F13	
DDRDATA[10]	I/O	G15	
DDRDATA[11]	I/O	G16	
DDRDATA[12]	I/O	H15	
DDRDATA[13]	I/O	H16	
DDRDATA[14]	I/O	H14	

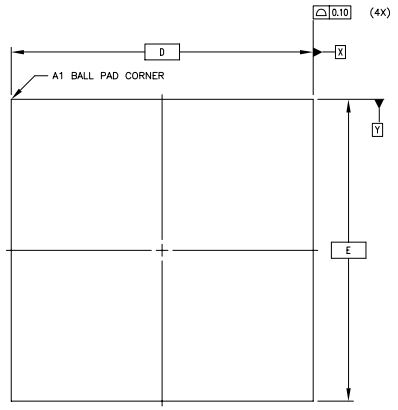
Table 24 RC32435 Alphabetical Signal List (Part 2 of 7)

Signal Name	I/O Type	Location	Signal Category
PCIAD[17]	I/O	R5	PCI Bus Interface
PCIAD[18]	I/O	N4	
PCIAD[19]	I/O	T4	
PCIAD[20]	I/O	P4	
PCIAD[21]	I/O	R4	
PCIAD[22]	I/O	T3	
PCIAD[23]	I/O	R3	
PCIAD[24]	I/O	T1	
PCIAD[25]	I/O	R1	
PCIAD[26]	I/O	P2	
PCIAD[27]	I/O	P1	
PCIAD[28]	I/O	N2	
PCIAD[29]	I/O	N1	
PCIAD[30]	I/O	N3	
PCIAD[31]	I/O	M2	
PCIBEN[0]	I/O	N12	
PCIBEN[1]	I/O	R9	
PCIBEN[2]	I/O	R7	
PCIBEN[3]	I/O	R2	
PCICLK	I	T6	
PCIDEVSELN	I/O	T8	
PCIFRAMEN	I/O	P7	
PCIGNTN[0]	I/O	T7	
PCIGNTN[1]	I/O	T15	
PCIGNTN[2]	I/O	R15	
PCIGNTN[3]	I/O	T16	
PCIIRDYN	I/O	N7	
PCILOCKN	I/O	N8	
PCIPAR	I/O	T9	
PCIPERRN	I/O	N9	
PCIREQN[0]	I/O	P6	
PCIREQN[1]	I/O	N5	
PCIREQN[2]	I/O	N6	
PCIREQN[3]	I/O	P5	
PCIRSTN	I/O	R6	
PCISERRN	I/O	P9	

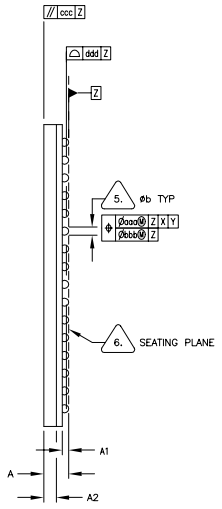
Table 24 RC32435 Alphabetical Signal List (Part 6 of 7)

RC32435 Package Drawing — 256-pin CABGA

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	06/09/00	D.G
	01	JEDEC VARIATION MODIFICATION	07/11/00	D.G
	02	UPDATE MAX. THICKNESS A	10/02/02	



TOP VIEW



SIDE VIEW

SYMBOL	JEDEC VARIATION AAF-1 MIN	NOM	MAX	NOTE
A	1.30	1.40	1.70	
A1	.31	.36	.41	
A2	.65	.70	.75	
D		17.00 BSC		
D1		15.00 BSC		
E		17.00 BSC		
E1		15.00 BSC		
MD		16		3
ME		16		3
N		256		4
e		1.00 BSC		
b	.41	.46	.51	5
aaa	–	–	.15	
bbb	–	–	.08	
ccc	–	–	.10	
ddd	–	–	.12	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS
DECIMAL: XX ±0.10, XXX ±0.05, XXXX ±0.08
ANGULAR: ±1°

APPROVALS	DATE
DRAWN	06/09/00
CHECKED	

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
(408) 727-6116 FAX (408) 492-8074

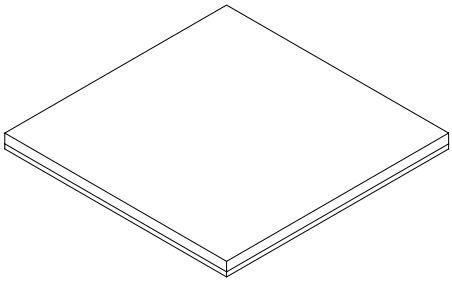
BC256 PACKAGE OUTLINE
17.0 X 17.0 mm BODY CABGA

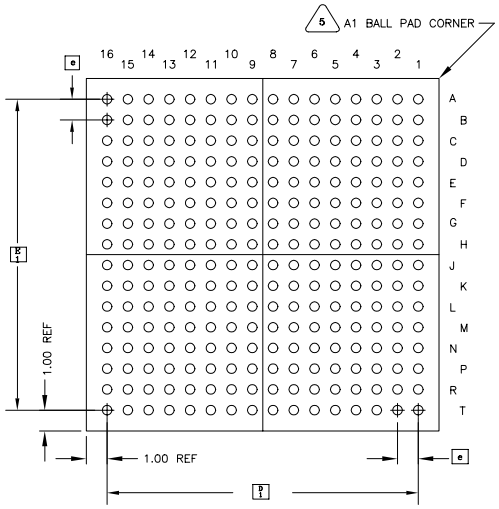
DRAWING No.	SIZE	SCALE	REV
PSC-4093	C	N/A	02

DO NOT SCALE DRAWING — SHEET 1 OF 2

RC32435 Package Drawing — Page Two

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	06/09/00	D.G
	01	JEDEC VARIATION MODIFICATION	07/11/00	D.G
	02	UPDATE MAX. THICKNESS A	10/02/02	





BOTTOM VIEW
256 SOLDER BALLS

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "MD" IS THE MAXIMUM SOLDER BALL MATRIX SIZE IN THE "D" DIRECTION.
   "ME" IS THE MAXIMUM SOLDER BALL MATRIX SIZE IN THE "E" DIRECTION.
4. "N" IS THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
6. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY.
8. ALL DIMENSIONS ARE IN MILLIMETERS.
9. THIS DRAWING CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–192 VARIATION AAF–1
   EXCEPTIONS:
   b MIN=0.41 NOM=0.46 MAX=0.51

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS
DECIMAL: X.X ±0.10, X.XX ±0.05, X.XXX ±0.00
ANGULAR: ±1°

APPROVALS	DATE
DRAWN BX	06/09/00
CHECKED	

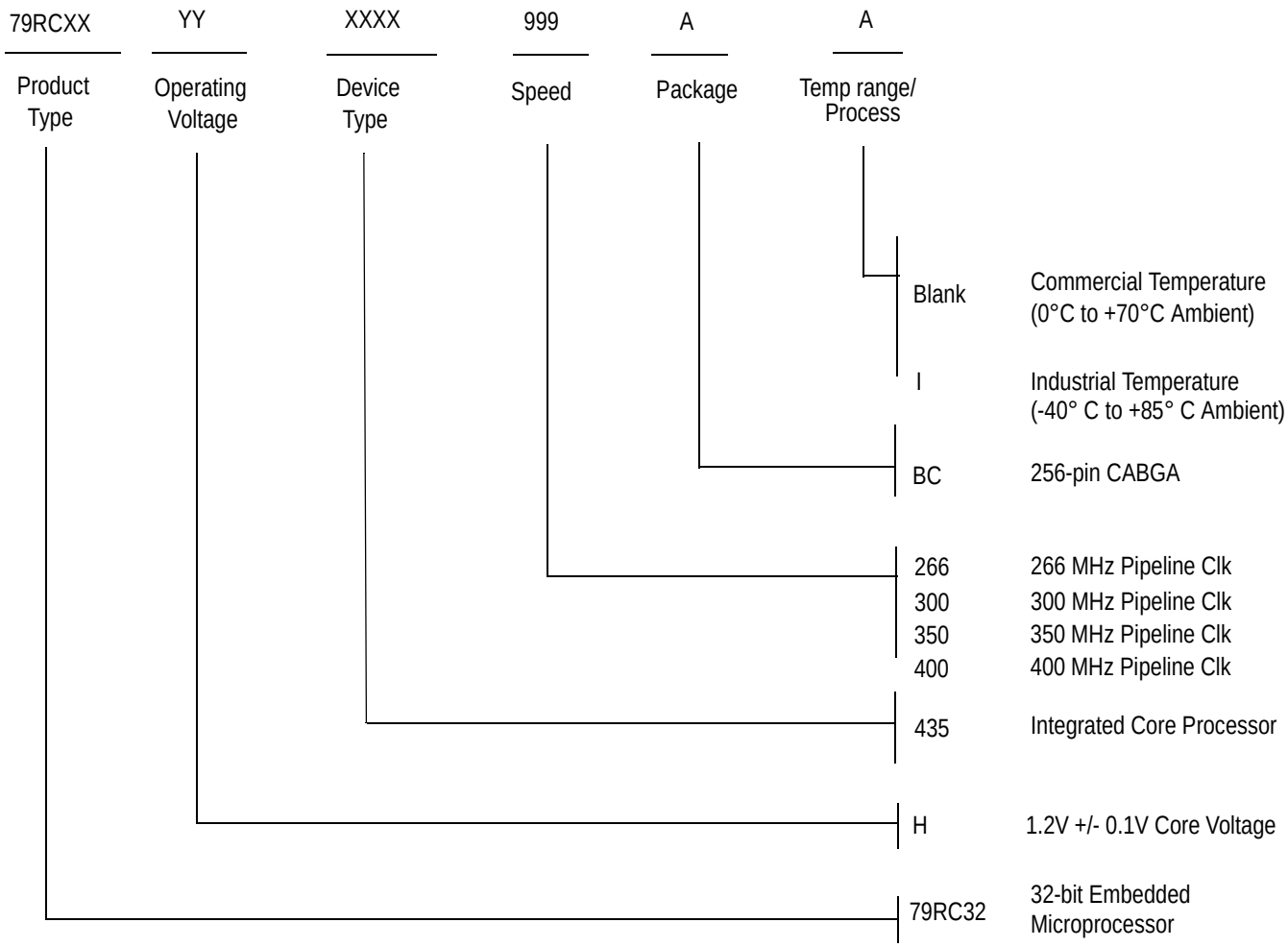
Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
(408) 727–6116 FAX (408) 492–8074

BC256 PACKAGE OUTLINE
17.0 X 17.0 mm BODY CABGA

DRAWING No.	SIZE	SCALE	REV
PSC–4093	C	N/A	02

DO NOT SCALE DRAWING — SHEET 2 OF 2

Ordering Information



Valid Combinations

79RC32H435 - 266BC, 300BC, 350BC, 400BC	256-pin CABGA package, Commercial Temperature
79RC32H435 - 266BCI, 300BCI, 350BCI	256-pin CABGA package, Industrial Temperature

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