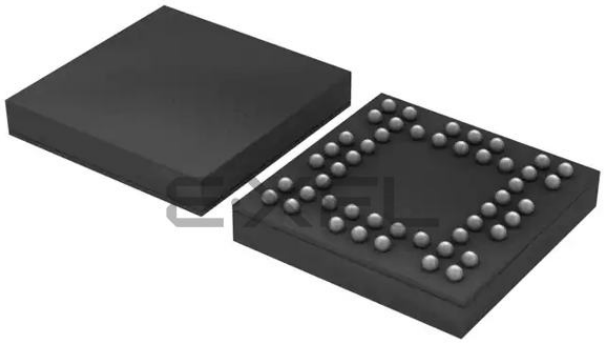

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SmartCard, SPI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TFBGA
Supplier Device Package	48-TFBGA (4.5x4.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11u14fet48-201

- Up to 40 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, repeater mode, input inverter, and open-drain mode. Eight pins support a programmable glitch filter.
- Up to 8 GPIO pins can be selected as edge and level sensitive interrupt sources.
- Two GPIO grouped interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
- High-current source output driver (20 mA) on one pin (P0_7).
- High-current sink driver (20 mA) on true open-drain pins (P0_4 and P0_5).
- Four general purpose counter/timers with a total of up to 5 capture inputs and 13 match outputs.
- Programmable Windowed WatchDog Timer (WWDT) with a dedicated, internal low-power WatchDog Oscillator (WDO).

- Analog peripherals:
  - 10-bit ADC with input multiplexing among eight pins.
- Serial interfaces:
  - USB 2.0 full-speed device controller.
  - USART with fractional baud rate generation, internal FIFO, a full modem control handshake interface, and support for RS-485/9-bit mode and synchronous mode. USART supports an asynchronous smart card interface (ISO 7816-3).
  - Two SSP controllers with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting the full I^2C-bus specification and Fast-mode Plus with a data rate of up to 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - Crystal Oscillator with an operating range of 1 MHz to 25 MHz (system oscillator).
  - 12 MHz high-frequency Internal RC oscillator (IRC) that can optionally be used as a system clock.
  - Internal low-power, low-frequency WatchDog Oscillator (WDO) with programmable frequency output.
  - PLL allows CPU operation up to the maximum CPU rate with the system oscillator or the IRC as clock sources.
  - A second, dedicated PLL is provided for USB.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Power profiles residing in boot ROM allow optimized performance and minimized power consumption for any given application through one simple function call.
  - Processor wake-up from Deep-sleep and Power-down modes via reset, selectable GPIO pins, watchdog interrupt, or USB port activity.
  - Processor wake-up from Deep power-down mode using one special function pin.
  - Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.
  - Power-On Reset (POR).
  - Brownout detect with four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single 3.3 V power supply (1.8 V to 3.6 V).

- Temperature range −40 °C to +85 °C.
- Available as LQFP48, TFBGA48, and HVQFN33 packages.
- Pin compatible to the LPC134x series.

3. Applications

- Consumer peripherals
- Medical
- Industrial control
- Handheld scanners
- USB audio devices

4. Ordering information

Table 1. Ordering information

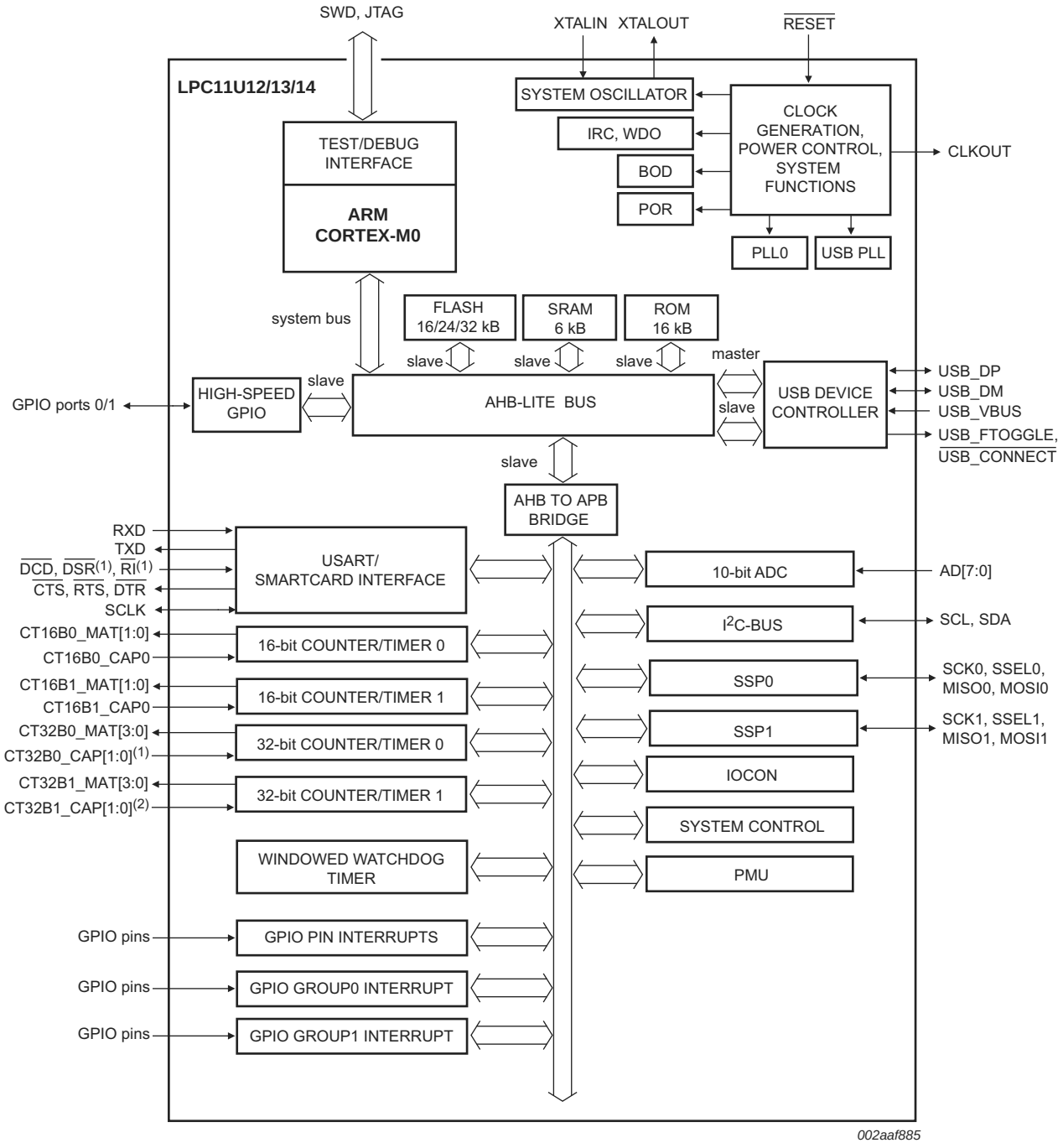
Type number	Package		
	Name	Description	Version
LPC11U12FHN33/201	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11U12FBD48/201	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U13FBD48/201	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U14FHN33/201	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11U14FHI33/201	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC11U14FBD48/201	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U14FET48/201	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 × 4.5 × 0.7 mm	SOT1155-2

4.1 Ordering options

Table 2. Ordering options

Type number	Flash	SRAM			USART	I^2C-bus FM+	SSP	USB device	ADC channels	GPIO pins
		CPU	USB	Total						
LPC11U12FHN33/201	16 kB	4 kB	2 kB	6 kB	1	1	2	1	8	26
LPC11U12FBD48/201	16 kB	4 kB	2 kB	6 kB	1	1	2	1	8	40
LPC11U13FBD48/201	24 kB	4 kB	2 kB	6 kB	1	1	2	1	8	40
LPC11U14FHN33/201	32 kB	4 kB	2 kB	6 kB	1	1	2	1	8	26
LPC11U14FHI33/201	32 kB	4 kB	2 kB	6 kB	1	1	2	1	8	26
LPC11U14FBD48/201	32 kB	4 kB	2 kB	6 kB	1	1	2	1	8	40
LPC11U14FET48/201	32 kB	4 kB	2 kB	6 kB	1	1	2	1	8	40

5. Block diagram



(1) DSR, RI, CT32B0_CAP1 are not available on HVQFN33 packages.

(2) CT32B1_CAP1 is available only on the TFBGA48package.

Fig 1. Block diagram

6.2 Pin description

Table 3 shows all pins and their assigned digital or analog functions ordered by GPIO port number. The default function after reset is listed first. All port pins have internal pull-up resistors enabled after reset with the exception of the true open-drain pins PIO0_4 and PIO0_5.

Every port pin has a corresponding IOCON register for programming the digital or analog function, the pull-up/pull-down configuration, the repeater, and the open-drain modes.

The USART, counter/timer, and SSP functions are available on more than one port pin. Table 4 shows how peripheral functions are assigned to port pins.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin LQFP48	Ball TFBGA48	Reset state [1]	Type	Description
$\overline{\text{RESET}}$/PIO0_0	2	3	C1 [2]	I; PU	I	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed and Deep power-down mode is not used.
				-	I/O	**PIO0_0 —** General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2/ USB_FTOGGLE	3	4	C2 [3][4]	I; PU	I/O	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
				-	O	**CLKOUT —** Clockout pin.
				-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
				-	O	**USB_FTOGGLE —** USB 1 ms Start-of-Frame signal.
PIO0_2/SSEL0/ CT16B0_CAP0	8	10	F1 [3]	I; PU	I/O	**PIO0_2 —** General purpose digital input/output pin.
				-	I/O	**SSEL0 —** Slave select for SSP0.
				-	I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3/USB_VBUS	9	14	H2 [3]	I; PU	I/O	**PIO0_3 —** General purpose digital input/output pin.
				-	I	**USB_VBUS —** Monitors the presence of USB bus power.

Table 3. Pin description *…continued*

Symbol	Pin HVQFN33	Pin LQFP48	Ball TFBGA48	Reset state [1]	Type	Description
PIO1_24/CT32B0_MAT0	-	21	G6 [3]	I; PU	I/O	**PIO1_24 —** General purpose digital input/output pin.
				-	O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO1_25/CT32B0_MAT1	-	1	A1 [3]	I; PU	I/O	**PIO1_25 —** General purpose digital input/output pin.
				-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_26/CT32B0_MAT2/ RXD	-	11	G2 [3]	I; PU	I/O	**PIO1_26 —** General purpose digital input/output pin.
				-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
				-	I	**RXD —** Receiver input for USART.
PIO1_27/CT32B0_MAT3/ TXD	-	12	G1 [3]	I; PU	I/O	**PIO1_27 —** General purpose digital input/output pin.
				-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
				-	O	**TXD —** Transmitter output for USART.
PIO1_28/CT32B0_CAP0/ SCLK	-	24	H7 [3]	I; PU	I/O	**PIO1_28 —** General purpose digital input/output pin.
				-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
				-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.
PIO1_29/SCK0/ CT32B0_CAP1	-	31	D7 [3]	I; PU	I/O	**PIO1_29 —** General purpose digital input/output pin.
				-	I/O	**SCK0 —** Serial clock for SSP0.
				-	I	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0.
PIO1_31	-	25	- [3]	I; PU	I/O	**PIO1_31 —** General purpose digital input/output pin.
USB_DM	13	19	G5 [8]	F	-	**USB_DM —** USB bidirectional D− line.
USB_DP	14	20	H5 [8]	F	-	**USB_DP —** USB bidirectional D+ line.
XTALIN	4	6	D1 [9]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5	7	E1 [9]	-	-	Output from the oscillator amplifier.
V_{DD}	6; 29	8; 44	B4, E2	-	-	Supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
V_{SS}	33	5; 41	B5, D2	-	-	Ground.

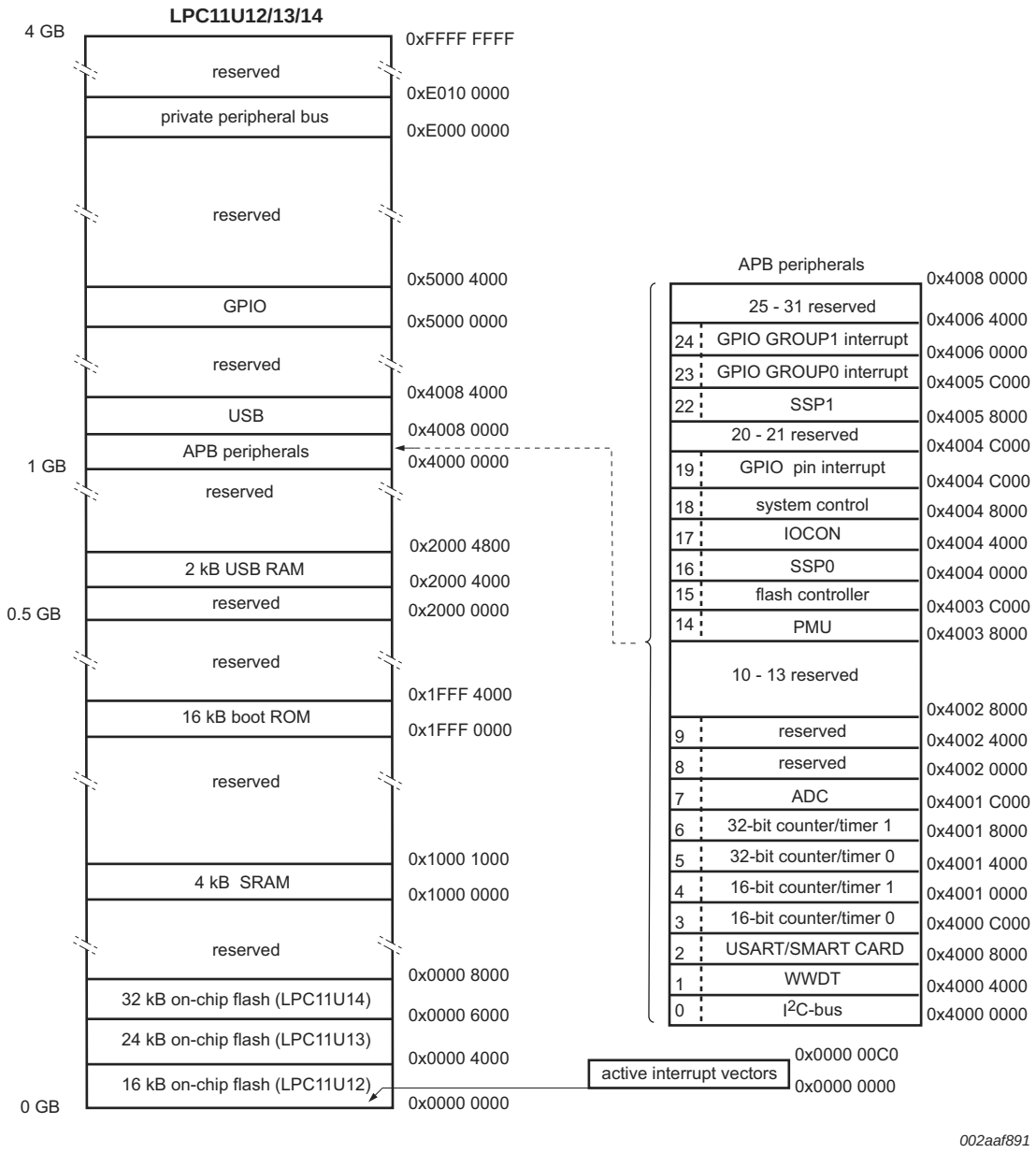


Fig 5. LPC11U1x memory map

7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11U1x, the NVIC supports 24 vectored interrupts.

- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.

7.14 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.15 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.15.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDO). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.16.5.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC11U1x for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

Remark: When using the USB, configure the LPC11U1x in Default mode.

7.16.5.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.16.5.3 Deep-sleep mode

In Deep-sleep mode, the LPC11U1x is in Sleep-mode and all peripheral clocks and all clock sources are off with the exception of the IRC. The IRC output is disabled unless the IRC is selected as input to the watchdog timer. In addition all analog blocks are shut down and the flash is in stand-by mode. In Deep-sleep mode, the user has the option to keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC11U1x can wake up from Deep-sleep mode via reset, selected GPIO pins, a watchdog timer interrupt, or an interrupt generating USB port activity.

Deep-sleep mode saves power and allows for short wake-up times.

7.16.5.4 Power-down mode

In Power-down mode, the LPC11U1x is in Sleep-mode and all peripheral clocks and all clock sources are off with the exception of watchdog oscillator if selected. In addition all analog blocks and the flash are shut down. In Power-down mode, the user has the option to keep the BOD circuit running for BOD protection.

The LPC11U1x can wake up from Power-down mode via reset, selected GPIO pins, a watchdog timer interrupt, or an interrupt generating USB port activity.

Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

7.16.5.5 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the WAKEUP pin. The LPC11U1x can wake up from Deep power-down mode via the WAKEUP pin.

The LPC11U1x can be prevented from entering Deep power-down mode by setting a lock bit in the PMU block. Locking out Deep power-down mode enables the user to always keep the watchdog timer or the BOD running.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. The $\overline{\text{RESET}}$ pin must also be held HIGH to prevent it from floating while in Deep power-down mode.

7.16.6 System control

7.16.6.1 Reset

Reset has four sources on the LPC11U1x: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin if Deep power-down mode is used.

7.16.6.2 Brownout detection

The LPC11U1x includes four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the four selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. Four additional threshold levels can be selected to cause a forced reset of the chip.

7.16.6.3 Code security (Code Read Protection - CRP)

This feature of the LPC11U1x allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details see the LPC11U1x *user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via the USART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details see the LPC11U1x *user manual*.

7.16.6.4 APB interface

The APB peripherals are located on one APB bus.

7.16.6.5 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the ROM.

7.16.6.6 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs.

Table 7. ADC static characteristics

T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz, V_{DD} = 2.5 V to 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DD}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	[3]	-	-	±1.5	LSB
E_O	offset error	[4]	-	-	±3.5	LSB
E_G	gain error	[5]	-	-	0.6	%
E_T	absolute error	[6]	-	-	±4	LSB
R_{vsi}	voltage source interface resistance		-	-	40	kΩ
R_i	input resistance	[7][8]	-	-	2.5	MΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 7.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 7.

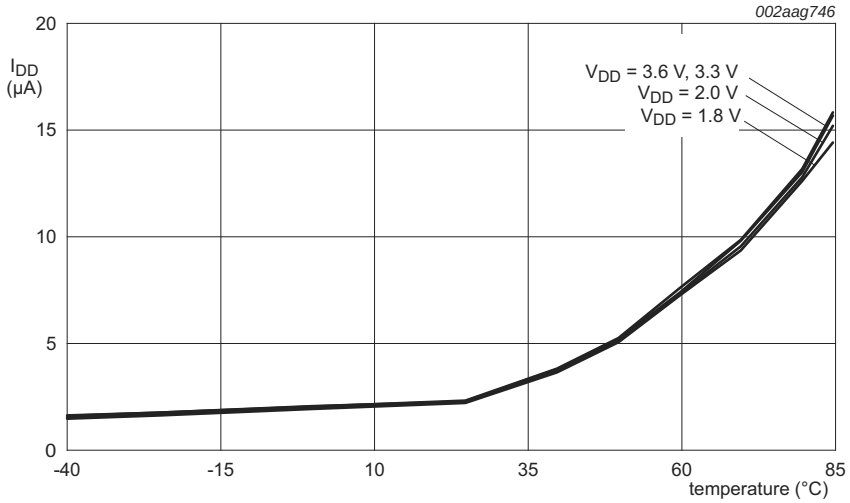
[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 7.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 7.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 7.

[7] T_{amb} = 25 °C; maximum sampling frequency f_s = 400kSamples/s and analog input capacitance C_{ia} = 1 pF.

[8] Input resistance R_i depends on the sampling frequency fs: $R_i = 1 / (f_s \times C_{ia})$.



Conditions: BOD disabled; all oscillators and analog blocks turned off in the PDSLEEPCFG register; USB_DP and USB_DM pulled LOW externally.

Fig 12. Typical supply current versus temperature in Power-down mode

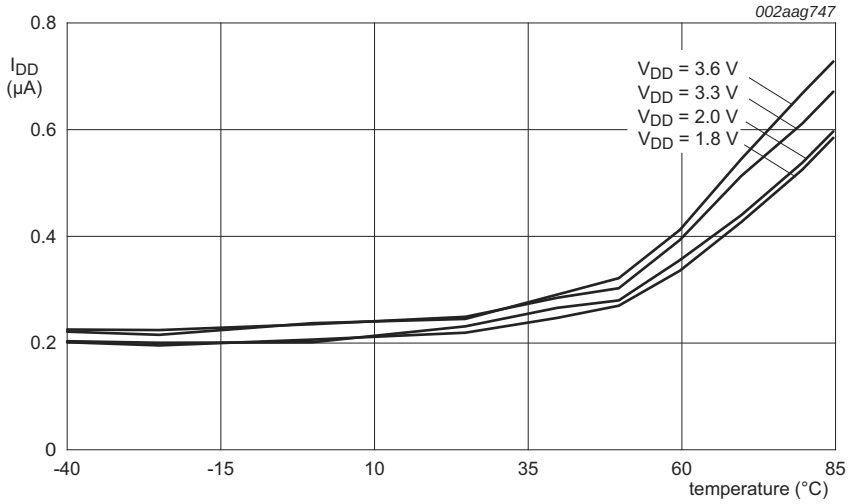


Fig 13. Typical supply current versus temperature in Deep power-down mode

9.3 Peripheral power consumption

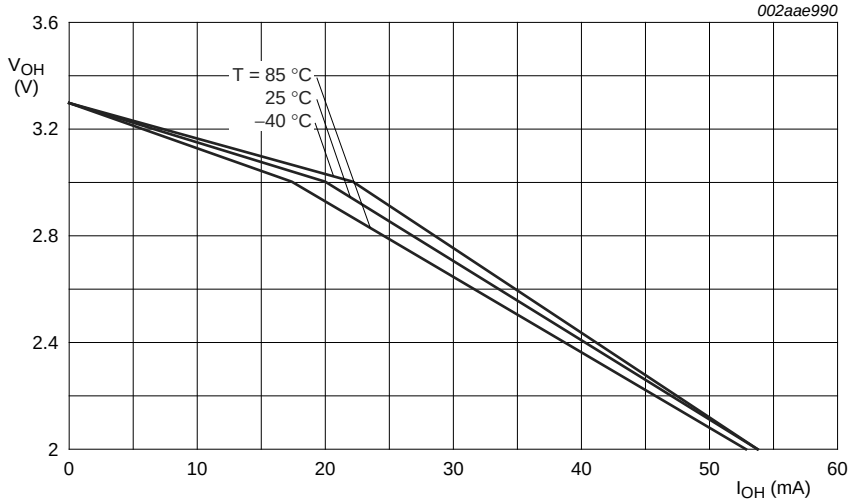
The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

Table 9. Power consumption for individual analog and digital blocks

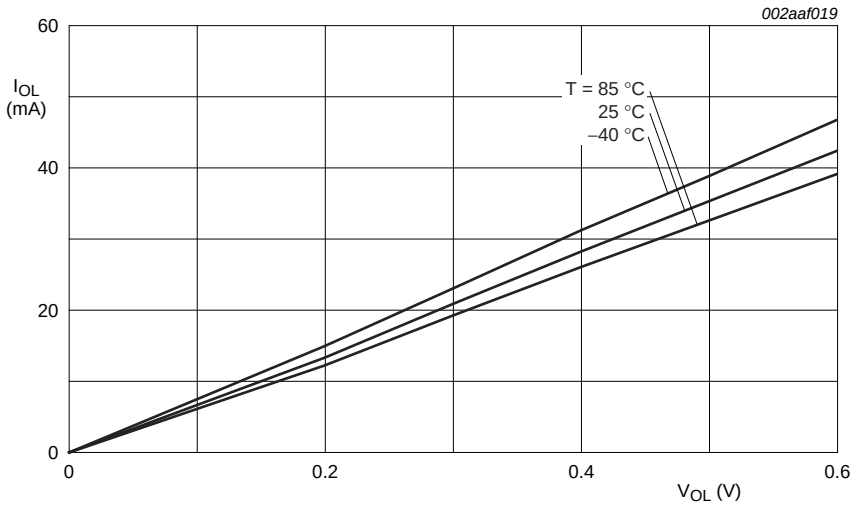
Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.27	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.22	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.004	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.051	-	-	Independent of main clock frequency.
Main PLL	-	0.21	-	-
ADC	-	0.08	0.29	-
CLKOUT	-	0.12	0.47	Main clock divided by 4 in the CLKOUTDIV register.
CT16B0	-	0.02	0.06	-
CT16B1	-	0.02	0.06	-
CT32B0	-	0.02	0.07	-
CT32B1	-	0.02	0.06	-
GPIO	-	0.23	0.88	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCONFIG	-	0.03	0.10	-
I2C	-	0.04	0.13	-
ROM	-	0.04	0.15	-
SPI0	-	0.12	0.45	-
SPI1	-	0.12	0.45	-
UART	-	0.22	0.82	-
WWDT	-	0.02	0.06	Main clock selected as clock source for the WDT.
USB	-	-	1.2	-

9.4 Electrical pin characteristics



Conditions: V_{DD} = 3.3 V; on pin PIO0_7.

Fig 14. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}.



Conditions: V_{DD} = 3.3 V; on pins PIO0_4 and PIO0_5.

Fig 15. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

For a bus-powered device, the VBUS signal does not need to be connected to the USB_VBUS pin (see Figure 27). The USB_CONNECT function can additionally be connected as shown in Figure 26 to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic.

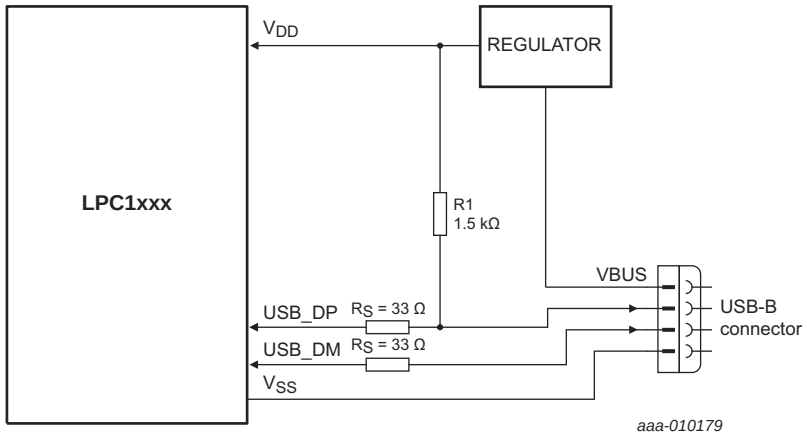


Fig 27. USB interface on a bus-powered device

Remark: When a bus-powered circuit as shown in Figure 27 is used, configure the PIO0_3/USB_VBUS pin for GPIO (PIO0_3) in the IOCON block to ensure that the USB_CONNECT signal can still be controlled by software. For details on the soft-connect feature, see the LPC11U1x *user manual* (Ref. 1).

Remark: When a self-powered circuit is used without connecting VBUS, configure the PIO0_3/USB_VBUS pin for GPIO (PIO0_3) and provide software that can detect the host presence through some other mechanism before enabling USB_CONNECT and the soft-connect feature. Enabling the soft-connect without host presence will lead to USB compliance failure.

11.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

Table 18. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

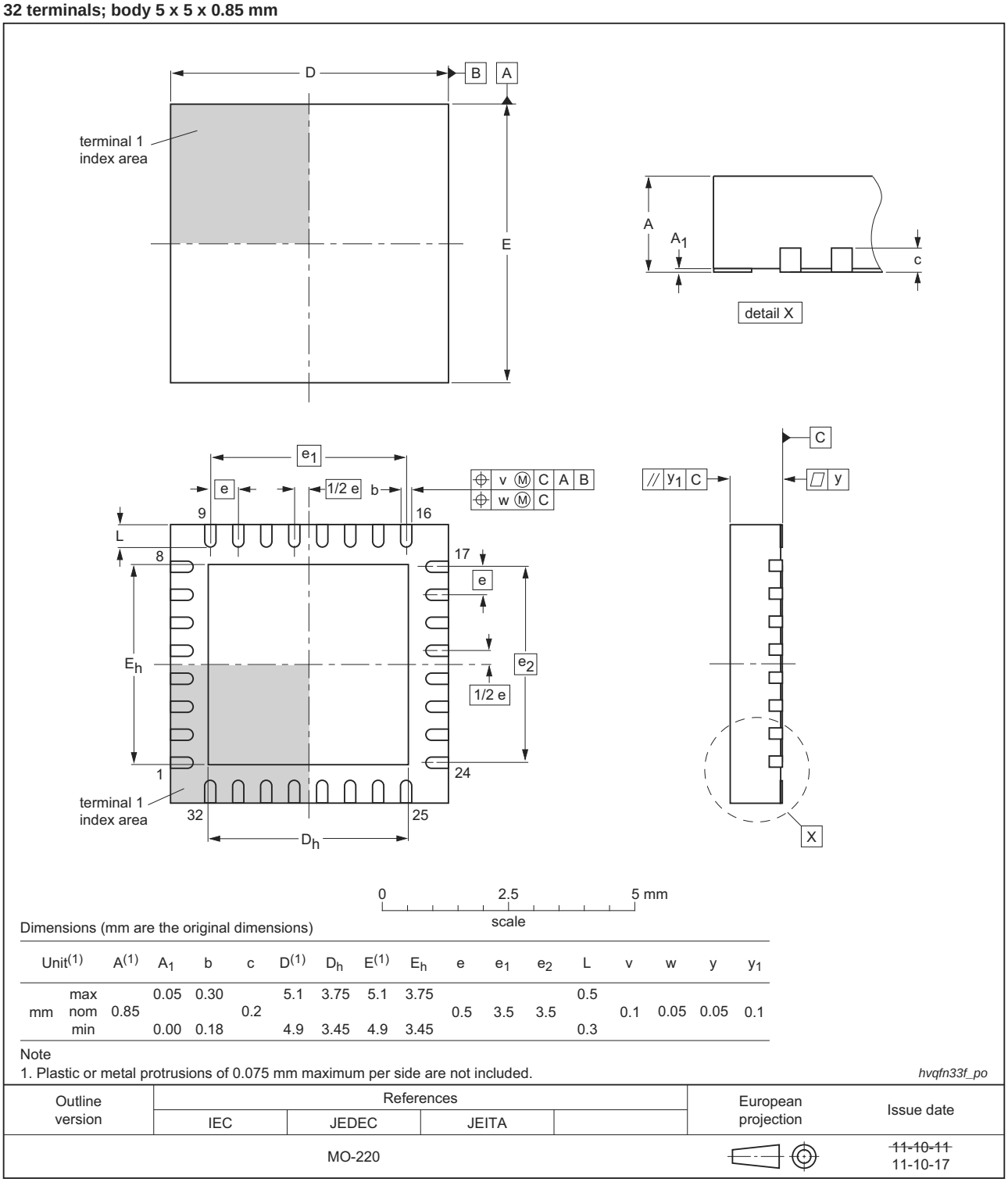
Table 19. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

11.3 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm



Dimensions (mm are the original dimensions)

Unit[1]		A[1]	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

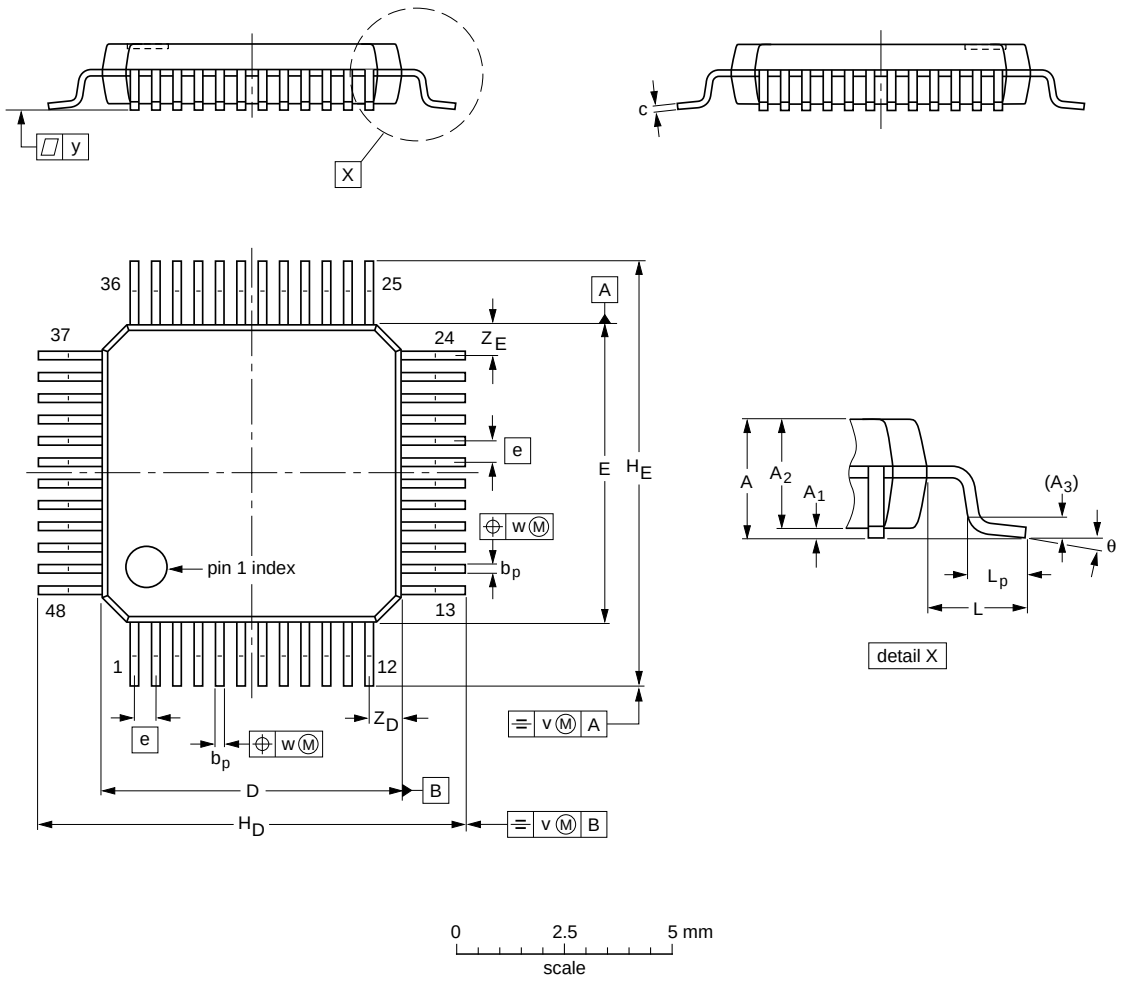
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33f_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		MO-220				~~11-10-11~~ 11-10-17

Fig 34. Package outline HVQFN33 (5 x 5 x 0.85 mm)

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 35. Package outline LQFP48 (SOT313-2)

Footprint information for reflow soldering of HVQFN33 package

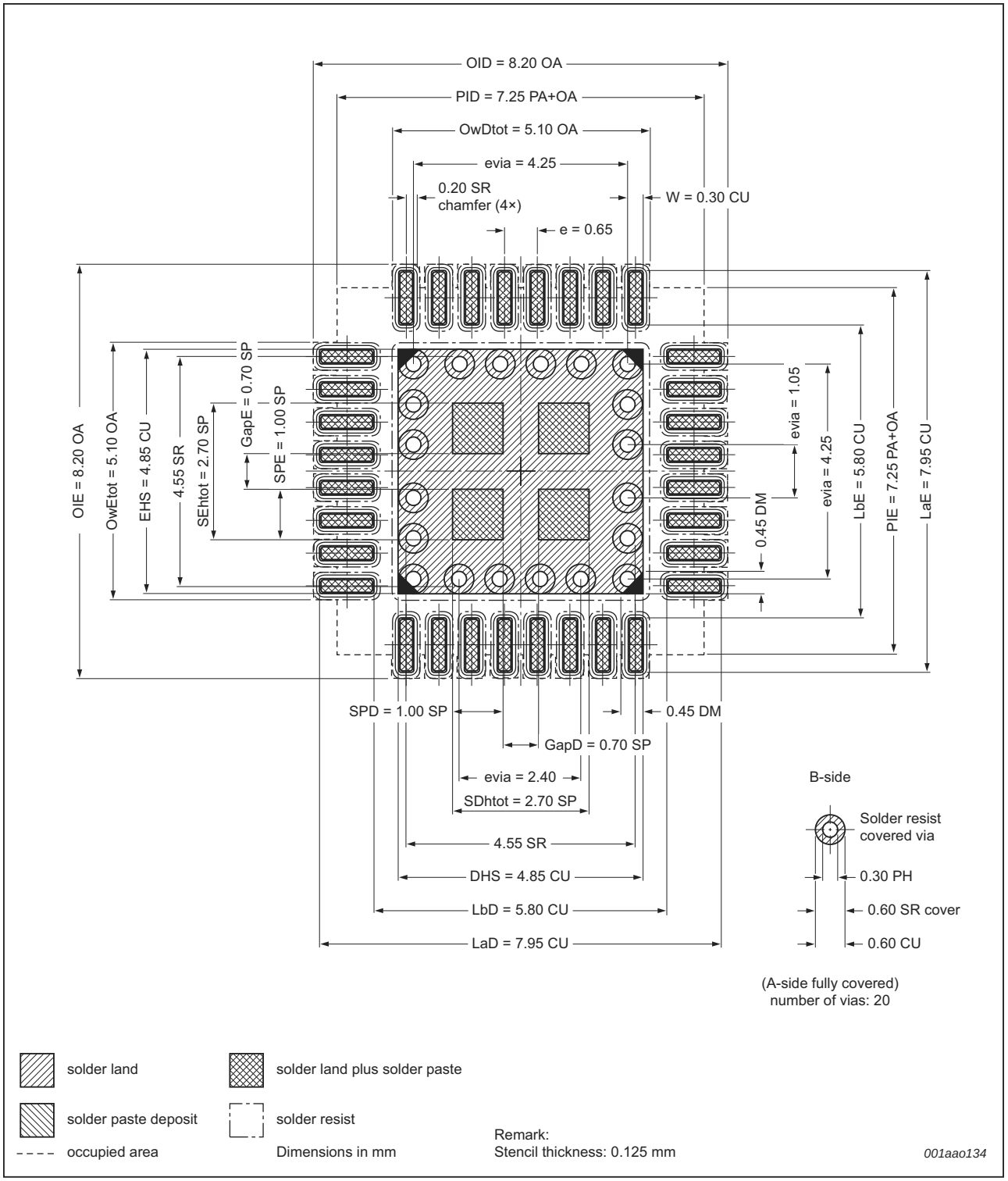


Fig 38. Reflow soldering for the HVQFN33 (7x7) package

16. Revision history

Table 21. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC11U1X v.2.2	20140311	Product data sheet	-	LPC11U1X v.2.1
Modifications:	• Updated Section 11.1 “Suggested USB interface solutions” for clarity. • Open-drain I2C-bus and RESET pin descriptions updated for clarity. See Table 3.			
LPC11U1X v.2.1	20130924	Product data sheet	-	LPC11U1X v.2
Modifications:	• Number of CT16B0 match outputs corrected in Figure 1. • Table 3: – Added Table note 2 “5 V tolerant pad” to $\overline{\text{RESET}}$/PIO0_0. – Added Table note 4 “For parts with bootloader version 7.0...” . • Table 8: Removed BOD interrupt level 0. • Added Section 11.6 “ADC effective input impedance”. • Programmable glitch filter is enabled by default. See Section 7.6.1. • Table 6 “Static characteristics” added Pin capacitance section. • Updated Section 11.1 “Suggested USB interface solutions”. • Table 5 “Limiting values”: – Updated V_{DD} min and max. – Updated V_I conditions. • Changed title of Figure 28 from “USB interface on a self-powered device” to “USB interface with soft-connect”. • Section 10.7 “USB interface” added. Parameter t_{EOPR1} and t_{EOPR2} renamed to t_{EOPR}.			
LPC11U1X v.2	20120111	Product data sheet	-	LPC11U1X v.1
Modifications:	• Number of physical and logical endpoints corrected in Section 7.8.1. • Use of JTAG updated in Section 2 (for BSDL only). • Sampling frequency corrected in Table note 7 of Table 7. • Conditions for parameter T_{stg} updated in Table 5. • Part LPC11U14FHI33/201 added. • Editorial updates. • ROM-based integer division routines added (Section 2). • Use of USB with power profiles specified (Section 7.8). • Power consumption data added in Section 9.2. • SSP dynamic characteristics added (Table 16). • IRC dynamic characteristics added (Table 12). • Data sheet status changed to Product data sheet. • Section 13 added. • Description of pin PIO0_3 updated in Table 3: this pin is not used by the boot loader.			
LPC11U1X v.1	20110411	Objective data sheet	-	-