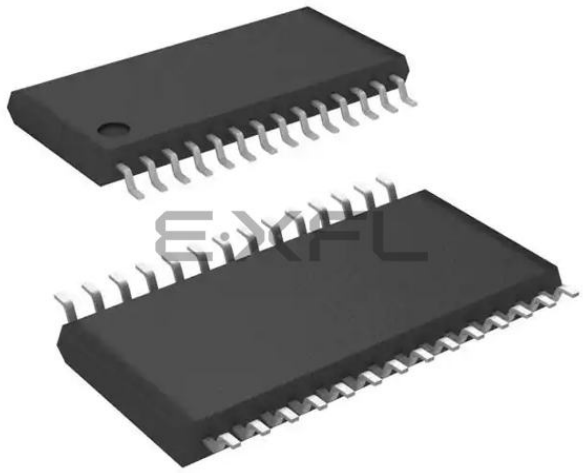

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Last Time Buy |
| Core Processor | XC800 |
| Core Size | 8-Bit |
| Speed | 24MHz |
| Connectivity | I²C, SSC, UART/USART |
| Peripherals | Brown-out Detect/Reset, LED, POR, PWM, WDT |
| Number of I/O | 23 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-TSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | PG-TSSOP-28-1 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xc8362friabfxuma1 |

# XC835/836

8-Bit Single-Chip Microcontroller

Data Sheet

V1.4 2011-10

Microcontrollers

# 1 Summary of Features

The XC835/836 has the following features:

- High-performance XC800 Core
  - compatible with standard 8051 processor
  - two clocks per machine cycle architecture (for memory access without wait state)
  - two data pointers
- On-chip memory
  - 8 Kbytes of Boot ROM, Library ROM and User routines
  - 256 bytes of RAM
  - 256 bytes of XRAM
  - 4/8 Kbytes of Flash (includes memory protection strategy)
- I/O port supply at 2.5 V - 5.5 V and core logic supply at 2.5 V (generated by embedded voltage regulator)

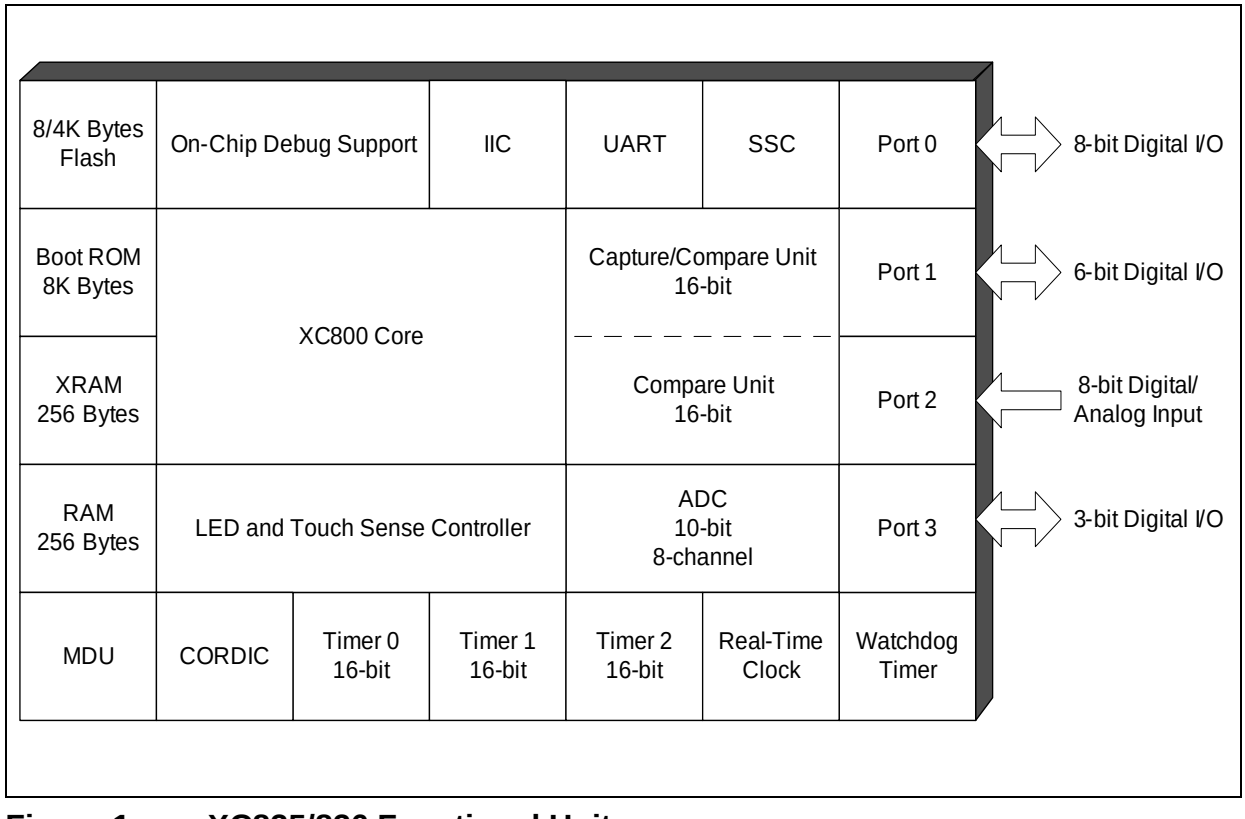


**Figure 1 XC835/836 Functional Units**

- Power-on reset generation
- Brownout detection for IO supply and core logic supply
- 48 MHz on-chip OSC for clock generation
  - Loss-of-Clock detection

(more features on next page)

Features: (continued)

- Power saving modes
  - idle mode
  - power-down mode with wake-up capability via real-time clock event
  - clock gating control to each peripheral
- Programmable 16-bit Watchdog Timer (WDT) running on independent oscillator with programmable window feature for refresh operation and warning prior to overflow
- Three general purpose I/O ports
  - 4 high current I/O
  - 2 high sink I/O
  - Up to 25 pins as digital I/O
  - Up to 8 pins as digital/analog input
- Up to 8 channels, 10-bit A/D Converter
  - support up to 7 differential input channel
  - results filtering by data reduction or digital low-pass filter, for up to 13-bit results
- Up to 8 channels, Out of range comparator
- Three 16-bit timers
  - Timer 0 and Timer 1 (T0 and T1)
  - Timer 2 (T2)
- Real-time clock with 32.768 kHz crystal pad
- 16-bit Vector Computer for Field-Oriented Control (FOC)
  - Multiplication/Division Unit (MDU) for arithmetic calculation
  - CORDIC Unit for trigonometric calculation
- Capture and Compare unit for PWM signal generation (CCU6)
- A full-duplex or half-duplex serial interface (UART)
- Synchronous serial channel (SSC)
- Inter-IC (IIC) serial interface
- LED and Touch-sense Controller (LEDTSCU)
- Software libraries to support fixed-point control and EEPROM emulation
- On-chip debug support via single pin DAP interface (SPD)
- Packages:
  - PG-DSO-24
  - PG-TSSOP-28
- Temperature range $T_A$:
  - SAF (-40 to 85 °C)
  - SAK (-40 to 125 °C)

### XC835/836 Variant Devices

The XC835/836 product family features devices with different configurations, program memory sizes, packages options and temperature profiles, to offer cost-effective solutions for different application requirements.

The list of XC835/836 device configurations are summarized in **Table 1**. The type of packages available are DSO-24 for XC835 and TSSOP-28 for XC836.

**Table 1 Device Configuration**

| Device Name | MDU and CORDIC Module | LEDTSCU Module |
|---|---|---|
| XC835/836 | No | No |
| XC835/836M | Yes | No |
| XC835/836T | No | Yes |
| XC835/836MT | Yes | Yes |

**Table 2** shows the device sales type available, based on above device.

**Table 2 Device Profile**

| Sales Type | Device Type | Program Memory (Kbytes) | Temp-erature Profile (°C) | Package Type | Quality Profile |
|---|---|---|---|---|---|
| SAF-XC835MT-2FGI | Flash | 8 | -40 to 85 | PG-DSO-24-1 | Industrial |
| SAF-XC836-2FRI | Flash | 8 | -40 to 85 | PG-TSSOP-28-1 | Industrial |
| SAF-XC836T-2FRI | Flash | 8 | -40 to 85 | PG-TSSOP-28-1 | Industrial |
| SAF-XC836M-2FRI | Flash | 8 | -40 to 85 | PG-TSSOP-28-1 | Industrial |
| SAF-XC836M-1FRI | Flash | 4 | -40 to 85 | PG-TSSOP-28-1 | Industrial |
| SAF-XC836MT-2FRI | Flash | 8 | -40 to 85 | PG-TSSOP-28-1 | Industrial |
| SAF-XC836-2FRA | Flash | 8 | -40 to 85 | PG-TSSOP-28-12 | Automotive |
| SAF-XC836MT-2FRA | Flash | 8 | -40 to 85 | PG-TSSOP-28-12 | Automotive |
| SAF-XC836MT-1FRA | Flash | 4 | -40 to 85 | PG-TSSOP-28-12 | Automotive |
| SAK-XC836MT-2FRA | Flash | 8 | -40 to 125 | PG-TSSOP-28-12 | Automotive |
| SAK-XC836MT-1FRA | Flash | 4 | -40 to 125 | PG-TSSOP-28-12 | Automotive |

As this document refers to all the derivatives, some description may not apply to a specific product. For simplicity, all versions are referred to by the term XC835/836 throughout this document.

## 2.3 Pin Configuration

The pin configuration of the XC835 in **Figure 4**.

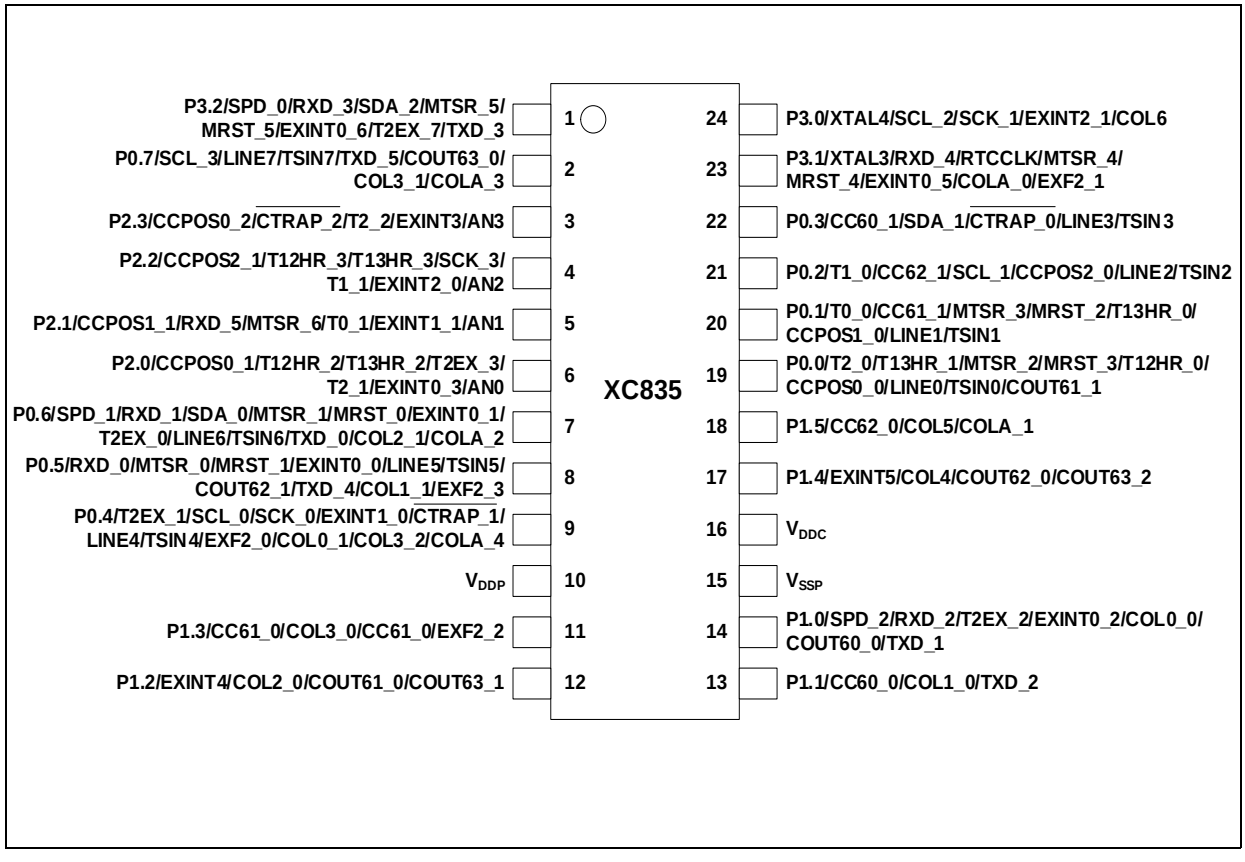


**Figure 4 XC835 Pin Configuration, PG-DSO-24 Package** (top view)

## 2.4 Pin Definitions and Functions

The functions and default states of the XC835/836 external pins are provided in **Table 3**.

**Table 3 Pin Definitions and Functions for XC835/836**

| Symbol | Pin Number TSSOP28/ DS024 | Type | Reset State | Function | |
|---|---|---|---|---|---|
| **P0** | | I/O | | **Port 0**<br>Port 0 is a bidirectional general purpose I/O port. It can be used as alternate functions for LEDTSCU, Timer 0, 1 and 2, SSC, CCU6, IIC, SPD and UART. | |
| P0.0 | 21/19 | | Hi-Z | T2_0 | Timer 2 Input |
| | | | | T13HR_1 | CCU6 Timer 13 Hardware Run Input |
| | | | | MTSR_2 | SSC Master Transmit Output/ Slave Receive Input |
| | | | | MRST_3 | SSC Master Receive Input |
| | | | | T12HR_0 | CCU6 Timer 12 Hardware Run Input |
| | | | | CCPOS0_0 | CCU6 Hall Input 0 |
| | | | | TSIN0 | Touch-sense Input 0 |
| | | | | LINE0 | LED Line 0 |
| | | | | COUT61_1 | Output of Capture/Compare Channel 1 |

**Table 3 Pin Definitions and Functions for XC835/836** (cont'd)

| Symbol | Pin Number TSSOP28/ DS024 | Type | Reset State | Function | |
|---|---|---|---|---|---|
| P2.2 | 6/4 | | Hi-Z | CCPOS2_1 | CCU6 Hall Input 2 |
| | | | | T12HR_3 | CCU6 Timer 12 Hardware Run Input |
| | | | | T13HR_3 | CCU6 Timer 13 Hardware Run Input |
| | | | | SCK_3 | SSC Clock Input/Output |
| | | | | T1_1 | Timer 1 Input |
| | | | | EXINT2_0 | External Interrupt Input 2 |
| | | | | AN2 | Analog Input 2 / Out of range comparator channel 2 |
| P2.3 | 5/3 | | Hi-Z | CCPOS0_2 | CCU6 Hall Input 0 |
| | | | | $\overline{\text{CTRAP}}$_2 | CCU6 Trap Input |
| | | | | T2_2 | Timer 2 Input |
| | | | | EXINT3 | External Interrupt Input 3 |
| | | | | AN3 | Analog Input 3 / Out of range comparator channel 3 |
| P2.4 | 4/- | | Hi-Z | T12HR_5 | CCU6 Timer 12 Hardware Run Input |
| | | | | T13HR_5 | CCU6 Timer 13 Hardware Run Input |
| | | | | T2_3 | Timer 2 Input |
| | | | | AN4 | Analog Input 4 / Out of range comparator channel 4 |
| P2.5 | 3/- | | Hi-Z | T12HR_7 | CCU6 Timer 12 Hardware Run Input |
| | | | | T13HR_7 | CCU6 Timer 13 Hardware Run Input |
| | | | | AN5 | Analog Input 5 / Out of range comparator channel 5 |

**Table 3 Pin Definitions and Functions for XC835/836** (cont'd)

| Symbol | Pin Number TSSOP28/ DS024 | Type | Reset State | Function | |
|---|---|---|---|---|---|
| P2.6 | 2/- | | Hi-Z | SCK_2 | SSC Clock Input/Output |
| | | | | EXINT6 | External Interrupt Input 6 |
| | | | | AN6 | Analog Input 6 / Out of range comparator channel 6 |
| P2.7 | 1/- | | Hi-Z | RXD_6 | UART Receive Input |
| | | | | T2EX_6 | Timer 2 External Trigger Input |
| | | | | MTSR_7 | SSC Slave Receive Input |
| | | | | EXINT0_4 | External Interrupt Input 0 |
| | | | | AN7 | Analog Input 7 / Out of range comparator channel 7 |
| **P3** | | I/O | | **Port 3** Port 3 is a bidirectional general purpose I/O port. It can be used as alternate functions for IIC, LEDTSCU, UART, Timer 2, SSC, SPD and 32.768 kHz crystal pad. | |
| P3.0 | 26/24 | | PU | SCL_2 | IIC Clock Line |
| | | | | SCK_1 | SSC Clock Input/Output |
| | | | | EXINT2_1 | External Interrupt Input 2 |
| | | | | COL6 | LED Column 6 |
| | | | | XTAL4 | 32.768 kHz External Oscillator Output |

### 3.1.3 Operating Condition

The following operating conditions must not be exceeded in order to ensure correct operation of the XC835/836. All parameters mentioned in the following tables refer to these operating conditions, unless otherwise noted.

**Table 7 Operating Condition Parameters**

| Parameter | Symbol | Limit Values | | Unit | Notes/ Conditions |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Digital power supply voltage | $V_{DDP}$ | 3.0 | 5.5 | V | |
| | | 2.5 | 3.0 | V | 1) |
| Digital core supply voltage2) | $V_{DDC}$ | 2.3 | 2.7 | V | |
| CPU Clock Frequency | $f_{CCLK}$ | 22.5 | 25.6 | MHz | typ. 24 MHz |
| | | 7.5 | 8.5 | MHz | typ. 8 MHz |
| Ambient temperature | $T_A$ | -40 | 85 | °C | SAF-XC835/836... |
| | | -40 | 125 | °C | SAK-XC836... |

1) In this voltage range, limited operations are available in active mode. Operations in power save modes are fully supported.

2) $V_{DDC}$ is supplied by the on-chip EVR. The limits are verified by design and production testing.

## 3.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

### 3.2.1 Input/Output Characteristics

**Table 8** provides the characteristics of the input/output pins of the XC835/836.

**Table 8 Input/Output Characteristics (Operating Conditions apply)**

| Parameter | Symbol | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Output low voltage on port pins (all except P1) | $V_{OLP}$ CC | – | 1.0 | V | $I_{OL}$ = 25 mA (5 V)<br>$I_{OL}$ = 13 mA (3.3 V) |
| | | – | 0.4 | V | $I_{OL}$ = 10 mA (5 V)<br>$I_{OL}$ = 5 mA (3.3 V) |
| Output low voltage on P1[3:0] | $V_{OLP1}$ CC | – | 1.0 | V | $I_{OL}$ = 50 mA (5 V)<br>$I_{OL}$ = 25 mA (3.3 V) |
| | | – | 0.32 | V | $I_{OL}$ = 20 mA (5 V) |
| | | – | 0.4 | V | $I_{OL}$ = 10 mA (3.3 V ) |
| Output low voltage on P1[5:4] | $V_{OLP2}$ CC | – | 1.0 | V | $I_{OL}$ = 50 mA (5 V)<br>$I_{OL}$ = 25 mA (3.3 V) |
| | | – | 0.4 | V | $I_{OL}$ = 20 mA (5 V)<br>$I_{OL}$ = 10 mA (3.3 V) |
| Output high voltage on port pins (all except P1) | $V_{OHP}$ CC | $V_{DDP}$ - 1.0 | – | V | $I_{OH}$ = -15 mA (5 V)<br>$I_{OH}$ = -8 mA (3.3 V ) |
| | | $V_{DDP}$ - 0.4 | – | V | $I_{OH}$ = -5 mA (5 V)<br>$I_{OH}$ = -2.5 mA (3.3 V) |
| Output high voltage on P1[3:0] | $V_{OHP1}$ CC | $V_{DDP}$ - 0.32 | – | V | $I_{OH}$ = -20 mA (5 V) |
| | | $V_{DDP}$ - 1.0 | – | V | $I_{OH}$ = -25 mA (3.3 V) |
| | | $V_{DDP}$ - 0.4 | – | V | $I_{OH}$ = -10 mA (3.3 V) |
| Output high voltage on P1[5:4] | $V_{OHP2}$ CC | $V_{DDP}$ - 1.0 | – | V | $I_{OH}$ = -30 mA (5 V)<br>$I_{OH}$ = -16 mA (3.3 V) |
| | | $V_{DDP}$ - 0.4 | – | V | $I_{OH}$ = -10 mA (5 V)<br>$I_{OH}$ =- 5 mA (3.3 V) |

**Table 8 Input/Output Characteristics (Operating Conditions apply)** (cont'd)

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| Voltage on any pin during $V_{DDP}$ power off | $V_{PO}$ | SR | – | 0.3 | V | 5) |
| Maximum current per pin (excluding P1, $V_{DDP}$ and $V_{SS}$) | $I_{MP}$ | SR | -15 | 25 | mA | – |
| Maximum current per pin for P1[3:0] | $I_{MP1A}$ | SR | -50 | 50 | mA | – |
| Maximum current per pin for P1[5:4] | $I_{MP1B}$ | SR | -30 | 50 | mA | – |
| Maximum current into $V_{DDP}$ | $I_{MVDDP}$ | SR | – | 130 | mA | 4) |
| Maximum current out of $V_{SS}$ | $I_{MVSS}$ | SR | – | 130 | mA | 4) |

1) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current ($I_{INJ}$) will flow if an overload current flows through an adjacent pin.

3) Over current detection is available for 5V application only.

4) Not subjected to production test, verified by design/characterization.

5) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when $V_{DDP}$ is powered off.

### 3.2.3 ADC Characteristics

The values in **Table 10** are given for an analog power supply of 5.0 V. The ADC can be used with an analog power supply down to 3 V. But in this case, analog parameters may show a reduced performance. In the reduced voltage mode (2.5 V < $V_{DDP}$ < 3 V), the ADC is not recommended to be used.

**Table 10 ADC Characteristics (Operating Conditions apply; $V_{DDP}$ = 5 V; $f_{ADCI}$ <= 12 MHz)**

| Parameter | Symbol | | Limit Values | | | Unit | Test Conditions / Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Analog reference voltage | $V_{AREF}$ | | – | $V_{DDP}$ | – | V | Connect internally to $V_{DDP}$ |
| Analog reference ground | $V_{AGND}$ | | – | $V_{SSP}$ | – | V | Connect internally to $V_{SSP}$ |
| Alternate analog reference ground | $V_{AGNDALT}$ | SR | $V_{SSP}$ - 0.1 | – | 2.5[1)] | V | Connect to AN0 in differential mode, See **Figure 9**. |
| Internal voltage reference | $V_{INTREF}$ | SR | 1.19 | 1.23 | 1.28 | V | [4)] |
| Analog input voltage range | $V_{AIN}$ | SR | $V_{AGND}$ | – | $V_{AREF}$ | V | – |
| ADC clock | $f_{ADCI}$ | | 8 | – | 16 | MHz | internal analog clock |
| Sample time | $t_S$ | CC | (2 + INPCR0.STC) × $t_{ADCI}$ | | | µs | – |
| Conversion time | $t_C$ | CC | See **Section 3.2.3.1** | | | µs | – |
| Set-up time between conversions using internal voltage reference | $t_{SETUP}$ | SR | – | 35 | – | µs | [2)] |

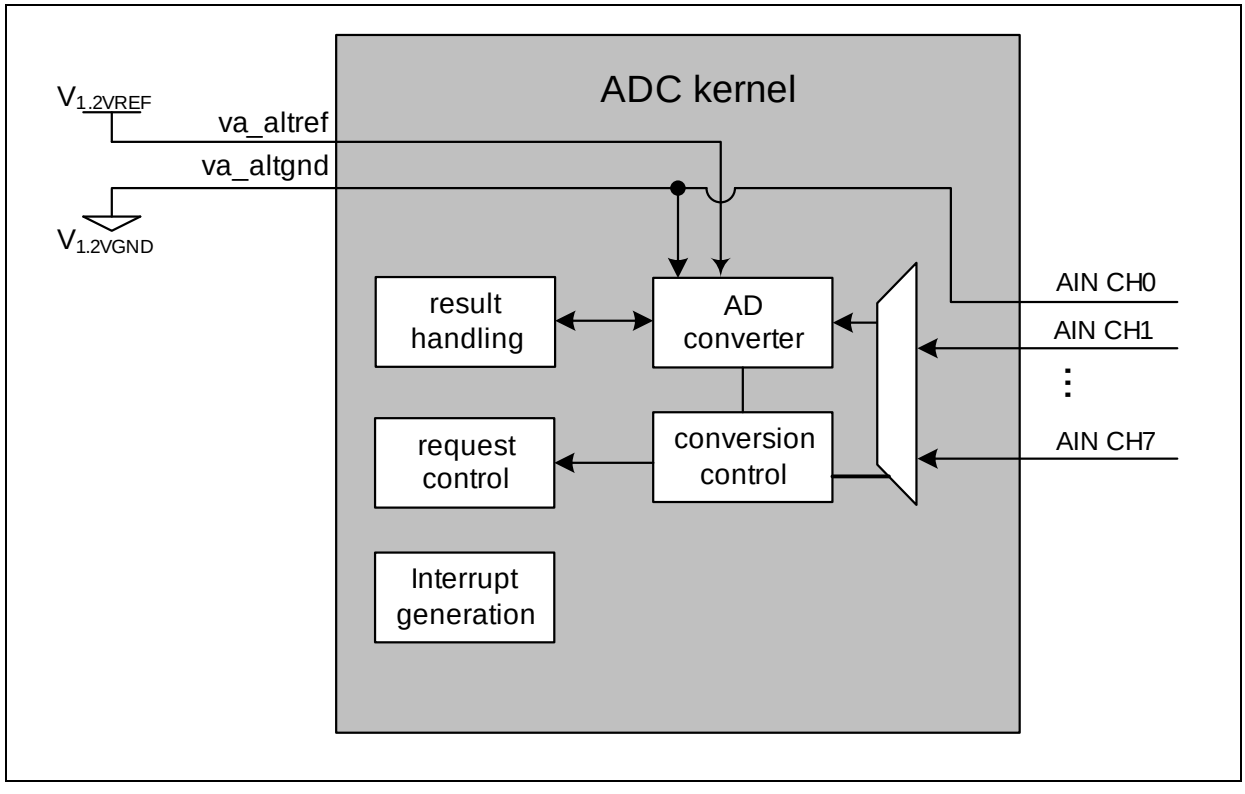


**Figure 9 Differential like measurement with internal 1.2V voltage reference, and CH0 gnd.**

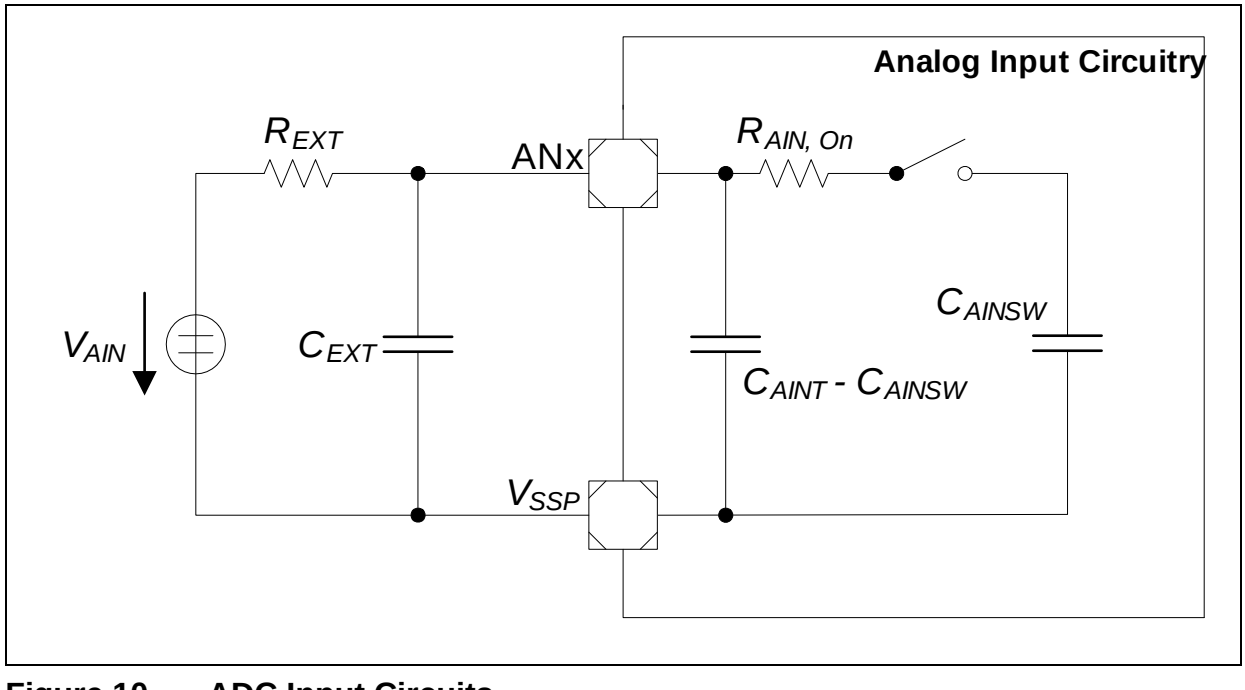


**Figure 10 ADC Input Circuits**

### 3.2.3.1 ADC Conversion Timing

Conversion time, $t_C = t_{ADC} \times (1 + r \times (3 + n + STC))$, where

- r = CTC + 3,
- CTC = Conversion Time Control (GLOBCTR.CTC),
- STC = Sample Time Control (INPCR0.STC),
- n = 8 or 10 (for 8-bit and 10-bit conversion respectively),
- $t_{ADC} = 1 / f_{ADC}$

### 3.2.3.2 Out of Range Comparator Characteristics

**Table 11** below shows the Out of Range Comparator characteristics.

**Table 11 Out of Range Comparator Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| DC Switching Level | $V_{SenseDC}$ | SR | 60 | 125 | 270 | mV | Above $V_{DDP}$ |
| DC Hysteresis | $V_{SenseHys}$ | CC | 30 | – | – | mV | 1) |
| Pulse Width | $t_{SensePW}$ | SR | 300 | – | – | ns | ANx > $V_{DDP}$ 1) |
| Switching Delay | $t_{SenseSD}$ | CC | – | – | 400 | ns | ANx >= $V_{DDP}$ + 350 mV 1) |
| Pulse Switching Level | $t_{SensePSL}$ | SR | – | 250 | – | mV | @ 300 nsec 1) |
| | | SR | – | 60 | – | mV | @ 800 usec 1) |

1) Not subject to production test, verified by design/characterization.

**Table 16** shows the maximum active current within the device in the reduced voltage condition of 2.5 V < $V_{DDP}$ < 3.0 V. The active current consumption needs to be below the specified values as according to the $V_{DDP}$ voltage. If the conditions are not met, a brownout reset may be triggered.

**Table 16 Active Current Consumption in Reduced Voltage Condition**

| $V_{DDP}$ | 2.5 V | 2.6 V | 2.7 V | 2.8 V |
|---|---|---|---|---|
| **Maximum active current** | 7 mA | 13 mA | 20 mA | 25 mA |

**Table 17** provides the active current consumption of some modules operating at 8 MHz active mode, 3 V power supply at 25 °C. The typical values shown are used as a reference guide for device operating in reduced voltage conditions.

**Table 17 Typical Active Current Consumption[1) 2)]**

| Active Current Consumption | Symbol | Limit Values | Unit | Test Condition |
|---|---|---|---|---|
| | | Typ. | | |
| Baseload current[3)] | $I_{CPUDDC}$ | 6900 | µA | Modules including Core, memories, UART, T0, T1 and EVR. Disable ADC analog (GLOBCTR.ANON = 0). |
| ADC[4)] | $I_{ADCDDC}$ | 3760 | µA | Set PMCON1.ADC_DIS to 0 and GLOBECTR. ANON to 1 |
| SSC[5)] | $I_{SSCDDC}$ | 460 | µA | Set PMCON1.SSC_DIS to 0 |
| CCU6[6)] | $I_{CCU6DDC}$ | 3320 | µA | Set PMCON1.CCU_DIS to 0 |
| Timer 2[7)] | $I_{T2DDC}$ | 200 | µA | Set PMCON1.T2_DIS to 0 |
| MDU[8)] | $I_{MDUDDC}$ | 1260 | µA | Set PMCON1.MDU_DIS to 0 |
| CORDIC[9)] | $I_{CORDICDDC}$ | 1880 | µA | Set PMCON1.CDC_DIS to 0 |
| LEDTSCU[10)] | $I_{LEDDDC}$ | 850 | µA | Set PMCON1.LTS_DIS to 0 |
| IIC[11)] | $I_{IICDDC}$ | 580 | µA | Set PMCON1.IIC_DIS to 0 |

1) Modules that are controllable by programming the register PMCON1.

2) Not subject to production test, verified by design/characterisation.

3) Baseload current is measured when the device is running in user mode with an endless loop in the flash memory. All modules in register PMCON1 are disabled.

4) ADC active current is measured with: module enable, ADC analog clock at 8MHz, running in parallel conversion request in autoscan mode for 4 channels

5) SSC active curremt is measured with: module enabled, running in loop back mode at a baud rate of 1 MBaud

6) CCU6 active current is measured with: module enabled, all timers running in 8 MHz, 6 PWM outputs are generated.

### 3.3.3 Oscillator Timing and Wake-up Timing

Table 19 provides the characteristics of the power-on reset, PLL and wake-up timings in the XC835/836.

**Table 19 Power-On Reset Wake-up Timing[1] (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 48 MHz Oscillator start-up time | $t_{48MOSCST}$ | CC | – | – | 13 | µs | |
| 75 KHz Oscillator start-up time | $t_{75KOSCST}$ | CC | – | – | 800 | µs | |
| 32 KHz external oscillator start-up time[2] | $t_{32KOSCST}$ | CC | – | – | 1 | s | |
| Flash initialization time | $t_{FINT}$ | CC | – | 160 | – | µs | |

1) Not subject to production test, verified by design/characterisation.

2) The external circuitry has to be optimized by the user and checked for negative resistance as recommended and specified by the crystal supplier.

### 3.3.4 On-Chip Oscillator Characteristics

**Table 20** provides the characteristics of the 48 MHz oscillator in the XC835/836.

**Table 20 48 MHz Oscillator Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Nominal frequency | $f_{NOM}$ | CC | -0.5 % | 48 | +0.5% | MHz | under nominal conditions[1] after trimming |
| Long term frequency deviation | $\Delta f_{LT}$ | CC | -2.0 | – | 3.0 | % | with respect to $f_{NOM}$, over lifetime and temperature (0 °C to 85 °C) |
| | | | -4.5 | – | 4.5 | % | with respect to $f_{NOM}$, over lifetime and temperature (-40 °C to 125 °C) |
| Short term frequency deviation (over $V_{DDC}$) | $\Delta f_{ST}$ | CC | -1 | – | 1 | % | with respect to $f_{NOM}$, within one LIN message (< 10 ms … 100 ms) |

1) Nominal condition: $V_{DDC}$ = 2.5 V, $T_A$ = + 25°C.

### 3.3.6 SPD Timing

The SPD interface will work with standard SPD tools having a sample/output clock frequency deviation of +/- 5% or less. For further details please refer to application note AP24004 in section SPD Timing Requirements.

*Note: These parameters are no subject to product test but verified by design and/or characterization.*

*Note: Operating Conditions apply.*

# 4 Package and Quality Declaration

**Chapter 4** provides the information of the XC835/836 package and reliability section.

## 4.1 Package Parameters

**Table 24** provides the thermal characteristics of the packages used in XC835 and XC836 respectively.

**Table 24 Thermal Characteristics of the Packages**

| Parameter | Symbol | Limit Values | | Unit | Package Types |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Thermal resistance junction case[1)] | $R_{TJC}$ CC | - | 30.8 | K/W | PG-DSO-24-1 |
| | | - | 27.0 | K/W | PG-TSSOP-28-1 |
| | | - | 20.2 | K/W | PG-TSSOP-28-12 |
| Thermal resistance junction lead[1)] | $R_{TJL}$ CC | - | 30.5 | K/W | PG-DSO-24-1 |
| | | - | 195.3 | K/W | PG-TSSOP-28-1 |
| | | - | 41 | K/W | PG-TSSOP-28-12 |

1) The thermal resistances between the case and the ambient ($R_{TCA}$) , the lead and the ambient ($R_{TLA}$) are to be combined with the thermal resistances between the junction and the case ($R_{TJC}$), the junction and the lead ($R_{TJL}$) given above, in order to calculate the total thermal resistance between the junction and the ambient ($R_{TJA}$). The thermal resistances between the case and the ambient ($R_{TCA}$), the lead and the ambient ($R_{TLA}$) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J=T_A+R_{TJA} \times P_D$, where the $R_{TJA}$ is the total thermal resistance between the junction and the ambient. This total junction ambient resistance $R_{TJA}$ can be obtained from the upper four partial thermal resistances, by
a) simply adding only the two thermal resistances (junction lead and lead ambient), or
b) by taking all four resistances into account, depending on the precision needed.

## 4.2 Package Outline

**Figure 17** and **Figure 18** shows the package outlines of the XC835 (DSO-24-1) and XC836 (TSSOP-28-1 and TSSOP-28-12) devices respectively.

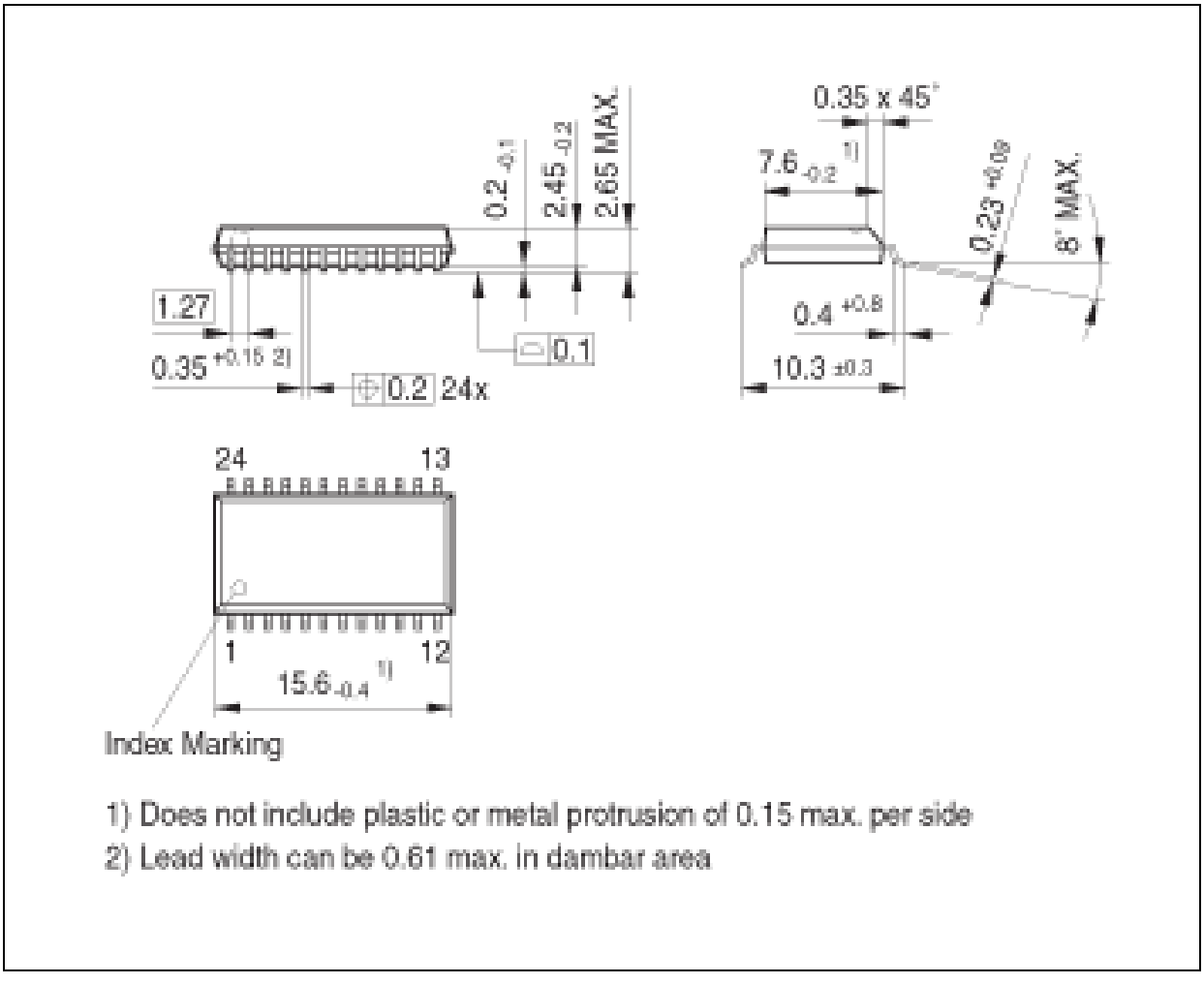


**Figure 17 PG-DSO-24-1 Package Outline**