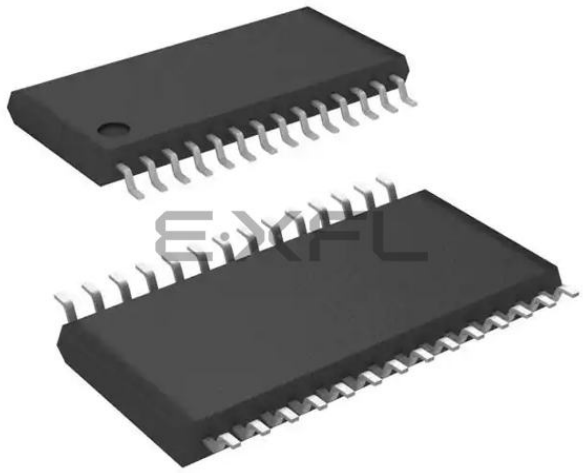
Infineon Technologies - XC836M2FRIABFXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-28-1
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc836m2friabfxuma1

1 Summary of Features

The XC835/836 has the following features:

- High-performance XC800 Core
  - compatible with standard 8051 processor
  - two clocks per machine cycle architecture (for memory access without wait state)
  - two data pointers
- On-chip memory
  - 8 Kbytes of Boot ROM, Library ROM and User routines
  - 256 bytes of RAM
  - 256 bytes of XRAM
  - 4/8 Kbytes of Flash (includes memory protection strategy)
- I/O port supply at 2.5 V - 5.5 V and core logic supply at 2.5 V (generated by embedded voltage regulator)

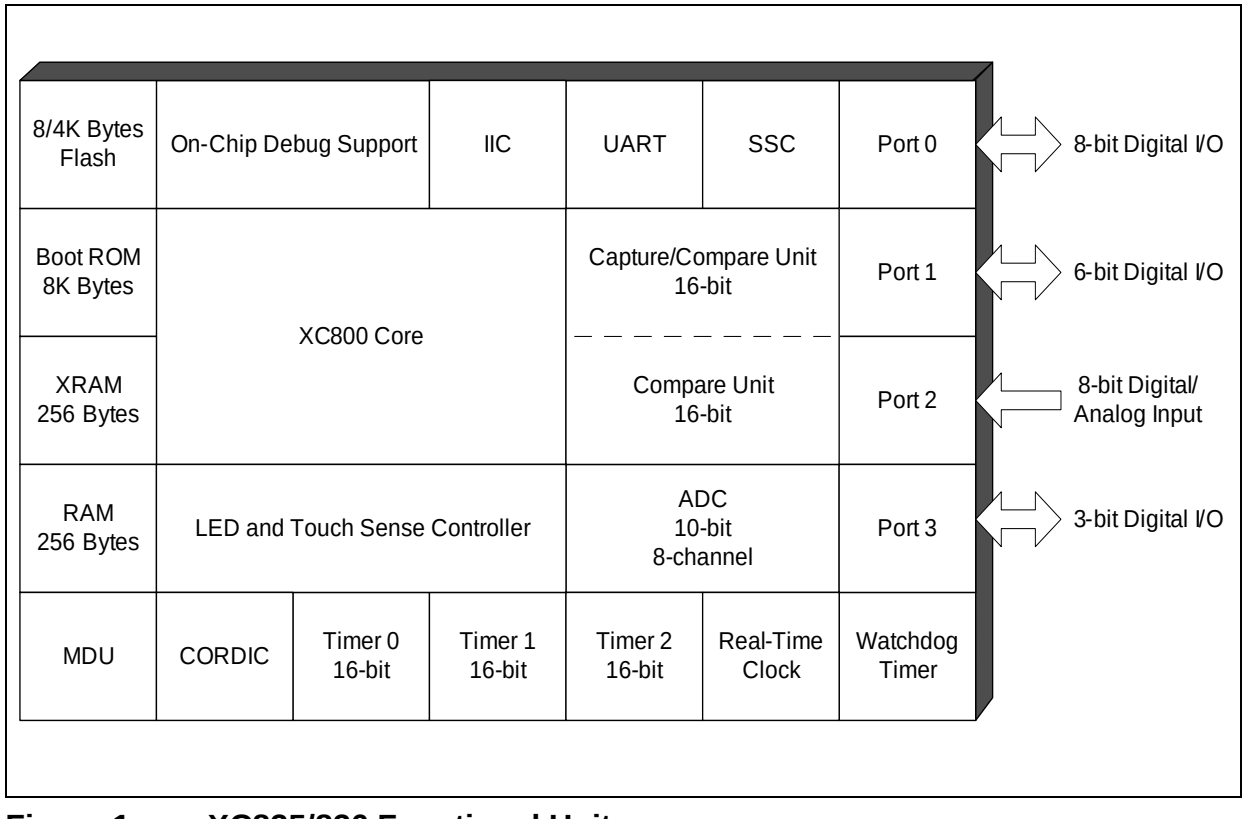


Figure 1 XC835/836 Functional Units

- Power-on reset generation
- Brownout detection for IO supply and core logic supply
- 48 MHz on-chip OSC for clock generation
  - Loss-of-Clock detection

(more features on next page)

Features: (continued)

- Power saving modes
  - idle mode
  - power-down mode with wake-up capability via real-time clock event
  - clock gating control to each peripheral
- Programmable 16-bit Watchdog Timer (WDT) running on independent oscillator with programmable window feature for refresh operation and warning prior to overflow
- Three general purpose I/O ports
  - 4 high current I/O
  - 2 high sink I/O
  - Up to 25 pins as digital I/O
  - Up to 8 pins as digital/analog input
- Up to 8 channels, 10-bit A/D Converter
  - support up to 7 differential input channel
  - results filtering by data reduction or digital low-pass filter, for up to 13-bit results
- Up to 8 channels, Out of range comparator
- Three 16-bit timers
  - Timer 0 and Timer 1 (T0 and T1)
  - Timer 2 (T2)
- Real-time clock with 32.768 kHz crystal pad
- 16-bit Vector Computer for Field-Oriented Control (FOC)
  - Multiplication/Division Unit (MDU) for arithmetic calculation
  - CORDIC Unit for trigonometric calculation
- Capture and Compare unit for PWM signal generation (CCU6)
- A full-duplex or half-duplex serial interface (UART)
- Synchronous serial channel (SSC)
- Inter-IC (IIC) serial interface
- LED and Touch-sense Controller (LEDTSCU)
- Software libraries to support fixed-point control and EEPROM emulation
- On-chip debug support via single pin DAP interface (SPD)
- Packages:
  - PG-DSO-24
  - PG-TSSOP-28
- Temperature range T_A:
  - SAF (-40 to 85 °C)
  - SAK (-40 to 125 °C)

XC835/836 Variant Devices

The XC835/836 product family features devices with different configurations, program memory sizes, packages options and temperature profiles, to offer cost-effective solutions for different application requirements.

The list of XC835/836 device configurations are summarized in **Table 1**. The type of packages available are DSO-24 for XC835 and TSSOP-28 for XC836.

Table 1 Device Configuration

Device Name	MDU and CORDIC Module	LEDTSCU Module
XC835/836	No	No
XC835/836M	Yes	No
XC835/836T	No	Yes
XC835/836MT	Yes	Yes

Table 2 shows the device sales type available, based on above device.

Table 2 Device Profile

Sales Type	Device Type	Program Memory (Kbytes)	Temp-erature Profile (°C)	Package Type	Quality Profile
SAF-XC835MT-2FGI	Flash	8	-40 to 85	PG-DSO-24-1	Industrial
SAF-XC836-2FRI	Flash	8	-40 to 85	PG-TSSOP-28-1	Industrial
SAF-XC836T-2FRI	Flash	8	-40 to 85	PG-TSSOP-28-1	Industrial
SAF-XC836M-2FRI	Flash	8	-40 to 85	PG-TSSOP-28-1	Industrial
SAF-XC836M-1FRI	Flash	4	-40 to 85	PG-TSSOP-28-1	Industrial
SAF-XC836MT-2FRI	Flash	8	-40 to 85	PG-TSSOP-28-1	Industrial
SAF-XC836-2FRA	Flash	8	-40 to 85	PG-TSSOP-28-12	Automotive
SAF-XC836MT-2FRA	Flash	8	-40 to 85	PG-TSSOP-28-12	Automotive
SAF-XC836MT-1FRA	Flash	4	-40 to 85	PG-TSSOP-28-12	Automotive
SAK-XC836MT-2FRA	Flash	8	-40 to 125	PG-TSSOP-28-12	Automotive
SAK-XC836MT-1FRA	Flash	4	-40 to 125	PG-TSSOP-28-12	Automotive

As this document refers to all the derivatives, some description may not apply to a specific product. For simplicity, all versions are referred to by the term XC835/836 throughout this document.

2.3 Pin Configuration

The pin configuration of the XC835 in **Figure 4**.

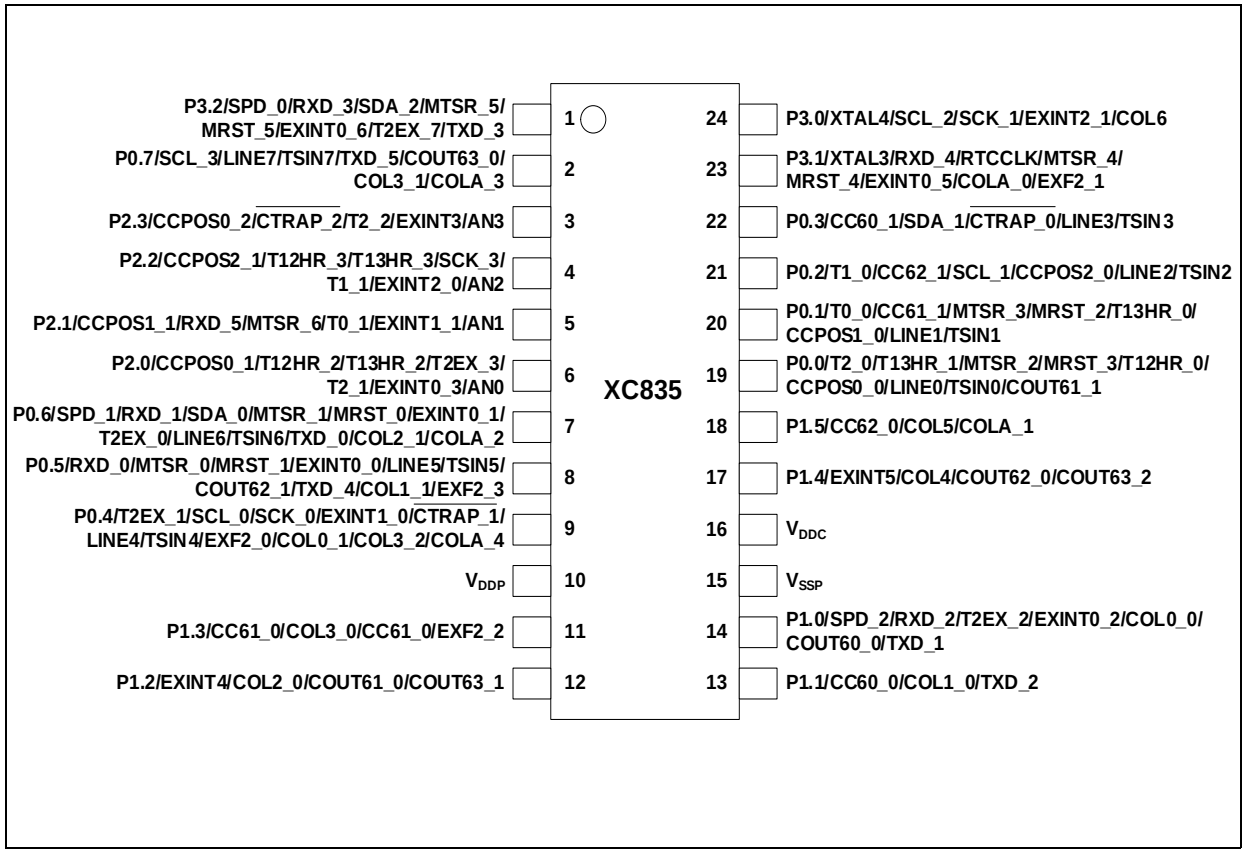


Figure 4 XC835 Pin Configuration, PG-DSO-24 Package (top view)

2.4 Pin Definitions and Functions

The functions and default states of the XC835/836 external pins are provided in **Table 3**.

Table 3 Pin Definitions and Functions for XC835/836

Symbol	Pin Number TSSOP28/ DS024	Type	Reset State	Function	
P0		I/O		**Port 0** Port 0 is a bidirectional general purpose I/O port. It can be used as alternate functions for LEDTSCU, Timer 0, 1 and 2, SSC, CCU6, IIC, SPD and UART.	
P0.0	21/19		Hi-Z	T2_0	Timer 2 Input
				T13HR_1	CCU6 Timer 13 Hardware Run Input
				MTSR_2	SSC Master Transmit Output/ Slave Receive Input
				MRST_3	SSC Master Receive Input
				T12HR_0	CCU6 Timer 12 Hardware Run Input
				CCPOS0_0	CCU6 Hall Input 0
				TSIN0	Touch-sense Input 0
				LINE0	LED Line 0
				COUT61_1	Output of Capture/Compare Channel 1

2.5 Memory Organization

The XC835/836 CPU operates in the following five address spaces:

- 8 Kbytes of Boot ROM, Library ROM and User routines
- 256 bytes of internal RAM
- 256 bytes of XRAM
  (XRAM can be read/written as program memory or external data memory)
- A 128-byte Special Function Register area
- 4/8 Kbytes of Flash

Figure 6 illustrates the memory address spaces of the 4 Kbyte Flash devices. **Figure 7** illustrates the memory address spaces of the 8 Kbyte Flash devices.

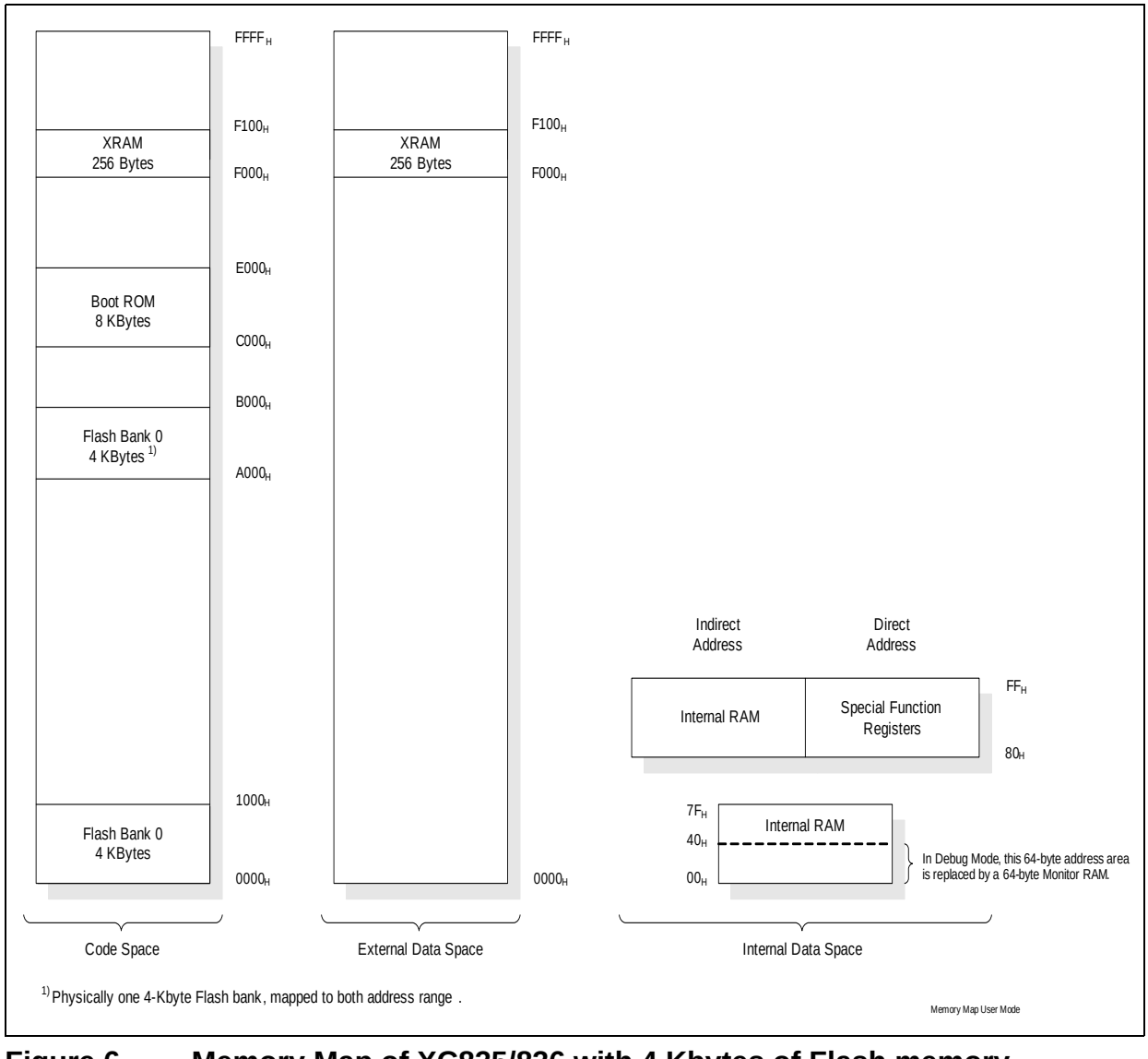


Figure 6 Memory Map of XC835/836 with 4 Kbytes of Flash memory

2.6 JTAG ID

JTAG ID register is a read-only register located inside the JTAG module, and is used to recognize the device(s) connected to the JTAG interface. Its content is shifted out when INSTRUCTION register contains the IDCODE command (opcode 04_H), and the same is also true immediately after reset.

The JTAG ID register contents for the XC835/836 Flash devices are given in **Table 4**.

Table 4 JTAG ID Summary

Device Type	Device Name	JTAG ID
Flash	XC835*-2FG	101B A083$_H$
	XC836*-2FR	
	XC836*-1FR	101B B083$_H$

Note: The asterisk (*) above denotes all possible device configurations.

3 Electrical Parameters

Chapter 3 provides the characteristics of the electrical parameters which are implementation-specific for the XC835/836.

3.1 General Parameters

The general parameters are described here to aid the users in interpreting the parameters mainly in **Section 3.2** and **Section 3.3**.

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XC835/836 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  - These parameters indicate **C**ontroller **C**haracteristics, which are distinctive features of the XC835/836 and must be regarded for a system design.
- **SR**
  - These parameters indicate **S**ystem **R**equirements, which must be provided by the microcontroller system in which the XC835/836 is designed in.

3.1.2 Absolute Maximum Rating

Maximum ratings are the extreme limits to which the XC835/836 can be subjected to without permanent damage.

Table 6 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Ambient temperature	T_A	-40	125	°C	under bias
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	150	°C	under bias
Voltage on power supply pin with respect to V_{SS}	V_{DDP}	-0.5	6	V	
Maximum current per pin for P1[3:0]	I_M	-115	115	mA	
Input current on any pin during overload condition	I_{IN}	-10	10	mA	
Absolute sum of all input currents during overload condition	$\Sigma\|I_{IN}\|$	–	50	mA	

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pin with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 8 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	5)
Maximum current per pin (excluding P1, V_{DDP} and V_{SS})	I_{MP}	SR	-15	25	mA	–
Maximum current per pin for P1[3:0]	I_{MP1A}	SR	-50	50	mA	–
Maximum current per pin for P1[5:4]	I_{MP1B}	SR	-30	50	mA	–
Maximum current into V_{DDP}	I_{MVDDP}	SR	–	130	mA	4)
Maximum current out of V_{SS}	I_{MVSS}	SR	–	130	mA	4)

1) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.

3) Over current detection is available for 5V application only.

4) Not subjected to production test, verified by design/characterization.

5) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

3.2.2 Supply Threshold Characteristics

Table 9 provides the characteristics of the supply threshold in the XC835/836.

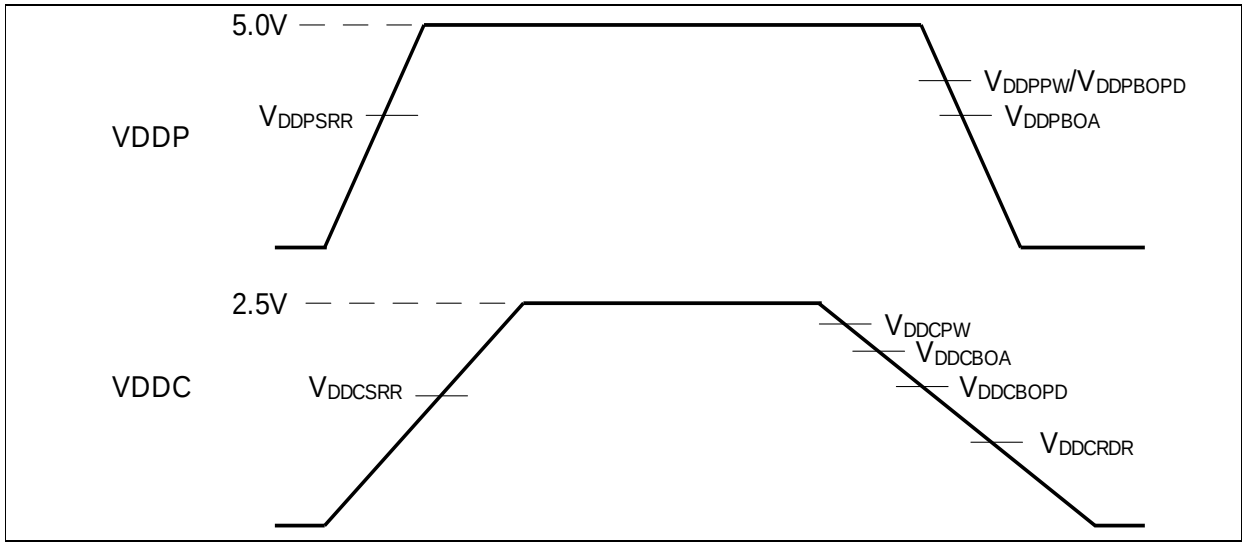


Figure 8 Supply Threshold Parameters

Table 9 Supply Threshold Parameters (Operating Conditions apply)

Parameters	Symbol		Limit Values			Unit
			Min.	Typ.	Max.	
V_{DDP} prewarning voltage[1)2)]	V_{DDPPW}	CC	3.0	3.6	4.5	V
V_{DDP} brownout voltage in active mode[2)3)]	V_{DDPBOA}	CC	2.65	2.75	2.87	V
V_{DDP} brownout voltage in all power down mode[2)3)]	$V_{DDPBOPD}$		3.0	3.6	4.5	V
V_{DDP} system reset release voltage[2)4)]	V_{DDPSRR}	CC	2.7	2.8	2.92	V
V_{DDC} prewarning voltage[2)5)]	V_{DDCPW}	CC	2.3	2.4	2.48	V
V_{DDC} brownout voltage in active mode[2)]	V_{DDCBOA}	CC	2.25	2.3	2.42	V
V_{DDC} brownout voltage in power down mode[2)]	$V_{DDCBOPD}$	CC	1.35	1.5	1.95	V
V_{DDC} system reset release voltage[2)4)]	V_{DDCSRR}	CC	2.28	2.3	2.47	V
RAM data retention voltage	V_{DDCRDR}	CC	1.1	–	–	V

1) Detection is enabled via SDCON register in active mode. It is automatically disabled in power down mode. Detection should be disabled for V_{DDP} less than maximum of V_{DDPPW}.

2) This parameter has a hysteresis of 50 mV.

3) Detection is enabled via SDCON register. Detection must be disabled for application with V_{DDP} less than the specified values.

4) V_{DDPSRR} and V_{DDCSRR} must be met before the system reset is released.

5) Detection is enabled via SDCON register in active mode. It is automatically disabled in power down mode.

3.2.3 ADC Characteristics

The values in **Table 10** are given for an analog power supply of 5.0 V. The ADC can be used with an analog power supply down to 3 V. But in this case, analog parameters may show a reduced performance. In the reduced voltage mode (2.5 V < V_{DDP} < 3 V), the ADC is not recommended to be used.

Table 10 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5 V; f_{ADCI} <= 12 MHz)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
Analog reference voltage	V_{AREF}		–	V_{DDP}	–	V	Connect internally to V_{DDP}
Analog reference ground	V_{AGND}		–	V_{SSP}	–	V	Connect internally to V_{SSP}
Alternate analog reference ground	$V_{AGNDALT}$	SR	V_{SSP} - 0.1	–	2.5[1)]	V	Connect to AN0 in differential mode, See **Figure 9**.
Internal voltage reference	V_{INTREF}	SR	1.19	1.23	1.28	V	[4)]
Analog input voltage range	V_{AIN}	SR	V_{AGND}	–	V_{AREF}	V	–
ADC clock	f_{ADCI}		8	–	16	MHz	internal analog clock
Sample time	t_S	CC	(2 + INPCR0.STC) × t_{ADCI}			µs	–
Conversion time	t_C	CC	See **Section 3.2.3.1**			µs	–
Set-up time between conversions using internal voltage reference	t_{SETUP}	SR	–	35	–	µs	[2)]

Table 10 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5 V; f_{ADCI} <= 12 MHz) (cont'd)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
Total unadjusted error	TUE[3]	CC	–	–	±1	LSB8	8-bit conversion with internal reference[4]
			–	–	+4/-2	LSB10	10-bit conversion with internal reference[4][5]
			–	–	+14/-2	LSB12	12-bit conversion using the Low Pass Filter [4]
Differential Nonlinearity	EA_{DNL}	CC	–	–	+1.5/ -1	LSB	10-bit conversion[4]
Integral Nonlinearity	EA_{INL}	CC	–	–	±1.5	LSB	10-bit conversion[4]
Offset	EA_{OFF}	CC	–	+4	–	LSB	10-bit conversion[4]
Gain	EA_{GAIN}	CC	–	-4	–	LSB	10-bit conversion[4]
Switched capacitance at an analog input	C_{AINSW}	CC	–	2	3	pF	[4][6]
Total capacitance at an analog input	C_{AINT}	CC	–	–	12	pF	[4][6]
Input resistance of an analog input	R_{AIN}	CC	–	1.5	2	kΩ	[4]

1) 1.2 V at V_{DDP} = 3.0 V.

2) Not subject to production test, verified at CPU clock ($f_{SCLK, CCLK}$) = 8 MHz, T_A = + 25 °C and V_{DDP} = 5 V.

3) TUE is tested at V_{AREF} = V_{DDP} = 5.0 V and CPU clock ($f_{SCLK, CCLK}$) = 8 MHz.

4) Not subject to production test, verified by design/characterization.

5) If a reduced positive reference voltage is used, TUE will increase. If the positive reference is reduced by a factor of K, the TUE will increased by 1/K. Example:K = 0.8, 1/K = 1.25; 1.25 X TUE = 2.5 LSB10.

6) The sampling capacity of the conversion C-Network is pre-charged to V_{AREF}/2 before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than V_{AREF}/2.

3.2.4 Flash Memory Parameters

The XC835/836 is delivered with all Flash sectors erased (read all zeros).

The data retention time of the XC835/836's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: Flash memory parameters are not subject to production test but verified by design and/or characterization.

Table 12 Flash Timing Parameters (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Read access time (per byte)	t_{ACC}	CC	–	125	–	ns	
Programming time (per wordline)	t_{PR}	CC	–	2.2	–	ms	
Erase time (one or more sectors)	t_{ER}	CC	–	120	–	ms	
Flash wait states	$N_{WSFLASH}$	CC	0				CPU clock = 8 MHz
			1				CPU clock = 24 MHz

Table 13 Flash Data Retention and Endurance (Operating Conditions apply)

Retention	Endurance[1)]	Size	Remarks
20 years	1,000 cycles	up to 8 Kbytes	
5 years	10,000 cycles	1 Kbyte	
2 years	70,000 cycles	512 bytes	
2 years	100,000 cycles	128 bytes	

1) One cycle refers to the programming of all wordlines in a sector and erasing of sector. The Flash endurance data specified in **Table 13** is valid only if the following conditions are fulfilled:
- the maximum number of erase cycles per Flash sector must not exceed 100,000 cycles.
- the maximum number of erase cycles per Flash bank must not exceed 300,000 cycles.
- the maximum number of program cycles per Flash bank must not exceed 2,500,000 cycles.

7) Timer 2 active current is measured with: module enabled, timer running in 8 MHz
8) MDU active current is measured with: module enabled, division operation was performed.
9) CORDIC active mode is measured with: module enabled, circular mode was selected for the calculation.
10) LEDTSCU active curent is measured with: module enabled, counter running in 8 MHz.
11) IIC active current is measured with: module enabled, performing a master transmit with the master clock running at 400 KHz.

3.3.2 Output Rise/Fall Times

Table 18 provides the characteristics of the output rise/fall times in the XC835/836.

Table 18 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Rise/fall times on High Current Pad Type A[1)2)]	t_{HCPR}, t_{HCPF}	–	15	ns	20 pF @ Fast edge (5 V) [3)].
		–	150	ns	20 pF @ Slow Edge (5 V)[3)].
		–	25	ns	20 pF @ Fast edge (3.3 V)[4)].
		–	300	ns	20 pF @ Slow edge (3.3 V)[4)].
Rise/fall times on High Current Pad Type B[1)2)]	t_R, t_F	–	10	ns	20 pF[3)4)] (5 V & 3.3 V).
Rise/fall times on Standard Pad[1)2)]	t_R, t_F	–	10	ns	20 pF[3)4)] (5 V & 3.3 V).

1) Rise/Fall time parameters are taken with 10% - 90% of supply.

2) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.

3) Additional rise/fall time valid for C_L = 20 pF - C_L = 100 pF @ 0.125 ns/pF at 5 V supply voltage.

4) Additional rise/fall time valid for C_L = 20 pF - C_L = 100 pF.@ 0.225 ns/pF at 3.3 V supply voltage.

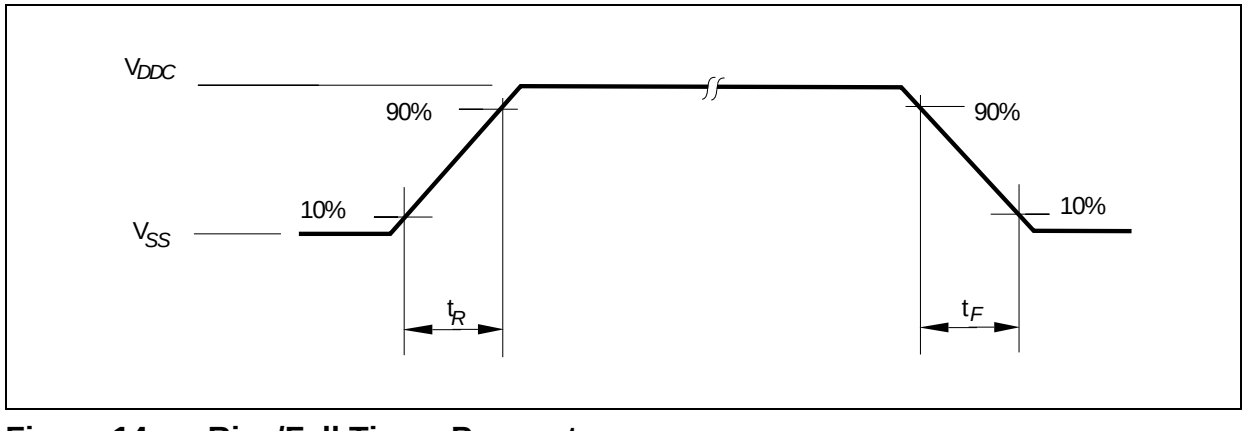


Figure 14 Rise/Fall Times Parameters

Table 21 provides the characteristics of the 75 kHz oscillator in the XC835/836.

Table 21 75 kHz Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	-1%	75	+1%	KHz	under nominal conditions[1] after trimming
Long term frequency deviation	Δf_{LT}	CC	-4.5	–	4.5	%	with respect to f_{NOM}, over lifetime and temperature (-40 °C to 125 °C)
Short term frequency deviation	Δf_{ST}	CC	-1.5	–	1.5	%	with respect to f_{NOM}, over V_{DDC}

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

3.3.5 SSC Timing

3.3.5.1 SSC Master Mode Timing

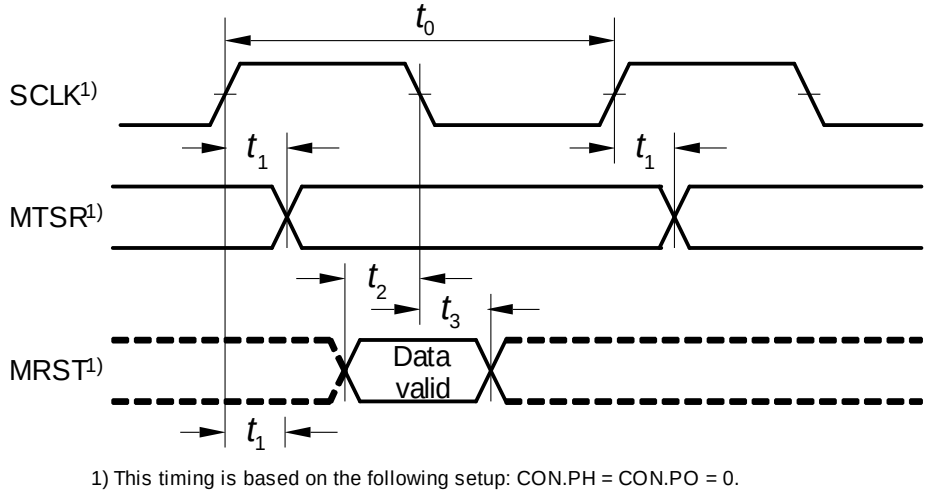
Table 22 provides the SSC master mode timing in the XC835/836.

Table 22 SSC Master Mode Timing[1] (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
SCLK clock period	t_0	CC	2 * T_{SSC}[2]	–	ns
MTSR delay from SCLK	t_1	CC	0	3	ns
MRST set-up to SCLK	t_2	SR	32	–	ns
MRST hold from SCLK	t_3	SR	0	–	ns

1) Not subject to production test, verified by design/characterisation.

2) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When f_{CPU} = 24 MHz, t_0 = 83.3 ns. T_{CPU} is the CPU clock period.



1) This timing is based on the following setup: CON.PH = CON.PO = 0.

SSC_Tmg1

Figure 15 SSC Master Mode Timing

4 Package and Quality Declaration

Chapter 4 provides the information of the XC835/836 package and reliability section.

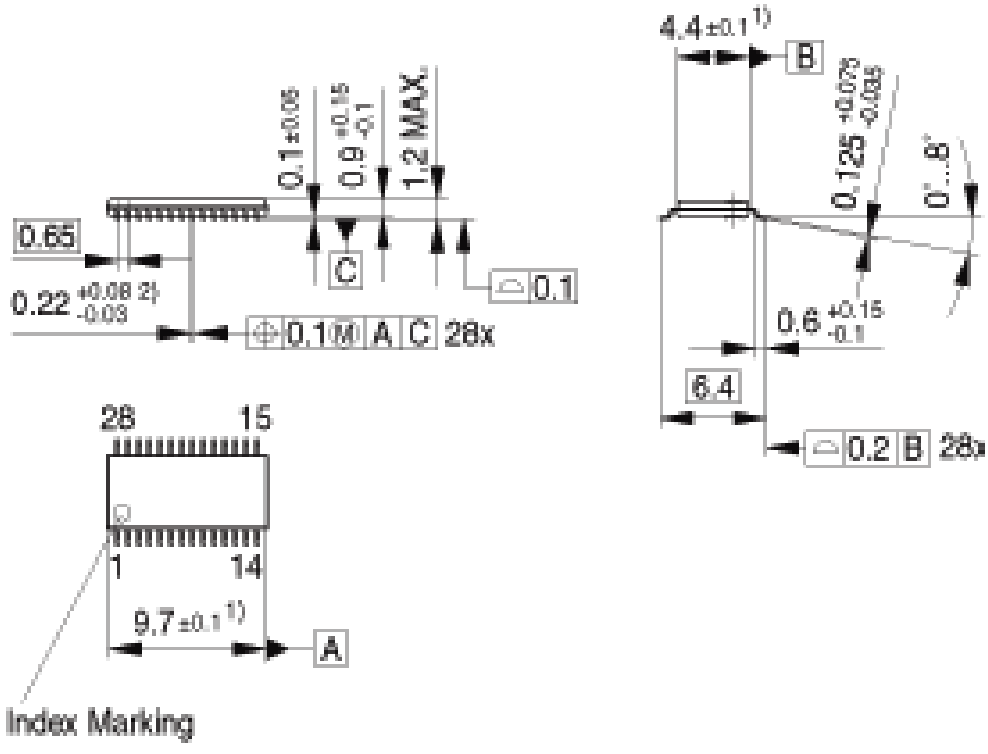
4.1 Package Parameters

Table 24 provides the thermal characteristics of the packages used in XC835 and XC836 respectively.

Table 24 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Thermal resistance junction case[1)]	R_{TJC} CC	-	30.8	K/W	PG-DSO-24-1
		-	27.0	K/W	PG-TSSOP-28-1
		-	20.2	K/W	PG-TSSOP-28-12
Thermal resistance junction lead[1)]	R_{TJL} CC	-	30.5	K/W	PG-DSO-24-1
		-	195.3	K/W	PG-TSSOP-28-1
		-	41	K/W	PG-TSSOP-28-12

1) The thermal resistances between the case and the ambient (R_{TCA}) , the lead and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case (R_{TJC}), the junction and the lead (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J=T_A+R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances, by
a) simply adding only the two thermal resistances (junction lead and lead ambient), or
b) by taking all four resistances into account, depending on the precision needed.



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

Figure 19 PG-TSSOP-28-12 Package Outline