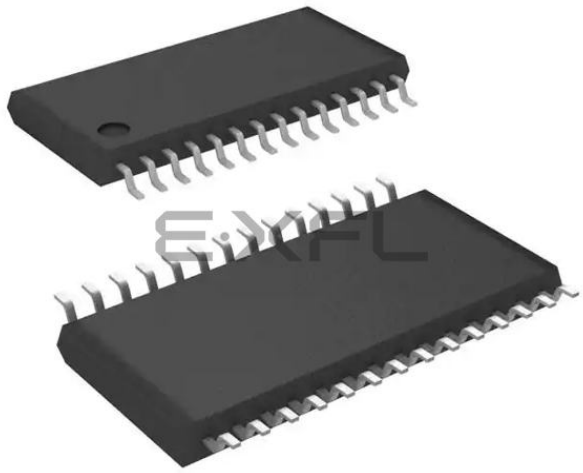

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-28-1
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc836mt2fraabkxuma1

1 Summary of Features

The XC835/836 has the following features:

- High-performance XC800 Core
  - compatible with standard 8051 processor
  - two clocks per machine cycle architecture (for memory access without wait state)
  - two data pointers
- On-chip memory
  - 8 Kbytes of Boot ROM, Library ROM and User routines
  - 256 bytes of RAM
  - 256 bytes of XRAM
  - 4/8 Kbytes of Flash (includes memory protection strategy)
- I/O port supply at 2.5 V - 5.5 V and core logic supply at 2.5 V (generated by embedded voltage regulator)

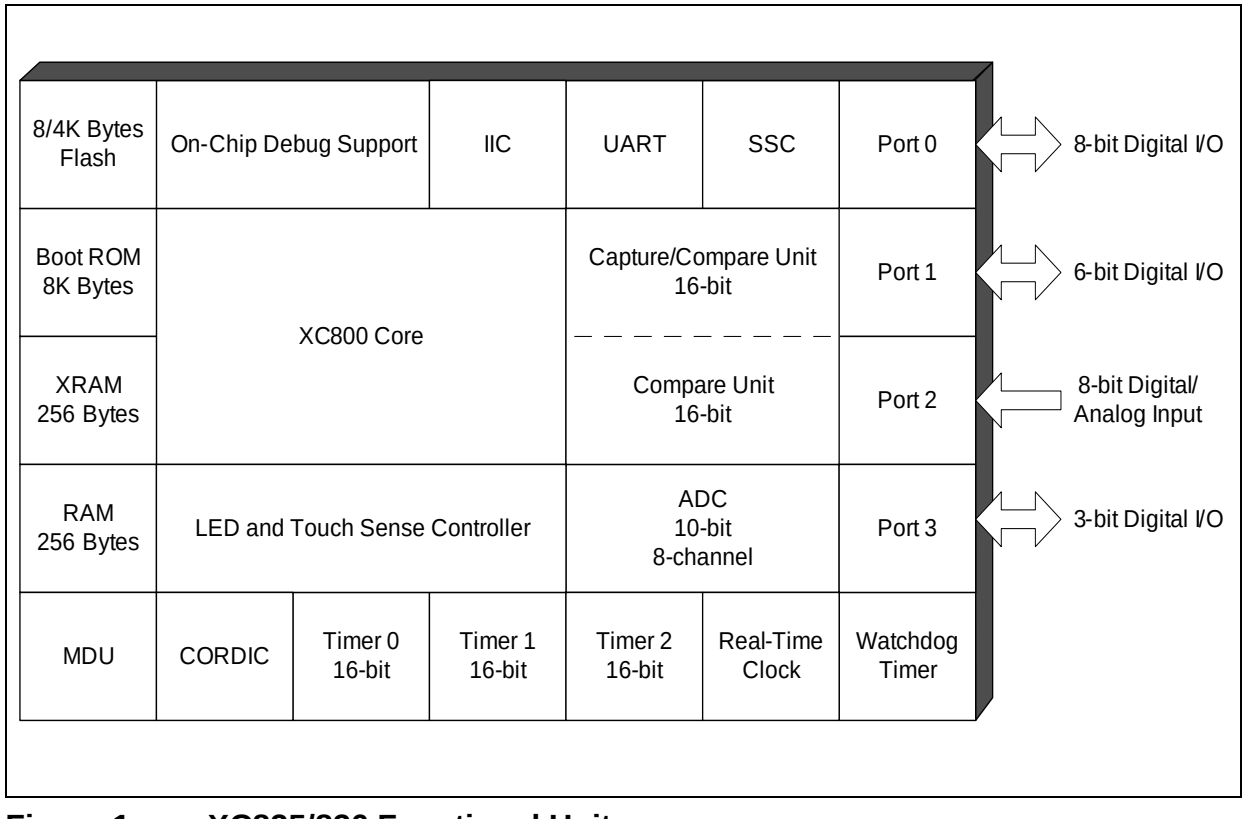


Figure 1 XC835/836 Functional Units

- Power-on reset generation
- Brownout detection for IO supply and core logic supply
- 48 MHz on-chip OSC for clock generation
  - Loss-of-Clock detection

(more features on next page)

2.2 Logic Symbol

The logic symbol of the XC835/836 is shown in **Figure 3**.

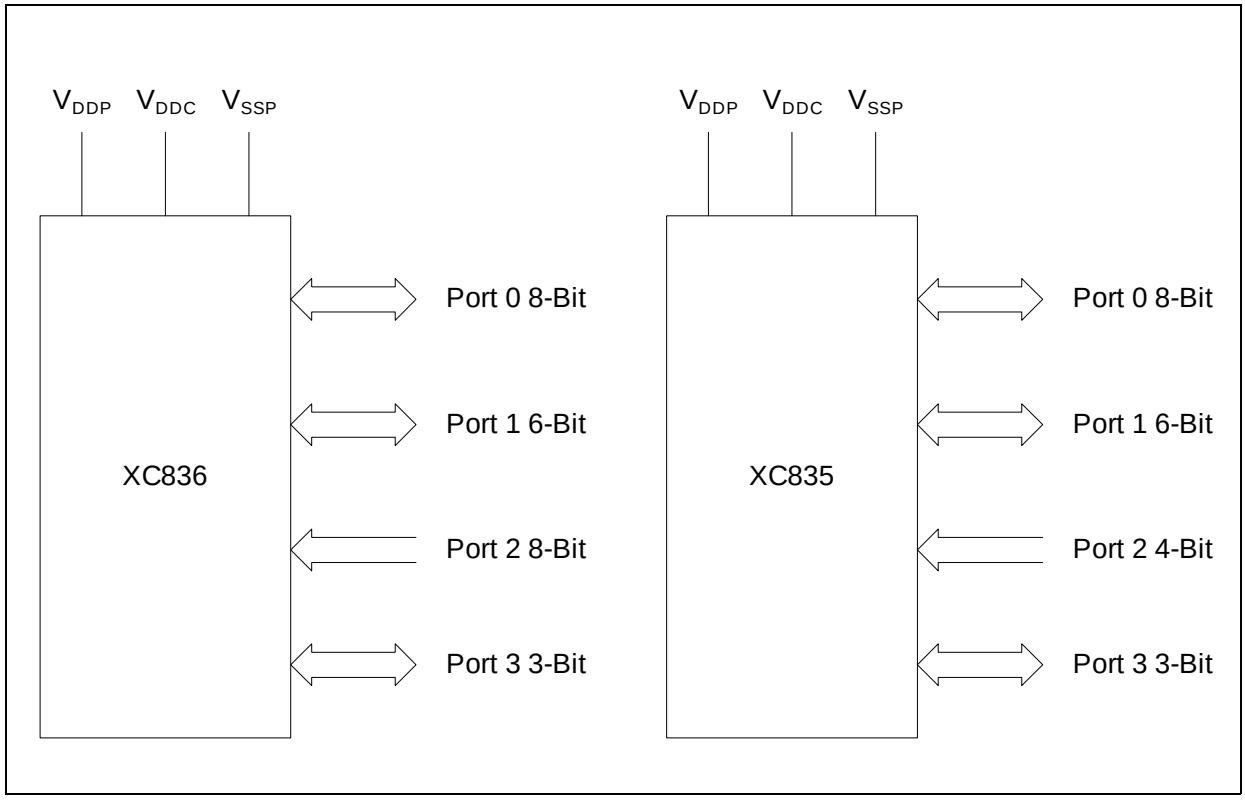


Figure 3 XC835/836 Logic Symbol

2.4 Pin Definitions and Functions

The functions and default states of the XC835/836 external pins are provided in **Table 3**.

Table 3 Pin Definitions and Functions for XC835/836

Symbol	Pin Number TSSOP28/ DS024	Type	Reset State	Function	
P0		I/O		**Port 0** Port 0 is a bidirectional general purpose I/O port. It can be used as alternate functions for LEDTSCU, Timer 0, 1 and 2, SSC, CCU6, IIC, SPD and UART.	
P0.0	21/19		Hi-Z	T2_0	Timer 2 Input
				T13HR_1	CCU6 Timer 13 Hardware Run Input
				MTSR_2	SSC Master Transmit Output/ Slave Receive Input
				MRST_3	SSC Master Receive Input
				T12HR_0	CCU6 Timer 12 Hardware Run Input
				CCPOS0_0	CCU6 Hall Input 0
				TSIN0	Touch-sense Input 0
				LINE0	LED Line 0
				COUT61_1	Output of Capture/Compare Channel 1

Table 3 Pin Definitions and Functions for XC835/836 (cont'd)

Symbol	Pin Number TSSOP28/ DS024	Type	Reset State	Function	
P0.1	22/20		Hi-Z	T0_0	Timer 0 Input
				CC61_1	Input/Output of Capture/Compare channel 1
				MTSR_3	SSC Slave Receive Input
				MRST_2	SSC Master Receive Input/ Slave Transmit Output
				T13HR_0	CCU6 Timer 13 Hardware Run Input
				CCPOS1_0	CCU6 Hall Input 1
				TSIN1	Touch-sense Input 1
				LINE1	LED Line 1
P0.2	23/21		Hi-Z	T1_0	Timer 1 Input
				CC62_1	Input/Output of Capture/Compare channel 2
				SCL_1	IIC Clock Line
				CCPOS2_0	CCU6 Hall Input 2
				TSIN2	Touch-sense Input 2
				LINE2	LED Line 2
P0.3	24/22		Hi-Z	CC60_1	Input/Output of Capture/Compare channel 0
				SDA_1	IIC Data Line
				$\overline{\text{CTRAP\_0}}$	CCU6 Trap Input
				TSIN3	Touch-sense Input 3
				LINE3	LED Line 3

Table 3 Pin Definitions and Functions for XC835/836 (cont'd)

Symbol	Pin Number TSSOP28/ DS024	Type	Reset State	Function	
P0.4	11/9		PD	T2EX_1	Timer 2 External Trigger Input
				SCK_0	SSC Clock Input/Output
				SCL_0	IIC Clock Line
				$\overline{\text{CTRAP}}$_1	CCU6 Trap Input
				EXINT1_0	External Interrupt Input 1
				TSIN4	Touch-sense Input 4
				LINE4	LED Line 4
				EXF2_0	Timer 2 Overflow Flag
				COL0_1	LED Column 0
				COL3_2	LED Column 3
				COLA_4	LED Column A
P0.5	10/8		Hi-Z	RXD_0	UART Receive Input
				MTSR_0	SSC Master Transmit Output/ Slave Receive Input
				MRST_1	SSC Master Receive Input
				EXINT0_0	External Interrupt Input 0
				TSIN5	Touch-sense Input 5
				LINE5	LED Line 5
				COUT62_1	Output of Capture/Compare Channel 2
				TXD_4	UART Transmit Output
				COL1_1	LED Column 1
				EXF2_3	Timer 2 Overflow Flag

Table 3 Pin Definitions and Functions for XC835/836 (cont'd)

Symbol	Pin Number TSSOP28/ DS024	Type	Reset State	Function	
P2.2	6/4		Hi-Z	CCPOS2_1	CCU6 Hall Input 2
				T12HR_3	CCU6 Timer 12 Hardware Run Input
				T13HR_3	CCU6 Timer 13 Hardware Run Input
				SCK_3	SSC Clock Input/Output
				T1_1	Timer 1 Input
				EXINT2_0	External Interrupt Input 2
				AN2	Analog Input 2 / Out of range comparator channel 2
P2.3	5/3		Hi-Z	CCPOS0_2	CCU6 Hall Input 0
				$\overline{\text{CTRAP}}$_2	CCU6 Trap Input
				T2_2	Timer 2 Input
				EXINT3	External Interrupt Input 3
				AN3	Analog Input 3 / Out of range comparator channel 3
P2.4	4/-		Hi-Z	T12HR_5	CCU6 Timer 12 Hardware Run Input
				T13HR_5	CCU6 Timer 13 Hardware Run Input
				T2_3	Timer 2 Input
				AN4	Analog Input 4 / Out of range comparator channel 4
P2.5	3/-		Hi-Z	T12HR_7	CCU6 Timer 12 Hardware Run Input
				T13HR_7	CCU6 Timer 13 Hardware Run Input
				AN5	Analog Input 5 / Out of range comparator channel 5

Table 3 Pin Definitions and Functions for XC835/836 (cont'd)

Symbol	Pin Number TSSOP28/ DS024	Type	Reset State	Function	
P3.1	25/23		PU	RXD_4	UART Receive Input
				RTCCLK	RTC External Clock Input
				MTSR_4	SSC Master Transmit Output/ Slave Receive Input
				MRST_4	SSC Master Receive Input
				EXINT0_5	External Interrupt Input 0
				COLA_0	LED Column A
				XTAL3	32.768 kHz External oscillator Input
				EXF2_1	Timer 2 Overflow Flag
P3.2	27/1		PU	SPD_0	SPD Input/Output
				RXD_3	UART Receive Input/ UART BSL Receive Input
				SDA_2	IIC Data Line
				MTSR_5	SSC Slave Receive Input
				MRST_5	SSC Master Receive Input/ Slave Transmit Output
				EXINT0_6	External Interrupt Input 0
				T2EX_7	Timer 2 External Trigger Input
				TXD_3	UART Transmit Output/ 1-wire UART BSL Transmit Output
V_{DDP}	12/10	–	–	I/O Port Supply (2.5 V - 5.5 V)	
V_{DDC}	18/16	–	–	Core Supply Monitor (2.5 V)	
V_{SSP}/ V_{SSC}	17/15	–	–	I/O Port Ground/ Core Supply Ground	

2.7 Chip Identification Number

The XC835/836 identity (ID) register is located at Page 1 of address $B3_H$. The value of ID register is 59_H. However, for easy identification of product variants, the Chip Identification Number, which is an unique number assigned to each product variant, is available. The differentiation is based on the product and variant type information.

Two methods are provided to read a device's Chip Identification number:

- In-application subroutine, GET_CHIP_INFO
- Boot-loader (BSL) mode A

Table 5 lists the Chip Identification numbers of XC835/836 device variants.

Table 5 Chip Identification Number

Product Variant	Chip Identification Number
XC835MT-2FG	59100001_H
XC836-2FR	59100060_H
XC836T-2FR	59100040_H
XC836M-2FR	59100020_H
XC836M-1FR	59100120_H
XC836MT-2FR	59100000_H
XC836MT-1FR	59100100_H

3.1.2 Absolute Maximum Rating

Maximum ratings are the extreme limits to which the XC835/836 can be subjected to without permanent damage.

Table 6 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Ambient temperature	T_A	-40	125	°C	under bias
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	150	°C	under bias
Voltage on power supply pin with respect to V_{SS}	V_{DDP}	-0.5	6	V	
Maximum current per pin for P1[3:0]	I_M	-115	115	mA	
Input current on any pin during overload condition	I_{IN}	-10	10	mA	
Absolute sum of all input currents during overload condition	$\Sigma\|I_{IN}\|$	–	50	mA	

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pin with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 8 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input low voltage on port pins	V_{ILP}	SR	–	0.3 × V_{DDP}	V	CMOS Mode (5 & 3.3 V)
Input high voltage on port pins	V_{IHP}	SR	0.7 × V_{DDP}	–	V	CMOS Mode (5 V & 3.3 V)
Input Hysteresis[1]	HYS	CC	0.08 × V_{DDP}	–	V	CMOS Mode (5 V)
			0.03 × V_{DDP}	–	V	CMOS Mode (3.3 V)
			0.01 × V_{DDP}	–	V	CMOS Mode (2.5 V)
Pull-up current	I_{PUP}	SR	–	-20	µA	$V_{IH,min}$ (5 V)
			-150	–	µA	$V_{IL,max}$ (5 V)
			–	-5	µA	$V_{IH,min}$ (3.3 V)
			-100	–	µA	$V_{IL,max}$ (3.3 V)
Pull-down current	I_{PDP}	SR	–	20	µA	$V_{IL,max}$ (5 V)
			150	–	µA	$V_{IH,min}$ (5 V)
			–	5	µA	$V_{IL,max}$ (3.3 V)
			100	–	µA	$V_{IH,min}$ (3.3 V)
Input leakage current on port pins[2] (all except P1)	I_{OZP}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 125$ °C
Input leakage current on P1[3:0][2]	I_{OZP1}	CC	-3	3	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 125$ °C
Input leakage current on P1[5:4][2]	I_{OZP2}	CC	-2	2	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 125$ °C
Overcurrent threshold per pin for P1[3:0][3]	$\|I_{OCP1}\|$	SR	60	115	mA	V_{DDP} = 5 V
Overload current on any pin	I_{OVP}	SR	-5	5	mA	[4]
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	SR	–	25	mA	[4]

3.2.2 Supply Threshold Characteristics

Table 9 provides the characteristics of the supply threshold in the XC835/836.

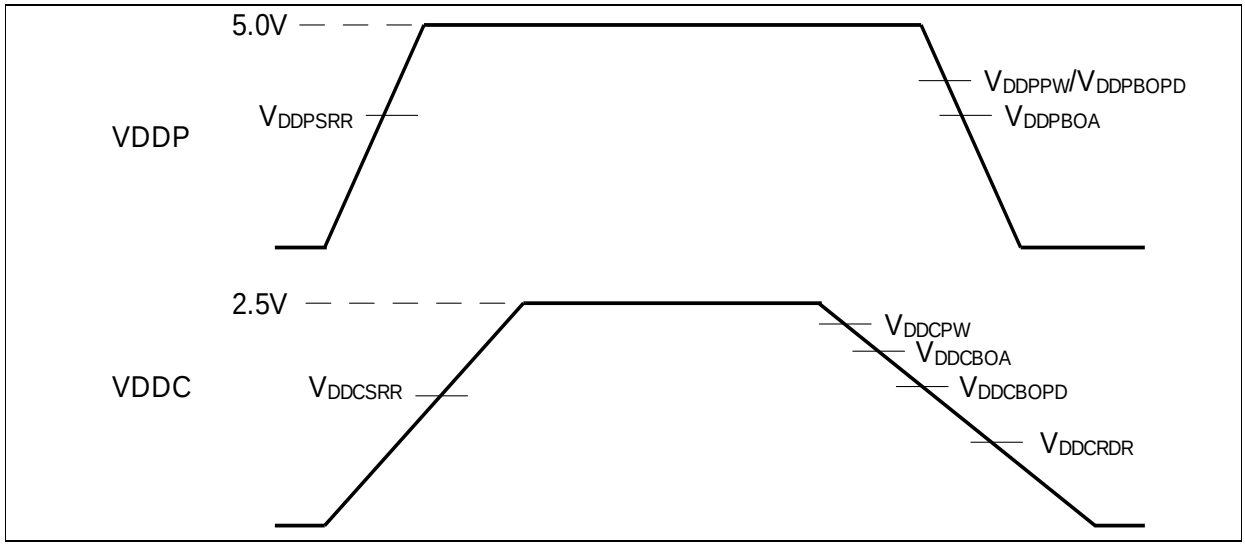


Figure 8 Supply Threshold Parameters

Table 9 Supply Threshold Parameters (Operating Conditions apply)

Parameters	Symbol		Limit Values			Unit
			Min.	Typ.	Max.	
V_{DDP} prewarning voltage[1)2)]	V_{DDPPW}	CC	3.0	3.6	4.5	V
V_{DDP} brownout voltage in active mode[2)3)]	V_{DDPBOA}	CC	2.65	2.75	2.87	V
V_{DDP} brownout voltage in all power down mode[2)3)]	$V_{DDPBOPD}$		3.0	3.6	4.5	V
V_{DDP} system reset release voltage[2)4)]	V_{DDPSRR}	CC	2.7	2.8	2.92	V
V_{DDC} prewarning voltage[2)5)]	V_{DDCPW}	CC	2.3	2.4	2.48	V
V_{DDC} brownout voltage in active mode[2)]	V_{DDCBOA}	CC	2.25	2.3	2.42	V
V_{DDC} brownout voltage in power down mode[2)]	$V_{DDCBOPD}$	CC	1.35	1.5	1.95	V
V_{DDC} system reset release voltage[2)4)]	V_{DDCSRR}	CC	2.28	2.3	2.47	V
RAM data retention voltage	V_{DDCRDR}	CC	1.1	–	–	V

1) Detection is enabled via SDCON register in active mode. It is automatically disabled in power down mode. Detection should be disabled for V_{DDP} less than maximum of V_{DDPPW}.

2) This parameter has a hysteresis of 50 mV.

3) Detection is enabled via SDCON register. Detection must be disabled for application with V_{DDP} less than the specified values.

4) V_{DDPSRR} and V_{DDCSRR} must be met before the system reset is released.

5) Detection is enabled via SDCON register in active mode. It is automatically disabled in power down mode.

3.2.3 ADC Characteristics

The values in **Table 10** are given for an analog power supply of 5.0 V. The ADC can be used with an analog power supply down to 3 V. But in this case, analog parameters may show a reduced performance. In the reduced voltage mode (2.5 V < V_{DDP} < 3 V), the ADC is not recommended to be used.

Table 10 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5 V; f_{ADCI} <= 12 MHz)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
Analog reference voltage	V_{AREF}		–	V_{DDP}	–	V	Connect internally to V_{DDP}
Analog reference ground	V_{AGND}		–	V_{SSP}	–	V	Connect internally to V_{SSP}
Alternate analog reference ground	$V_{AGNDALT}$	SR	V_{SSP} - 0.1	–	2.5[1)]	V	Connect to AN0 in differential mode, See **Figure 9**.
Internal voltage reference	V_{INTREF}	SR	1.19	1.23	1.28	V	[4)]
Analog input voltage range	V_{AIN}	SR	V_{AGND}	–	V_{AREF}	V	–
ADC clock	f_{ADCI}		8	–	16	MHz	internal analog clock
Sample time	t_S	CC	(2 + INPCR0.STC) × t_{ADCI}			µs	–
Conversion time	t_C	CC	See **Section 3.2.3.1**			µs	–
Set-up time between conversions using internal voltage reference	t_{SETUP}	SR	–	35	–	µs	[2)]

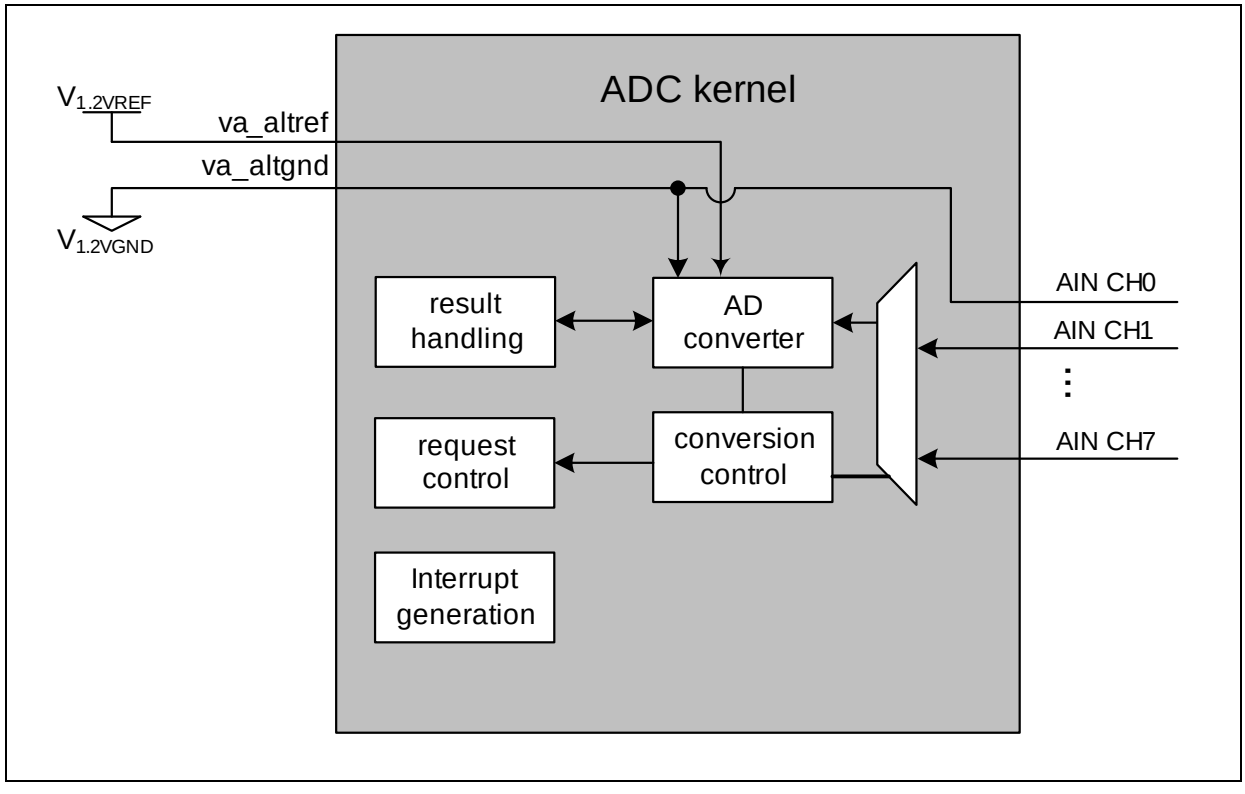


Figure 9 Differential like measurement with internal 1.2V voltage reference, and CH0 gnd.

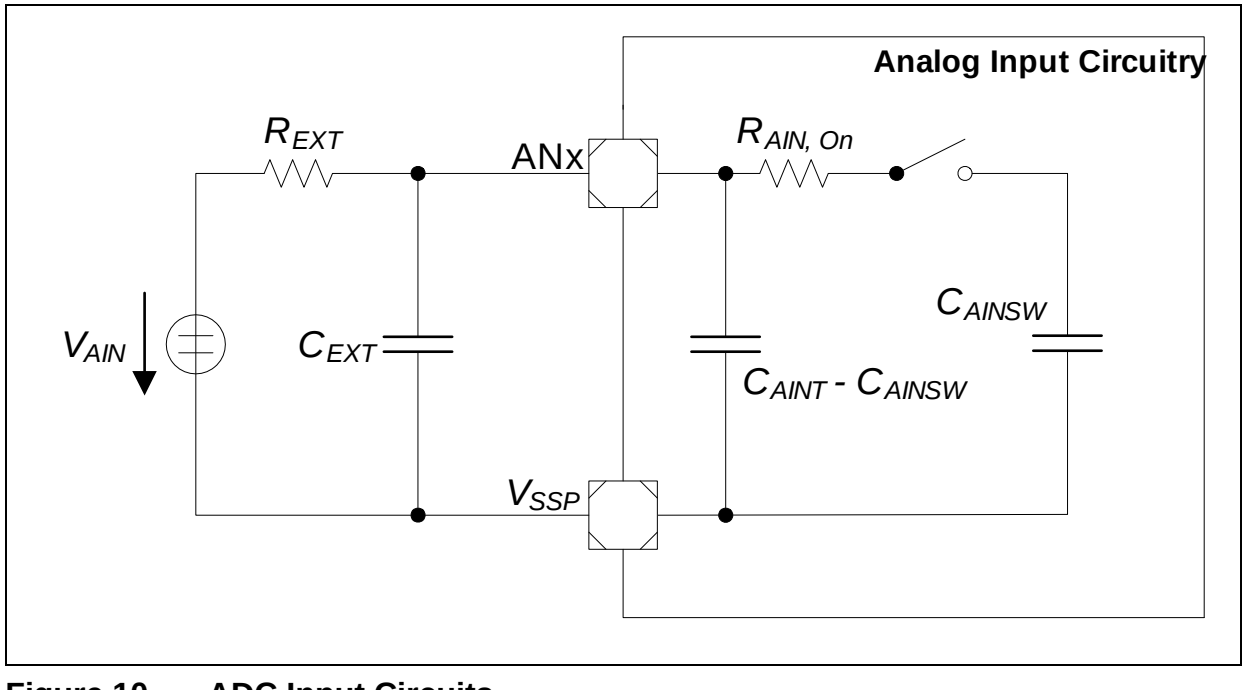


Figure 10 ADC Input Circuits

3.2.3.1 ADC Conversion Timing

Conversion time, $t_C = t_{ADC} \times (1 + r \times (3 + n + STC))$, where

- r = CTC + 3,
- CTC = Conversion Time Control (GLOBCTR.CTC),
- STC = Sample Time Control (INPCR0.STC),
- n = 8 or 10 (for 8-bit and 10-bit conversion respectively),
- $t_{ADC} = 1 / f_{ADC}$

3.2.3.2 Out of Range Comparator Characteristics

Table 11 below shows the Out of Range Comparator characteristics.

Table 11 Out of Range Comparator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
DC Switching Level	$V_{SenseDC}$	SR	60	125	270	mV	Above V_{DDP}
DC Hysteresis	$V_{SenseHys}$	CC	30	–	–	mV	1)
Pulse Width	$t_{SensePW}$	SR	300	–	–	ns	ANx > V_{DDP} 1)
Switching Delay	$t_{SenseSD}$	CC	–	–	400	ns	ANx >= V_{DDP} + 350 mV 1)
Pulse Switching Level	$t_{SensePSL}$	SR	–	250	–	mV	@ 300 nsec 1)
		SR	–	60	–	mV	@ 800 usec 1)

1) Not subject to production test, verified by design/characterization.

3.2.4 Flash Memory Parameters

The XC835/836 is delivered with all Flash sectors erased (read all zeros).

The data retention time of the XC835/836's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: Flash memory parameters are not subject to production test but verified by design and/or characterization.

Table 12 Flash Timing Parameters (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Read access time (per byte)	t_{ACC}	CC	–	125	–	ns	
Programming time (per wordline)	t_{PR}	CC	–	2.2	–	ms	
Erase time (one or more sectors)	t_{ER}	CC	–	120	–	ms	
Flash wait states	$N_{WSFLASH}$	CC	0				CPU clock = 8 MHz
			1				CPU clock = 24 MHz

Table 13 Flash Data Retention and Endurance (Operating Conditions apply)

Retention	Endurance[1)]	Size	Remarks
20 years	1,000 cycles	up to 8 Kbytes	
5 years	10,000 cycles	1 Kbyte	
2 years	70,000 cycles	512 bytes	
2 years	100,000 cycles	128 bytes	

1) One cycle refers to the programming of all wordlines in a sector and erasing of sector. The Flash endurance data specified in **Table 13** is valid only if the following conditions are fulfilled:
- the maximum number of erase cycles per Flash sector must not exceed 100,000 cycles.
- the maximum number of erase cycles per Flash bank must not exceed 300,000 cycles.
- the maximum number of program cycles per Flash bank must not exceed 2,500,000 cycles.

Table 14 Emulated Flash Data Retention and Endurance based on EEPROM Emulation ROM Library (Operating Conditions apply)

Retention	Endurance[1)]	Emulation Size	Remarks
2 years	1,600,000 cycles	31 bytes	
2 years	1,400,000 cycles	62 bytes	
2 years	1,200,000 cycles	93 bytes	
2 years	1,000,000 cycles	124 bytes	

1) These values show the maximum endurance. Maximum endurance is the maximum possible unique data write if each data update is only 31 bytes. Minimum endurance cycle is the maximum possible unique data write if each data update is the same as the emulation size. The minimum endurance cycle can be calculated using the formulae [(max. endurance)*(31)/(emulation size)].

3.3.4 On-Chip Oscillator Characteristics

Table 20 provides the characteristics of the 48 MHz oscillator in the XC835/836.

Table 20 48 MHz Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	-0.5 %	48	+0.5%	MHz	under nominal conditions[1] after trimming
Long term frequency deviation	Δf_{LT}	CC	-2.0	–	3.0	%	with respect to f_{NOM}, over lifetime and temperature (0 °C to 85 °C)
			-4.5	–	4.5	%	with respect to f_{NOM}, over lifetime and temperature (-40 °C to 125 °C)
Short term frequency deviation (over V_{DDC})	Δf_{ST}	CC	-1	–	1	%	with respect to f_{NOM}, within one LIN message (< 10 ms … 100 ms)

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

3.3.5 SSC Timing

3.3.5.1 SSC Master Mode Timing

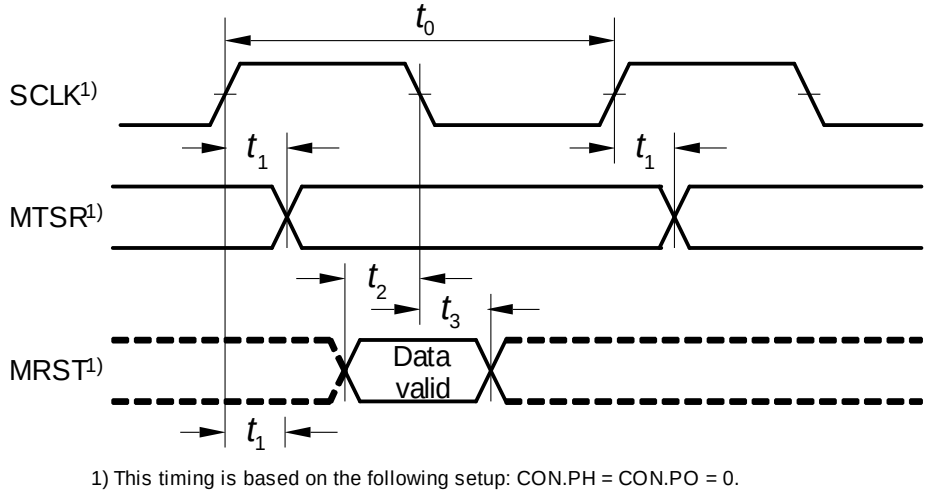
Table 22 provides the SSC master mode timing in the XC835/836.

Table 22 SSC Master Mode Timing[1] (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
SCLK clock period	t_0	CC	2 * T_{SSC}[2]	–	ns
MTSR delay from SCLK	t_1	CC	0	3	ns
MRST set-up to SCLK	t_2	SR	32	–	ns
MRST hold from SCLK	t_3	SR	0	–	ns

1) Not subject to production test, verified by design/characterisation.

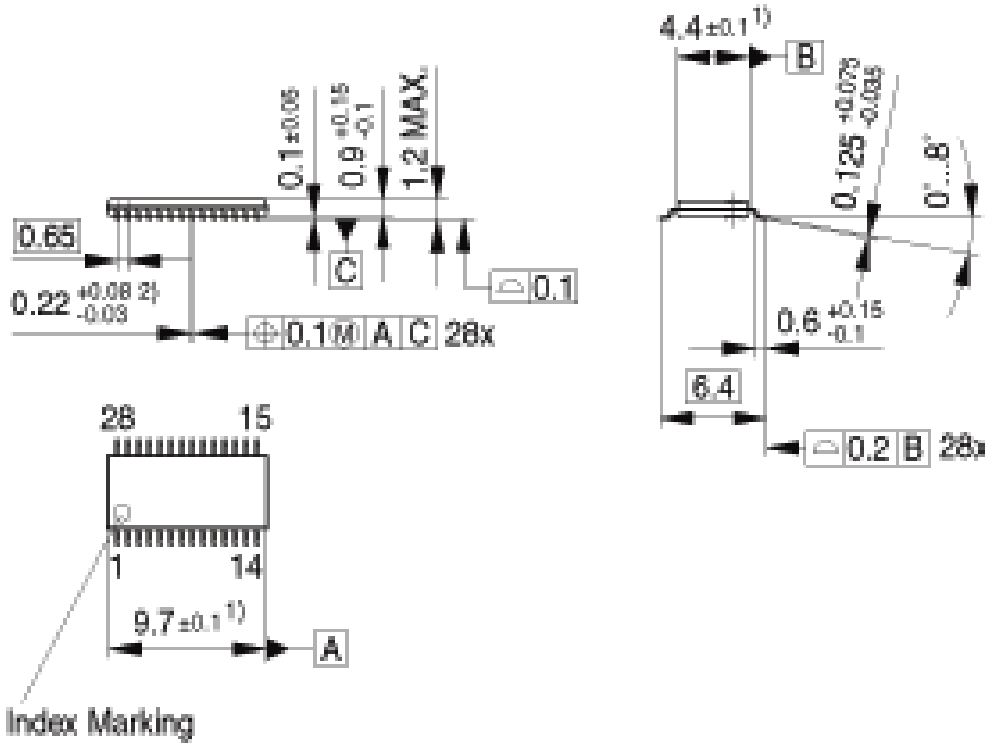
2) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When f_{CPU} = 24 MHz, t_0 = 83.3 ns. T_{CPU} is the CPU clock period.



1) This timing is based on the following setup: CON.PH = CON.PO = 0.

SSC_Tmg1

Figure 15 SSC Master Mode Timing



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

Figure 19 PG-TSSOP-28-12 Package Outline

4.3 Quality Declaration

Table 25 shows the characteristics of the quality parameters in the XC835/836.

Table 25 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Operation Lifetime when the device is used at the three stated T_J [1]	t_{OP1}	-	1500	hours	T_J = 150°C
		-	15000	hours	T_J = 110°C
		-	1500	hours	T_J = -40°C
Operation Lifetime when the device is used at the stated T_J [1]	t_{OP2}	-	131400	hours	T_J = 27°C
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	-	2000	V	Conforming to EIA/JESD22-A114-B [2]
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM}	-	500	V	Conforming to JESD22-C101-C [2]

1) This lifetime refers only to the time when device is powered-on.

2) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.