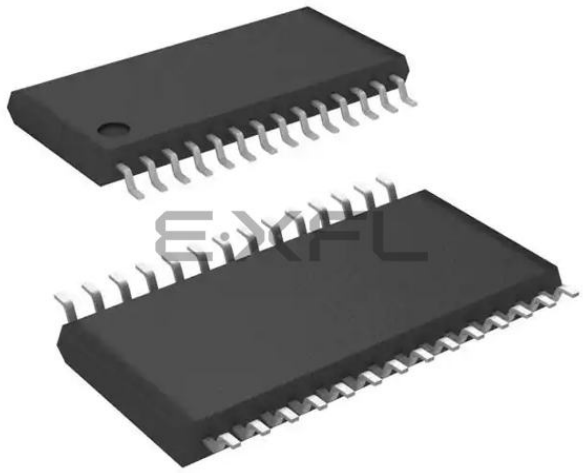
Infineon Technologies - XC836MT2FRIABFXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-28-1
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc836mt2friabfxuma1

Table of Contents

1 Summary of Features

The XC835/836 has the following features:

- High-performance XC800 Core
  - compatible with standard 8051 processor
  - two clocks per machine cycle architecture (for memory access without wait state)
  - two data pointers
- On-chip memory
  - 8 Kbytes of Boot ROM, Library ROM and User routines
  - 256 bytes of RAM
  - 256 bytes of XRAM
  - 4/8 Kbytes of Flash (includes memory protection strategy)
- I/O port supply at 2.5 V - 5.5 V and core logic supply at 2.5 V (generated by embedded voltage regulator)

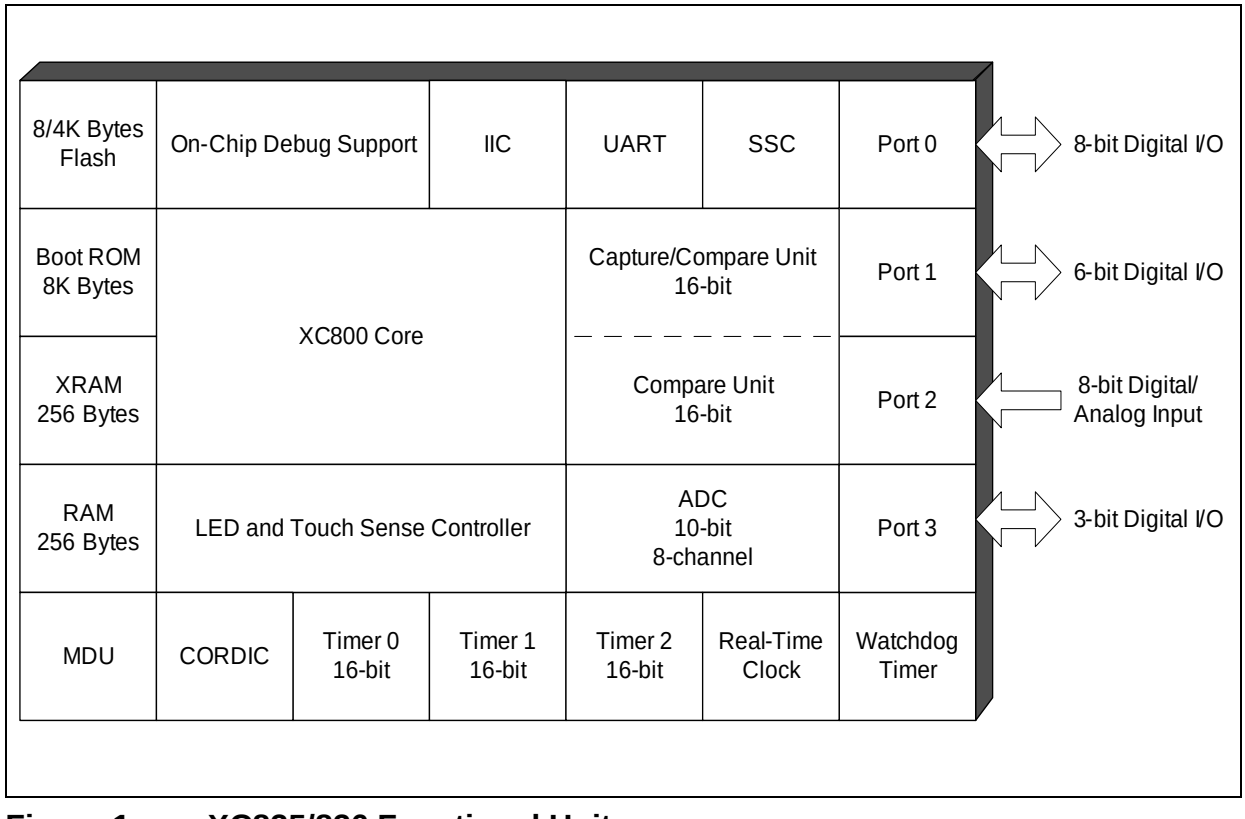


Figure 1 XC835/836 Functional Units

- Power-on reset generation
- Brownout detection for IO supply and core logic supply
- 48 MHz on-chip OSC for clock generation
  - Loss-of-Clock detection

(more features on next page)

Features: (continued)

- Power saving modes
  - idle mode
  - power-down mode with wake-up capability via real-time clock event
  - clock gating control to each peripheral
- Programmable 16-bit Watchdog Timer (WDT) running on independent oscillator with programmable window feature for refresh operation and warning prior to overflow
- Three general purpose I/O ports
  - 4 high current I/O
  - 2 high sink I/O
  - Up to 25 pins as digital I/O
  - Up to 8 pins as digital/analog input
- Up to 8 channels, 10-bit A/D Converter
  - support up to 7 differential input channel
  - results filtering by data reduction or digital low-pass filter, for up to 13-bit results
- Up to 8 channels, Out of range comparator
- Three 16-bit timers
  - Timer 0 and Timer 1 (T0 and T1)
  - Timer 2 (T2)
- Real-time clock with 32.768 kHz crystal pad
- 16-bit Vector Computer for Field-Oriented Control (FOC)
  - Multiplication/Division Unit (MDU) for arithmetic calculation
  - CORDIC Unit for trigonometric calculation
- Capture and Compare unit for PWM signal generation (CCU6)
- A full-duplex or half-duplex serial interface (UART)
- Synchronous serial channel (SSC)
- Inter-IC (IIC) serial interface
- LED and Touch-sense Controller (LEDTSCU)
- Software libraries to support fixed-point control and EEPROM emulation
- On-chip debug support via single pin DAP interface (SPD)
- Packages:
  - PG-DSO-24
  - PG-TSSOP-28
- Temperature range T_A:
  - SAF (-40 to 85 °C)
  - SAK (-40 to 125 °C)

2.3 Pin Configuration

The pin configuration of the XC835 in **Figure 4**.

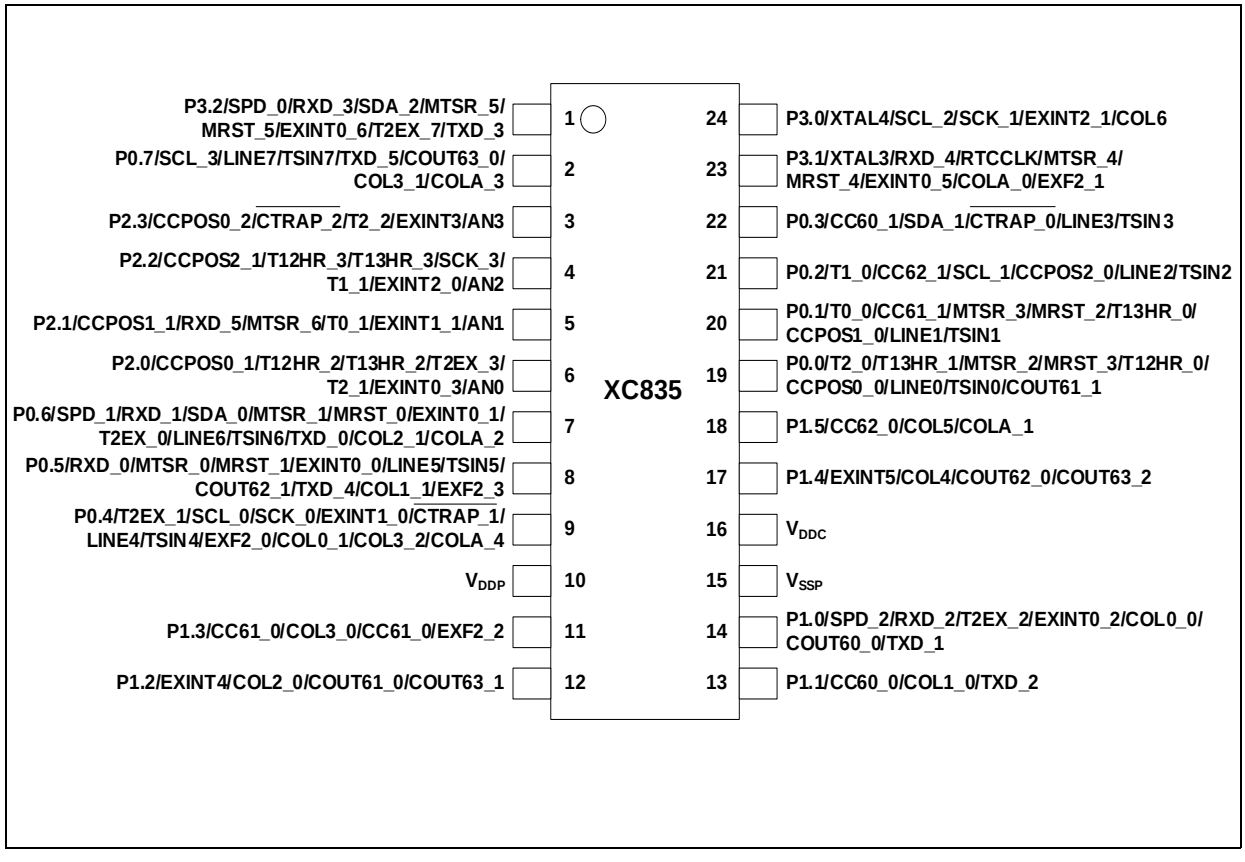


Figure 4 XC835 Pin Configuration, PG-DSO-24 Package (top view)

The pin configuration of the XC836 in **Figure 5**.

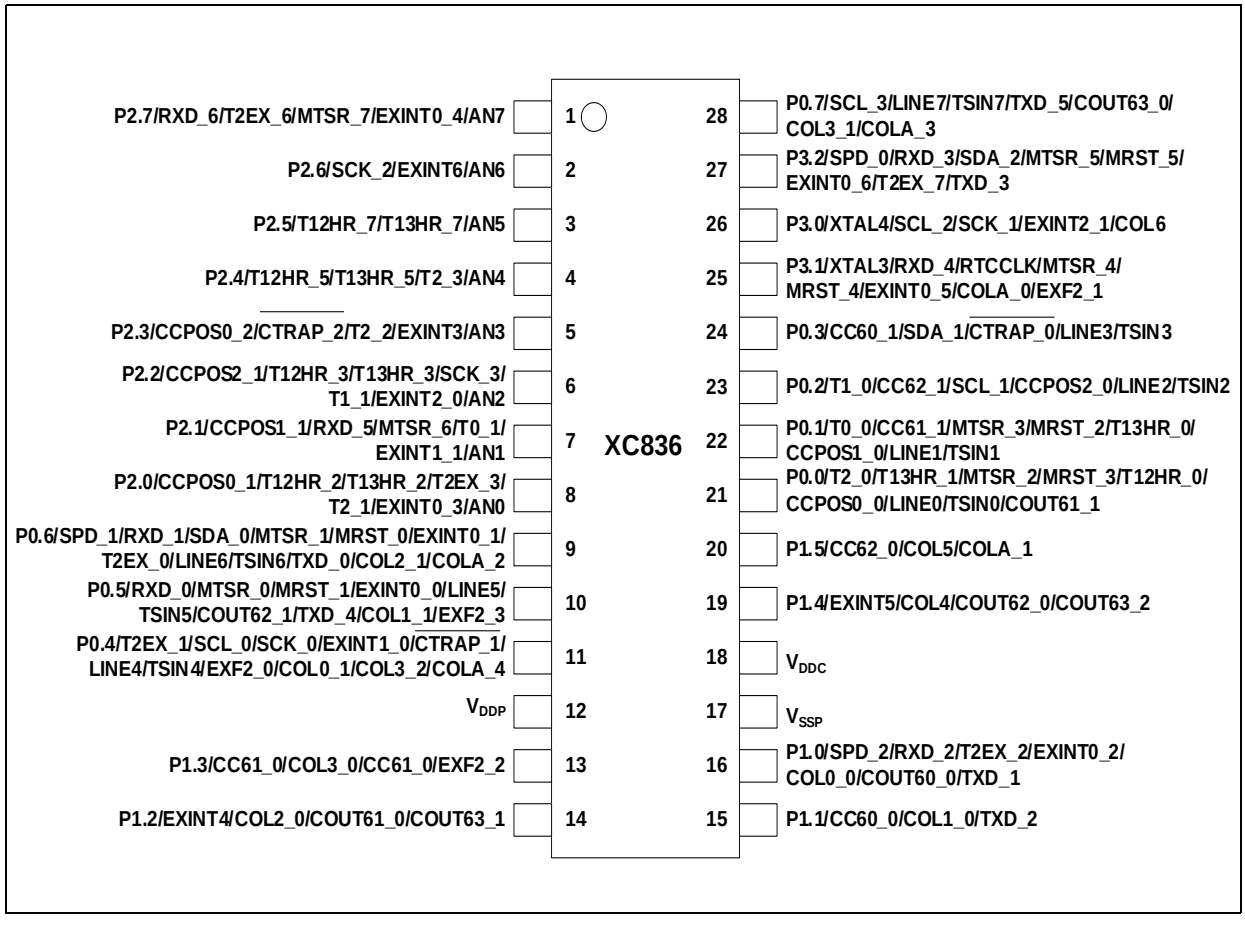


Figure 5 XC836 Pin Configuration, PG-TSSOP-28 Package (top view)

Table 3 Pin Definitions and Functions for XC835/836 (cont'd)

Symbol	Pin Number TSSOP28/ DS024	Type	Reset State	Function	
P0.1	22/20		Hi-Z	T0_0	Timer 0 Input
				CC61_1	Input/Output of Capture/Compare channel 1
				MTSR_3	SSC Slave Receive Input
				MRST_2	SSC Master Receive Input/ Slave Transmit Output
				T13HR_0	CCU6 Timer 13 Hardware Run Input
				CCPOS1_0	CCU6 Hall Input 1
				TSIN1	Touch-sense Input 1
				LINE1	LED Line 1
P0.2	23/21		Hi-Z	T1_0	Timer 1 Input
				CC62_1	Input/Output of Capture/Compare channel 2
				SCL_1	IIC Clock Line
				CCPOS2_0	CCU6 Hall Input 2
				TSIN2	Touch-sense Input 2
				LINE2	LED Line 2
P0.3	24/22		Hi-Z	CC60_1	Input/Output of Capture/Compare channel 0
				SDA_1	IIC Data Line
				$\overline{\text{CTRAP\_0}}$	CCU6 Trap Input
				TSIN3	Touch-sense Input 3
				LINE3	LED Line 3

Table 3 Pin Definitions and Functions for XC835/836 (cont'd)

Symbol	Pin Number TSSOP28/ DS024	Type	Reset State	Function	
P0.4	11/9		PD	T2EX_1	Timer 2 External Trigger Input
				SCK_0	SSC Clock Input/Output
				SCL_0	IIC Clock Line
				$\overline{\text{CTRAP}}$_1	CCU6 Trap Input
				EXINT1_0	External Interrupt Input 1
				TSIN4	Touch-sense Input 4
				LINE4	LED Line 4
				EXF2_0	Timer 2 Overflow Flag
				COL0_1	LED Column 0
				COL3_2	LED Column 3
				COLA_4	LED Column A
P0.5	10/8		Hi-Z	RXD_0	UART Receive Input
				MTSR_0	SSC Master Transmit Output/ Slave Receive Input
				MRST_1	SSC Master Receive Input
				EXINT0_0	External Interrupt Input 0
				TSIN5	Touch-sense Input 5
				LINE5	LED Line 5
				COUT62_1	Output of Capture/Compare Channel 2
				TXD_4	UART Transmit Output
				COL1_1	LED Column 1
				EXF2_3	Timer 2 Overflow Flag

Table 3 Pin Definitions and Functions for XC835/836 (cont'd)

Symbol	Pin Number TSSOP28/ DS024	Type	Reset State	Function	
P0.6	9/7		PU	SPD_1	SPD Input/Output
				RXD_1	UART Receive Input
				SDA_0	IIC Data Line
				MTSR_1	SSC Slave Receive Input
				MRST_0	SSC Master Receive Input/ Slave Transmit Output
				EXINT0_1	External Interrupt Input 0
				T2EX_0	Timer 2 External Trigger Input
				TSIN6	Touch-sense Input 6
				LINE6	LED Line 6
				TXD_0	UART Transmit Output
				COL2_1	LED Column 2
				COLA_2	LED Column A
P0.7	28/2		Hi-Z	SCL_3	IIC Clock Line
				TSIN7	Touch-sense Input 7
				LINE7	LED Line 7
				TXD_5	UART Transmit Output/ 2-wire UART BSL Transmit Output
				COUT63_0	Output of Capture/Compare Channel 3
				COL3_1	LED Column 3
				COLA_3	LED Column A
P1		I/O		**Port 1** Port 1 is a bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, LEDTSCU, SPD, UART and Timer 2	

Table 3 Pin Definitions and Functions for XC835/836 (cont'd)

Symbol	Pin Number TSSOP28/ DS024	Type	Reset State	Function	
P1.0	16/14		Hi-Z	SPD_2	SPD Input/Output
				RXD_2	UART Receive Input
				T2EX_2	Timer 2 External Trigger Input
				EXINT0_2	External Interrupt Input 0
				COL0_0	LED Column 0
				COUT60_0	Output of Capture/Compare Channel 0
				TXD_1	UART Transmit Output
P1.1	15/13		Hi-Z	CC60_0	Input/Output of Capture/Compare channel 0
				COL1_0	LED Column 1
				TXD_2	UART Transmit Output
P1.2	14/12		Hi-Z	EXINT4	External Interrupt Input 4
				COL2_0	LED Column 2
				COUT61_0	Output of Capture/Compare channel 1
				COUT63_1	Output of Capture/Compare channel 3
P1.3	13/11		Hi-Z	CC61_0	Input/Output of Capture/Compare channel 1
				COL3_0	LED Column 3
				EXF2_2	Timer 2 Overflow Flag
P1.4	19/17		Hi-Z	EXINT5	External Interrupt Input 5
				COL4	LED Column 4
				COUT62_0	Output of Capture/Compare channel 2
				COUT63_2	Output of Capture/Compare channel 3

2.7 Chip Identification Number

The XC835/836 identity (ID) register is located at Page 1 of address $B3_H$. The value of ID register is 59_H. However, for easy identification of product variants, the Chip Identification Number, which is an unique number assigned to each product variant, is available. The differentiation is based on the product and variant type information.

Two methods are provided to read a device's Chip Identification number:

- In-application subroutine, GET_CHIP_INFO
- Boot-loader (BSL) mode A

Table 5 lists the Chip Identification numbers of XC835/836 device variants.

Table 5 Chip Identification Number

Product Variant	Chip Identification Number
XC835MT-2FG	59100001_H
XC836-2FR	59100060_H
XC836T-2FR	59100040_H
XC836M-2FR	59100020_H
XC836M-1FR	59100120_H
XC836MT-2FR	59100000_H
XC836MT-1FR	59100100_H

3.1.3 Operating Condition

The following operating conditions must not be exceeded in order to ensure correct operation of the XC835/836. All parameters mentioned in the following tables refer to these operating conditions, unless otherwise noted.

Table 7 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes/ Conditions
		Min.	Max.		
Digital power supply voltage	V_{DDP}	3.0	5.5	V	
		2.5	3.0	V	1)
Digital core supply voltage2)	V_{DDC}	2.3	2.7	V	
CPU Clock Frequency	f_{CCLK}	22.5	25.6	MHz	typ. 24 MHz
		7.5	8.5	MHz	typ. 8 MHz
Ambient temperature	T_A	-40	85	°C	SAF-XC835/836...
		-40	125	°C	SAK-XC836...

1) In this voltage range, limited operations are available in active mode. Operations in power save modes are fully supported.

2) V_{DDC} is supplied by the on-chip EVR. The limits are verified by design and production testing.

3.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

3.2.1 Input/Output Characteristics

Table 8 provides the characteristics of the input/output pins of the XC835/836.

Table 8 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Output low voltage on port pins (all except P1)	V_{OLP} CC	–	1.0	V	I_{OL} = 25 mA (5 V) I_{OL} = 13 mA (3.3 V)
		–	0.4	V	I_{OL} = 10 mA (5 V) I_{OL} = 5 mA (3.3 V)
Output low voltage on P1[3:0]	V_{OLP1} CC	–	1.0	V	I_{OL} = 50 mA (5 V) I_{OL} = 25 mA (3.3 V)
		–	0.32	V	I_{OL} = 20 mA (5 V)
		–	0.4	V	I_{OL} = 10 mA (3.3 V)
Output low voltage on P1[5:4]	V_{OLP2} CC	–	1.0	V	I_{OL} = 50 mA (5 V) I_{OL} = 25 mA (3.3 V)
		–	0.4	V	I_{OL} = 20 mA (5 V) I_{OL} = 10 mA (3.3 V)
Output high voltage on port pins (all except P1)	V_{OHP} CC	V_{DDP} - 1.0	–	V	I_{OH} = -15 mA (5 V) I_{OH} = -8 mA (3.3 V)
		V_{DDP} - 0.4	–	V	I_{OH} = -5 mA (5 V) I_{OH} = -2.5 mA (3.3 V)
Output high voltage on P1[3:0]	V_{OHP1} CC	V_{DDP} - 0.32	–	V	I_{OH} = -20 mA (5 V)
		V_{DDP} - 1.0	–	V	I_{OH} = -25 mA (3.3 V)
		V_{DDP} - 0.4	–	V	I_{OH} = -10 mA (3.3 V)
Output high voltage on P1[5:4]	V_{OHP2} CC	V_{DDP} - 1.0	–	V	I_{OH} = -30 mA (5 V) I_{OH} = -16 mA (3.3 V)
		V_{DDP} - 0.4	–	V	I_{OH} = -10 mA (5 V) I_{OH} =- 5 mA (3.3 V)

Table 8 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	5)
Maximum current per pin (excluding P1, V_{DDP} and V_{SS})	I_{MP}	SR	-15	25	mA	–
Maximum current per pin for P1[3:0]	I_{MP1A}	SR	-50	50	mA	–
Maximum current per pin for P1[5:4]	I_{MP1B}	SR	-30	50	mA	–
Maximum current into V_{DDP}	I_{MVDDP}	SR	–	130	mA	4)
Maximum current out of V_{SS}	I_{MVSS}	SR	–	130	mA	4)

1) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.

3) Over current detection is available for 5V application only.

4) Not subjected to production test, verified by design/characterization.

5) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

Table 14 Emulated Flash Data Retention and Endurance based on EEPROM Emulation ROM Library (Operating Conditions apply)

Retention	Endurance[1)]	Emulation Size	Remarks
2 years	1,600,000 cycles	31 bytes	
2 years	1,400,000 cycles	62 bytes	
2 years	1,200,000 cycles	93 bytes	
2 years	1,000,000 cycles	124 bytes	

1) These values show the maximum endurance. Maximum endurance is the maximum possible unique data write if each data update is only 31 bytes. Minimum endurance cycle is the maximum possible unique data write if each data update is the same as the emulation size. The minimum endurance cycle can be calculated using the formulae [(max. endurance)*(31)/(emulation size)].

3.3 AC Parameters

The electrical characteristics of the AC Parameters are detailed in this section.

3.3.1 Testing Waveforms

The testing waveforms for rise/fall time, output delay and output high impedance are shown in **Figure 11**, **Figure 12** and **Figure 13**.

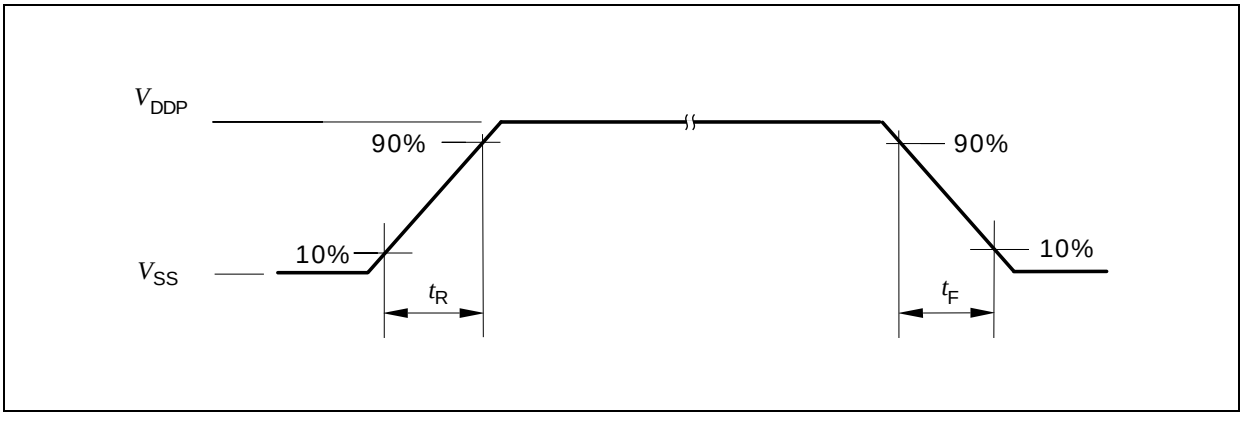


Figure 11 Rise/Fall Time Parameters

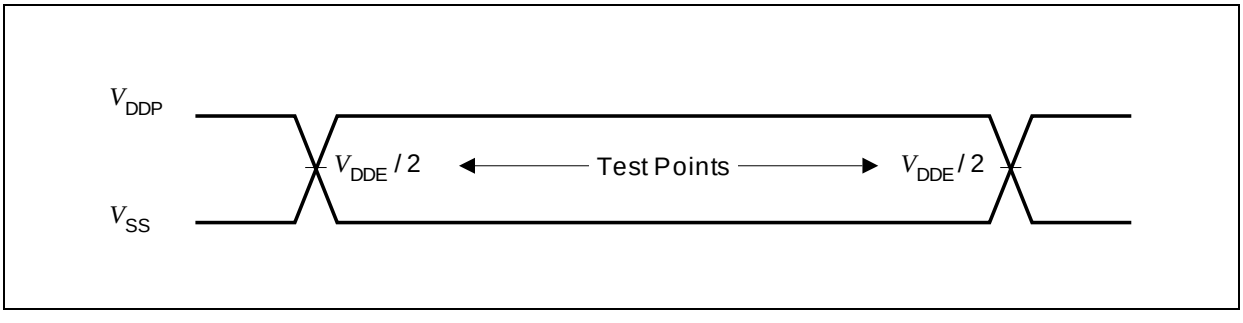


Figure 12 Testing Waveform, Output Delay

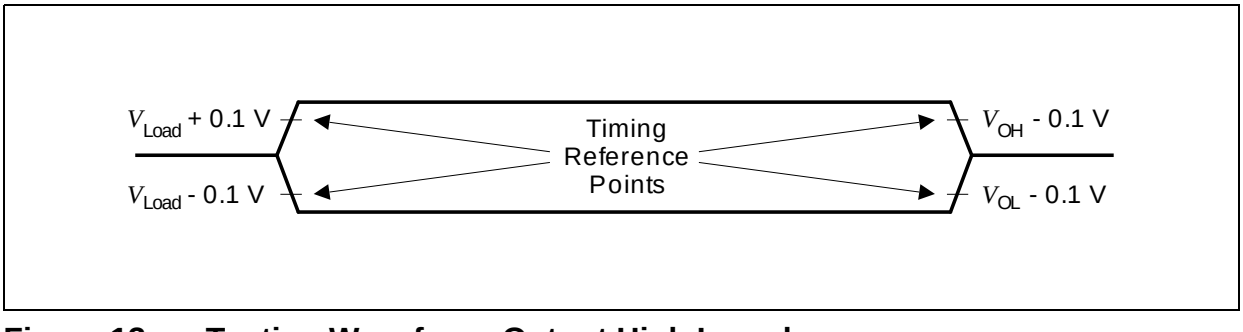


Figure 13 Testing Waveform, Output High Impedance

3.3.2 Output Rise/Fall Times

Table 18 provides the characteristics of the output rise/fall times in the XC835/836.

Table 18 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Rise/fall times on High Current Pad Type A[1)2)]	t_{HCPR}, t_{HCPF}	–	15	ns	20 pF @ Fast edge (5 V) [3)].
		–	150	ns	20 pF @ Slow Edge (5 V)[3)].
		–	25	ns	20 pF @ Fast edge (3.3 V)[4)].
		–	300	ns	20 pF @ Slow edge (3.3 V)[4)].
Rise/fall times on High Current Pad Type B[1)2)]	t_R, t_F	–	10	ns	20 pF[3)4)] (5 V & 3.3 V).
Rise/fall times on Standard Pad[1)2)]	t_R, t_F	–	10	ns	20 pF[3)4)] (5 V & 3.3 V).

1) Rise/Fall time parameters are taken with 10% - 90% of supply.

2) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.

3) Additional rise/fall time valid for C_L = 20 pF - C_L = 100 pF @ 0.125 ns/pF at 5 V supply voltage.

4) Additional rise/fall time valid for C_L = 20 pF - C_L = 100 pF.@ 0.225 ns/pF at 3.3 V supply voltage.

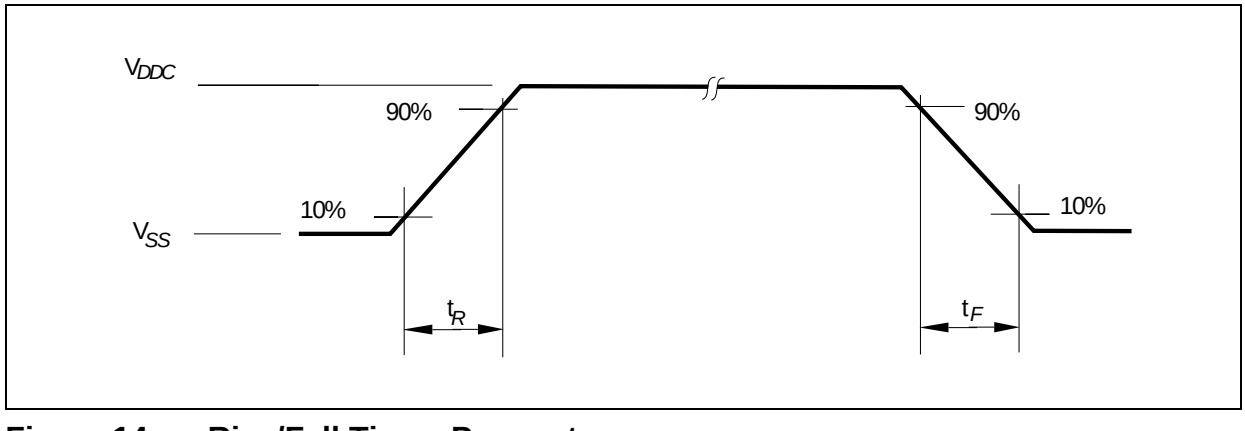


Figure 14 Rise/Fall Times Parameters

3.3.4 On-Chip Oscillator Characteristics

Table 20 provides the characteristics of the 48 MHz oscillator in the XC835/836.

Table 20 48 MHz Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	-0.5 %	48	+0.5%	MHz	under nominal conditions[1] after trimming
Long term frequency deviation	Δf_{LT}	CC	-2.0	–	3.0	%	with respect to f_{NOM}, over lifetime and temperature (0 °C to 85 °C)
			-4.5	–	4.5	%	with respect to f_{NOM}, over lifetime and temperature (-40 °C to 125 °C)
Short term frequency deviation (over V_{DDC})	Δf_{ST}	CC	-1	–	1	%	with respect to f_{NOM}, within one LIN message (< 10 ms … 100 ms)

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

Table 21 provides the characteristics of the 75 kHz oscillator in the XC835/836.

Table 21 75 kHz Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	-1%	75	+1%	KHz	under nominal conditions[1] after trimming
Long term frequency deviation	Δf_{LT}	CC	-4.5	–	4.5	%	with respect to f_{NOM}, over lifetime and temperature (-40 °C to 125 °C)
Short term frequency deviation	Δf_{ST}	CC	-1.5	–	1.5	%	with respect to f_{NOM}, over V_{DDC}

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

3.3.5.2 SSC Slave Mode Timing

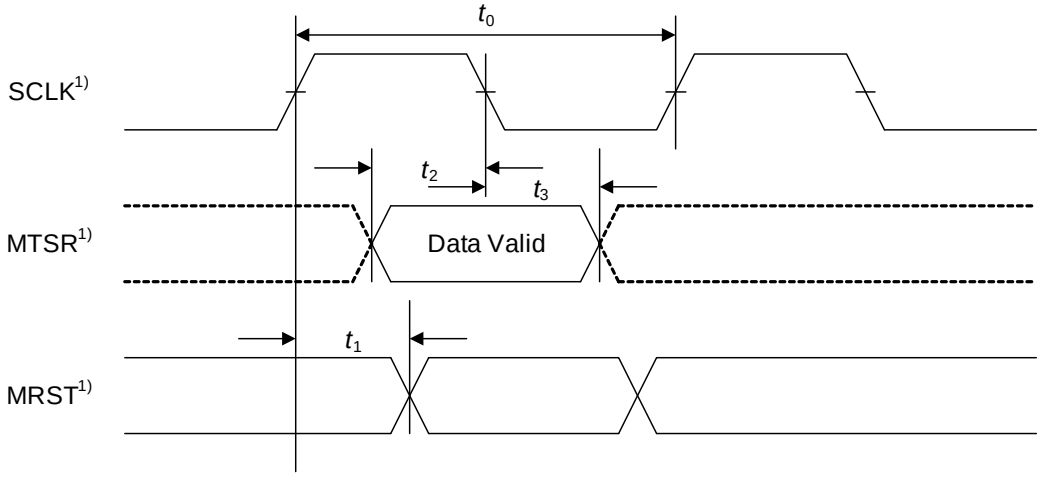
Table 23 provides the SSC slave mode timing in the XC835/836.

Table 23 SSC Slave Mode Timing[1] (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
SCLK clock period	t_0	SR	4 * T_{SSC}[2]	–	ns
MRST delay from SCLK	t_1	CC	0	29	ns
MTSR set-up to SCLK	t_2	SR	32	–	ns
MTSR hold from SCLK	t_3	SR	0	–	ns

1) Not subject to production test, verified by design/characterisation.

2) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When f_{CPU} = 24 MHz, t_0 = 166.7 ns. T_{CPU} is the CPU clock period.



1) This timing is based on the following setup : CON.PH = CON.PO = 0.

Figure 16 SSC Slave Mode Timing

4 Package and Quality Declaration

Chapter 4 provides the information of the XC835/836 package and reliability section.

4.1 Package Parameters

Table 24 provides the thermal characteristics of the packages used in XC835 and XC836 respectively.

Table 24 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Thermal resistance junction case[1)]	R_{TJC} CC	-	30.8	K/W	PG-DSO-24-1
		-	27.0	K/W	PG-TSSOP-28-1
		-	20.2	K/W	PG-TSSOP-28-12
Thermal resistance junction lead[1)]	R_{TJL} CC	-	30.5	K/W	PG-DSO-24-1
		-	195.3	K/W	PG-TSSOP-28-1
		-	41	K/W	PG-TSSOP-28-12

1) The thermal resistances between the case and the ambient (R_{TCA}) , the lead and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case (R_{TJC}), the junction and the lead (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J=T_A+R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances, by
a) simply adding only the two thermal resistances (junction lead and lead ambient), or
b) by taking all four resistances into account, depending on the precision needed.