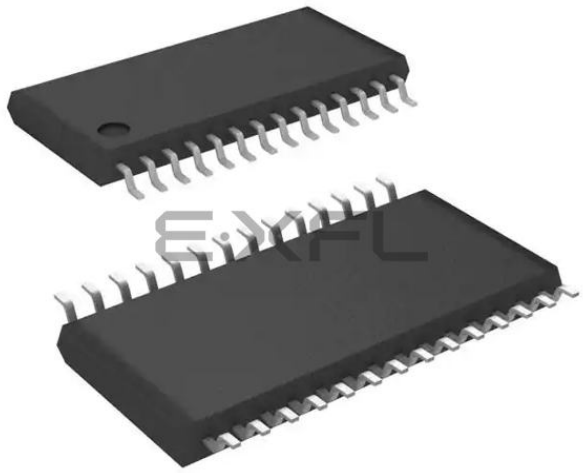
Infineon Technologies - XC836T2FRIABFXUMA1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-28-1
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc836t2friabfxuma1

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Features: (continued)

- Power saving modes
  - idle mode
  - power-down mode with wake-up capability via real-time clock event
  - clock gating control to each peripheral
- Programmable 16-bit Watchdog Timer (WDT) running on independent oscillator with programmable window feature for refresh operation and warning prior to overflow
- Three general purpose I/O ports
  - 4 high current I/O
  - 2 high sink I/O
  - Up to 25 pins as digital I/O
  - Up to 8 pins as digital/analog input
- Up to 8 channels, 10-bit A/D Converter
  - support up to 7 differential input channel
  - results filtering by data reduction or digital low-pass filter, for up to 13-bit results
- Up to 8 channels, Out of range comparator
- Three 16-bit timers
  - Timer 0 and Timer 1 (T0 and T1)
  - Timer 2 (T2)
- Real-time clock with 32.768 kHz crystal pad
- 16-bit Vector Computer for Field-Oriented Control (FOC)
  - Multiplication/Division Unit (MDU) for arithmetic calculation
  - CORDIC Unit for trigonometric calculation
- Capture and Compare unit for PWM signal generation (CCU6)
- A full-duplex or half-duplex serial interface (UART)
- Synchronous serial channel (SSC)
- Inter-IC (IIC) serial interface
- LED and Touch-sense Controller (LEDTSCU)
- Software libraries to support fixed-point control and EEPROM emulation
- On-chip debug support via single pin DAP interface (SPD)
- Packages:
  - PG-DSO-24
  - PG-TSSOP-28
- Temperature range T_A:
  - SAF (-40 to 85 °C)
  - SAK (-40 to 125 °C)

Ordering Information

The ordering code for Infineon Technologies microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery

For the available ordering codes for the XC835/836, please refer to your responsible sales representative or your local distributor.

2 General Device Information

Chapter 2 contains the block diagram, pin configurations, definitions and functions of the XC835/836.

2.1 Block Diagram

The block diagram of the XC835/836 is shown in **Figure 2**.

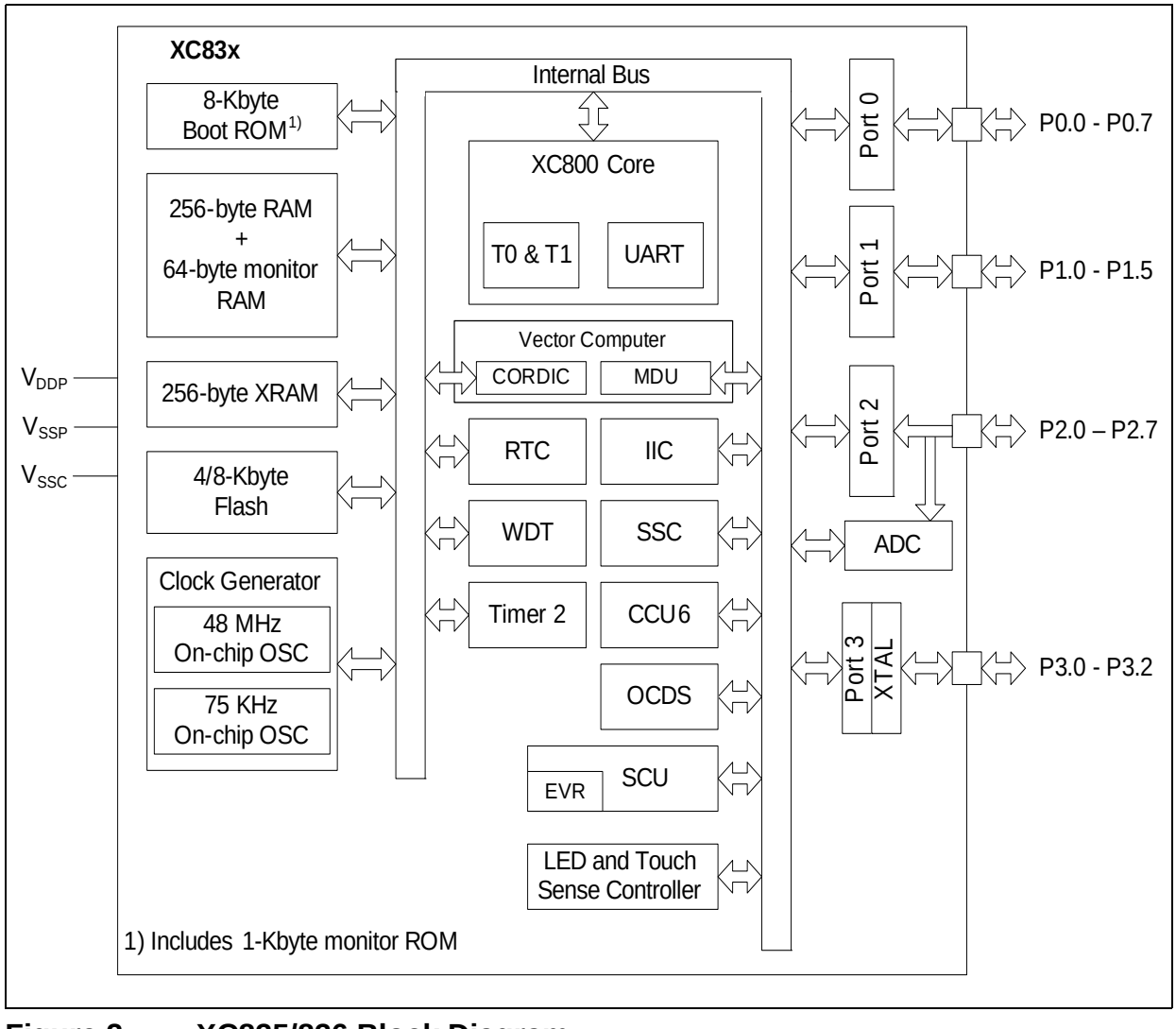


Figure 2 XC835/836 Block Diagram

2.2 Logic Symbol

The logic symbol of the XC835/836 is shown in **Figure 3**.

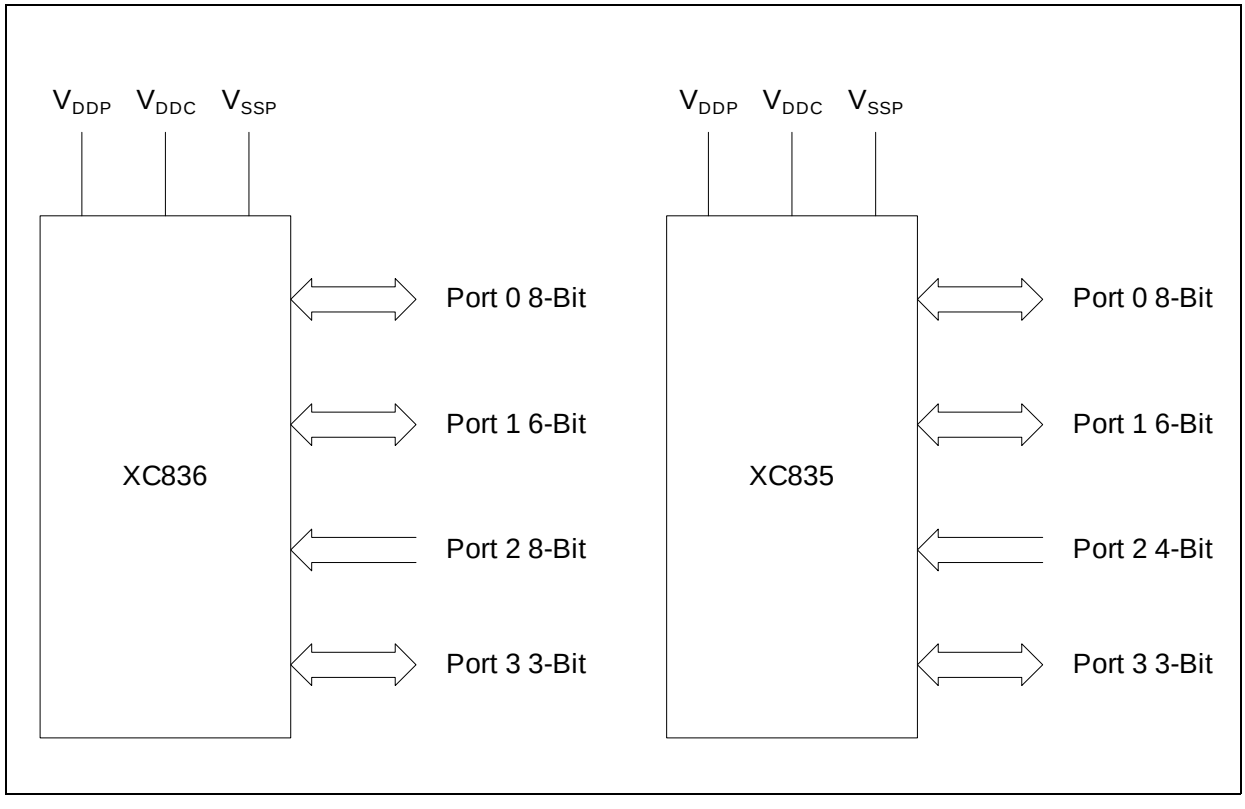


Figure 3 XC835/836 Logic Symbol

Table 3 Pin Definitions and Functions for XC835/836 (cont'd)

Symbol	Pin Number TSSOP28/ DS024	Type	Reset State	Function	
P1.0	16/14		Hi-Z	SPD_2	SPD Input/Output
				RXD_2	UART Receive Input
				T2EX_2	Timer 2 External Trigger Input
				EXINT0_2	External Interrupt Input 0
				COL0_0	LED Column 0
				COUT60_0	Output of Capture/Compare Channel 0
				TXD_1	UART Transmit Output
P1.1	15/13		Hi-Z	CC60_0	Input/Output of Capture/Compare channel 0
				COL1_0	LED Column 1
				TXD_2	UART Transmit Output
P1.2	14/12		Hi-Z	EXINT4	External Interrupt Input 4
				COL2_0	LED Column 2
				COUT61_0	Output of Capture/Compare channel 1
				COUT63_1	Output of Capture/Compare channel 3
P1.3	13/11		Hi-Z	CC61_0	Input/Output of Capture/Compare channel 1
				COL3_0	LED Column 3
				EXF2_2	Timer 2 Overflow Flag
P1.4	19/17		Hi-Z	EXINT5	External Interrupt Input 5
				COL4	LED Column 4
				COUT62_0	Output of Capture/Compare channel 2
				COUT63_2	Output of Capture/Compare channel 3

Table 3 Pin Definitions and Functions for XC835/836 (cont'd)

Symbol	Pin Number TSSOP28/ DS024	Type	Reset State	Function	
P1.5	20/18		Hi-Z	CC62_0	Input/Output of Capture/Compare channel 2
				COL5	LED Column 5
				COLA_1	LED Column A
P2		I		**Port 2** Port 2 is a general purpose input-only port. It can be used as inputs for A/D Converter and out of range comparator, CCU6, Timer 2, SSC and UART.	
P2.0	8/6		Hi-Z	CCPOS0_1	CCU6 Hall Input 0
				T12HR_2	CCU6 Timer 12 Hardware Run Input
				T13HR_2	CCU6 Timer 13 Hardware Run Input
				T2EX_3	Timer 2 External Trigger Input
				T2_1	Timer 2 Input
				EXINT0_3	External Interrupt Input 0
				AN0	Analog Input 0 / Out of range comparator channel 0
P2.1	7/5		Hi-Z	CCPOS1_1	CCU6 Hall Input 1
				RXD_5	UART Receive Input
				MTSR_6	SSC Slave Receive Input
				T0_1	Timer 0 Input
				EXINT1_1	External Interrupt Input 1
				AN1	Analog Input 1 / Out of range comparator channel 1

Table 3 Pin Definitions and Functions for XC835/836 (cont'd)

Symbol	Pin Number TSSOP28/ DS024	Type	Reset State	Function	
P2.2	6/4		Hi-Z	CCPOS2_1	CCU6 Hall Input 2
				T12HR_3	CCU6 Timer 12 Hardware Run Input
				T13HR_3	CCU6 Timer 13 Hardware Run Input
				SCK_3	SSC Clock Input/Output
				T1_1	Timer 1 Input
				EXINT2_0	External Interrupt Input 2
				AN2	Analog Input 2 / Out of range comparator channel 2
P2.3	5/3		Hi-Z	CCPOS0_2	CCU6 Hall Input 0
				$\overline{\text{CTRAP}}$_2	CCU6 Trap Input
				T2_2	Timer 2 Input
				EXINT3	External Interrupt Input 3
				AN3	Analog Input 3 / Out of range comparator channel 3
P2.4	4/-		Hi-Z	T12HR_5	CCU6 Timer 12 Hardware Run Input
				T13HR_5	CCU6 Timer 13 Hardware Run Input
				T2_3	Timer 2 Input
				AN4	Analog Input 4 / Out of range comparator channel 4
P2.5	3/-		Hi-Z	T12HR_7	CCU6 Timer 12 Hardware Run Input
				T13HR_7	CCU6 Timer 13 Hardware Run Input
				AN5	Analog Input 5 / Out of range comparator channel 5

Table 3 Pin Definitions and Functions for XC835/836 (cont'd)

Symbol	Pin Number TSSOP28/ DS024	Type	Reset State	Function	
P2.6	2/-		Hi-Z	SCK_2	SSC Clock Input/Output
				EXINT6	External Interrupt Input 6
				AN6	Analog Input 6 / Out of range comparator channel 6
P2.7	1/-		Hi-Z	RXD_6	UART Receive Input
				T2EX_6	Timer 2 External Trigger Input
				MTSR_7	SSC Slave Receive Input
				EXINT0_4	External Interrupt Input 0
				AN7	Analog Input 7 / Out of range comparator channel 7
P3		I/O		**Port 3** Port 3 is a bidirectional general purpose I/O port. It can be used as alternate functions for IIC, LEDTSCU, UART, Timer 2, SSC, SPD and 32.768 kHz crystal pad.	
P3.0	26/24		PU	SCL_2	IIC Clock Line
				SCK_1	SSC Clock Input/Output
				EXINT2_1	External Interrupt Input 2
				COL6	LED Column 6
				XTAL4	32.768 kHz External Oscillator Output

3 Electrical Parameters

Chapter 3 provides the characteristics of the electrical parameters which are implementation-specific for the XC835/836.

3.1 General Parameters

The general parameters are described here to aid the users in interpreting the parameters mainly in **Section 3.2** and **Section 3.3**.

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XC835/836 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  - These parameters indicate **C**ontroller **C**haracteristics, which are distinctive features of the XC835/836 and must be regarded for a system design.
- **SR**
  - These parameters indicate **S**ystem **R**equirements, which must be provided by the microcontroller system in which the XC835/836 is designed in.

3.1.2 Absolute Maximum Rating

Maximum ratings are the extreme limits to which the XC835/836 can be subjected to without permanent damage.

Table 6 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Ambient temperature	T_A	-40	125	°C	under bias
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	150	°C	under bias
Voltage on power supply pin with respect to V_{SS}	V_{DDP}	-0.5	6	V	
Maximum current per pin for P1[3:0]	I_M	-115	115	mA	
Input current on any pin during overload condition	I_{IN}	-10	10	mA	
Absolute sum of all input currents during overload condition	$\Sigma\|I_{IN}\|$	–	50	mA	

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pin with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

3.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

3.2.1 Input/Output Characteristics

Table 8 provides the characteristics of the input/output pins of the XC835/836.

Table 8 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Output low voltage on port pins (all except P1)	V_{OLP} CC	–	1.0	V	I_{OL} = 25 mA (5 V) I_{OL} = 13 mA (3.3 V)
		–	0.4	V	I_{OL} = 10 mA (5 V) I_{OL} = 5 mA (3.3 V)
Output low voltage on P1[3:0]	V_{OLP1} CC	–	1.0	V	I_{OL} = 50 mA (5 V) I_{OL} = 25 mA (3.3 V)
		–	0.32	V	I_{OL} = 20 mA (5 V)
		–	0.4	V	I_{OL} = 10 mA (3.3 V)
Output low voltage on P1[5:4]	V_{OLP2} CC	–	1.0	V	I_{OL} = 50 mA (5 V) I_{OL} = 25 mA (3.3 V)
		–	0.4	V	I_{OL} = 20 mA (5 V) I_{OL} = 10 mA (3.3 V)
Output high voltage on port pins (all except P1)	V_{OHP} CC	V_{DDP} - 1.0	–	V	I_{OH} = -15 mA (5 V) I_{OH} = -8 mA (3.3 V)
		V_{DDP} - 0.4	–	V	I_{OH} = -5 mA (5 V) I_{OH} = -2.5 mA (3.3 V)
Output high voltage on P1[3:0]	V_{OHP1} CC	V_{DDP} - 0.32	–	V	I_{OH} = -20 mA (5 V)
		V_{DDP} - 1.0	–	V	I_{OH} = -25 mA (3.3 V)
		V_{DDP} - 0.4	–	V	I_{OH} = -10 mA (3.3 V)
Output high voltage on P1[5:4]	V_{OHP2} CC	V_{DDP} - 1.0	–	V	I_{OH} = -30 mA (5 V) I_{OH} = -16 mA (3.3 V)
		V_{DDP} - 0.4	–	V	I_{OH} = -10 mA (5 V) I_{OH} =- 5 mA (3.3 V)

Table 8 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	5)
Maximum current per pin (excluding P1, V_{DDP} and V_{SS})	I_{MP}	SR	-15	25	mA	–
Maximum current per pin for P1[3:0]	I_{MP1A}	SR	-50	50	mA	–
Maximum current per pin for P1[5:4]	I_{MP1B}	SR	-30	50	mA	–
Maximum current into V_{DDP}	I_{MVDDP}	SR	–	130	mA	4)
Maximum current out of V_{SS}	I_{MVSS}	SR	–	130	mA	4)

1) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.

3) Over current detection is available for 5V application only.

4) Not subjected to production test, verified by design/characterization.

5) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

3.2.2 Supply Threshold Characteristics

Table 9 provides the characteristics of the supply threshold in the XC835/836.

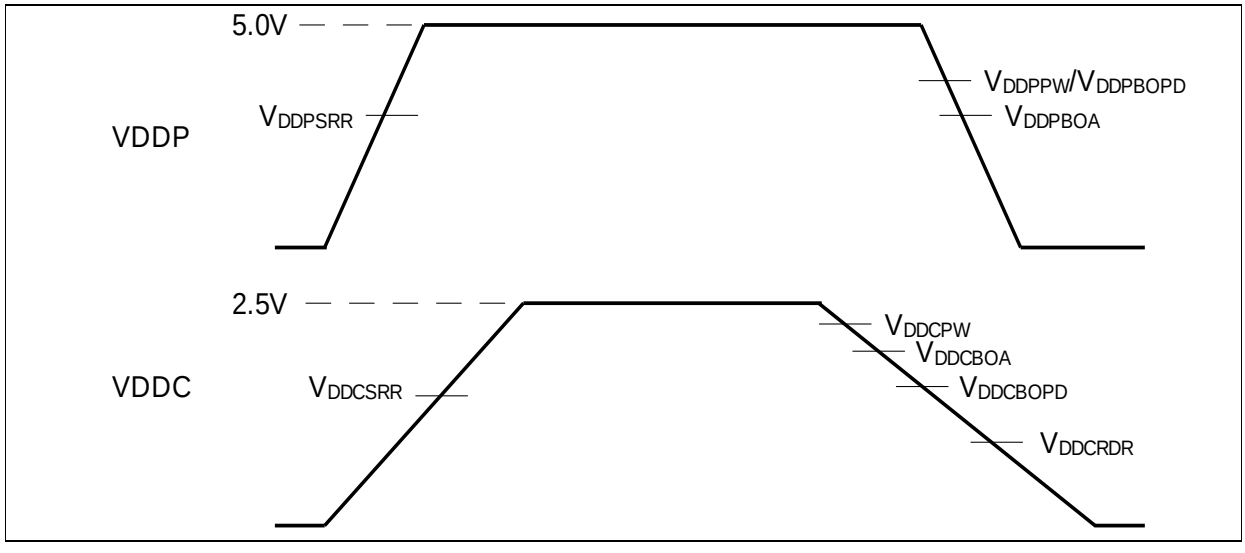


Figure 8 Supply Threshold Parameters

Table 9 Supply Threshold Parameters (Operating Conditions apply)

Parameters	Symbol		Limit Values			Unit
			Min.	Typ.	Max.	
V_{DDP} prewarning voltage[1)2)]	V_{DDPPW}	CC	3.0	3.6	4.5	V
V_{DDP} brownout voltage in active mode[2)3)]	V_{DDPBOA}	CC	2.65	2.75	2.87	V
V_{DDP} brownout voltage in all power down mode[2)3)]	$V_{DDPBOPD}$		3.0	3.6	4.5	V
V_{DDP} system reset release voltage[2)4)]	V_{DDPSRR}	CC	2.7	2.8	2.92	V
V_{DDC} prewarning voltage[2)5)]	V_{DDCPW}	CC	2.3	2.4	2.48	V
V_{DDC} brownout voltage in active mode[2)]	V_{DDCBOA}	CC	2.25	2.3	2.42	V
V_{DDC} brownout voltage in power down mode[2)]	$V_{DDCBOPD}$	CC	1.35	1.5	1.95	V
V_{DDC} system reset release voltage[2)4)]	V_{DDCSRR}	CC	2.28	2.3	2.47	V
RAM data retention voltage	V_{DDCRDR}	CC	1.1	–	–	V

1) Detection is enabled via SDCON register in active mode. It is automatically disabled in power down mode. Detection should be disabled for V_{DDP} less than maximum of V_{DDPPW}.

2) This parameter has a hysteresis of 50 mV.

3) Detection is enabled via SDCON register. Detection must be disabled for application with V_{DDP} less than the specified values.

4) V_{DDPSRR} and V_{DDCSRR} must be met before the system reset is released.

5) Detection is enabled via SDCON register in active mode. It is automatically disabled in power down mode.

3.2.3 ADC Characteristics

The values in **Table 10** are given for an analog power supply of 5.0 V. The ADC can be used with an analog power supply down to 3 V. But in this case, analog parameters may show a reduced performance. In the reduced voltage mode (2.5 V < V_{DDP} < 3 V), the ADC is not recommended to be used.

Table 10 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5 V; f_{ADCI} <= 12 MHz)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
Analog reference voltage	V_{AREF}		–	V_{DDP}	–	V	Connect internally to V_{DDP}
Analog reference ground	V_{AGND}		–	V_{SSP}	–	V	Connect internally to V_{SSP}
Alternate analog reference ground	$V_{AGNDALT}$	SR	V_{SSP} - 0.1	–	2.5[1)]	V	Connect to AN0 in differential mode, See **Figure 9**.
Internal voltage reference	V_{INTREF}	SR	1.19	1.23	1.28	V	[4)]
Analog input voltage range	V_{AIN}	SR	V_{AGND}	–	V_{AREF}	V	–
ADC clock	f_{ADCI}		8	–	16	MHz	internal analog clock
Sample time	t_S	CC	(2 + INPCR0.STC) × t_{ADCI}			µs	–
Conversion time	t_C	CC	See **Section 3.2.3.1**			µs	–
Set-up time between conversions using internal voltage reference	t_{SETUP}	SR	–	35	–	µs	[2)]

Table 10 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5 V; f_{ADCI} <= 12 MHz) (cont'd)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
Total unadjusted error	TUE[3]	CC	–	–	±1	LSB8	8-bit conversion with internal reference[4]
			–	–	+4/-2	LSB10	10-bit conversion with internal reference[4][5]
			–	–	+14/-2	LSB12	12-bit conversion using the Low Pass Filter [4]
Differential Nonlinearity	EA_{DNL}	CC	–	–	+1.5/ -1	LSB	10-bit conversion[4]
Integral Nonlinearity	EA_{INL}	CC	–	–	±1.5	LSB	10-bit conversion[4]
Offset	EA_{OFF}	CC	–	+4	–	LSB	10-bit conversion[4]
Gain	EA_{GAIN}	CC	–	-4	–	LSB	10-bit conversion[4]
Switched capacitance at an analog input	C_{AINSW}	CC	–	2	3	pF	[4][6]
Total capacitance at an analog input	C_{AINT}	CC	–	–	12	pF	[4][6]
Input resistance of an analog input	R_{AIN}	CC	–	1.5	2	kΩ	[4]

1) 1.2 V at V_{DDP} = 3.0 V.

2) Not subject to production test, verified at CPU clock ($f_{SCLK, CCLK}$) = 8 MHz, T_A = + 25 °C and V_{DDP} = 5 V.

3) TUE is tested at V_{AREF} = V_{DDP} = 5.0 V and CPU clock ($f_{SCLK, CCLK}$) = 8 MHz.

4) Not subject to production test, verified by design/characterization.

5) If a reduced positive reference voltage is used, TUE will increase. If the positive reference is reduced by a factor of K, the TUE will increased by 1/K. Example:K = 0.8, 1/K = 1.25; 1.25 X TUE = 2.5 LSB10.

6) The sampling capacity of the conversion C-Network is pre-charged to V_{AREF}/2 before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than V_{AREF}/2.

3.2.4 Flash Memory Parameters

The XC835/836 is delivered with all Flash sectors erased (read all zeros).

The data retention time of the XC835/836's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: Flash memory parameters are not subject to production test but verified by design and/or characterization.

Table 12 Flash Timing Parameters (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Read access time (per byte)	t_{ACC}	CC	–	125	–	ns	
Programming time (per wordline)	t_{PR}	CC	–	2.2	–	ms	
Erase time (one or more sectors)	t_{ER}	CC	–	120	–	ms	
Flash wait states	$N_{WSFLASH}$	CC	0				CPU clock = 8 MHz
			1				CPU clock = 24 MHz

Table 13 Flash Data Retention and Endurance (Operating Conditions apply)

Retention	Endurance[1)]	Size	Remarks
20 years	1,000 cycles	up to 8 Kbytes	
5 years	10,000 cycles	1 Kbyte	
2 years	70,000 cycles	512 bytes	
2 years	100,000 cycles	128 bytes	

1) One cycle refers to the programming of all wordlines in a sector and erasing of sector. The Flash endurance data specified in **Table 13** is valid only if the following conditions are fulfilled:
- the maximum number of erase cycles per Flash sector must not exceed 100,000 cycles.
- the maximum number of erase cycles per Flash bank must not exceed 300,000 cycles.
- the maximum number of program cycles per Flash bank must not exceed 2,500,000 cycles.

Table 14 Emulated Flash Data Retention and Endurance based on EEPROM Emulation ROM Library (Operating Conditions apply)

Retention	Endurance[1)]	Emulation Size	Remarks
2 years	1,600,000 cycles	31 bytes	
2 years	1,400,000 cycles	62 bytes	
2 years	1,200,000 cycles	93 bytes	
2 years	1,000,000 cycles	124 bytes	

1) These values show the maximum endurance. Maximum endurance is the maximum possible unique data write if each data update is only 31 bytes. Minimum endurance cycle is the maximum possible unique data write if each data update is the same as the emulation size. The minimum endurance cycle can be calculated using the formulae [(max. endurance)*(31)/(emulation size)].

3.3.5 SSC Timing

3.3.5.1 SSC Master Mode Timing

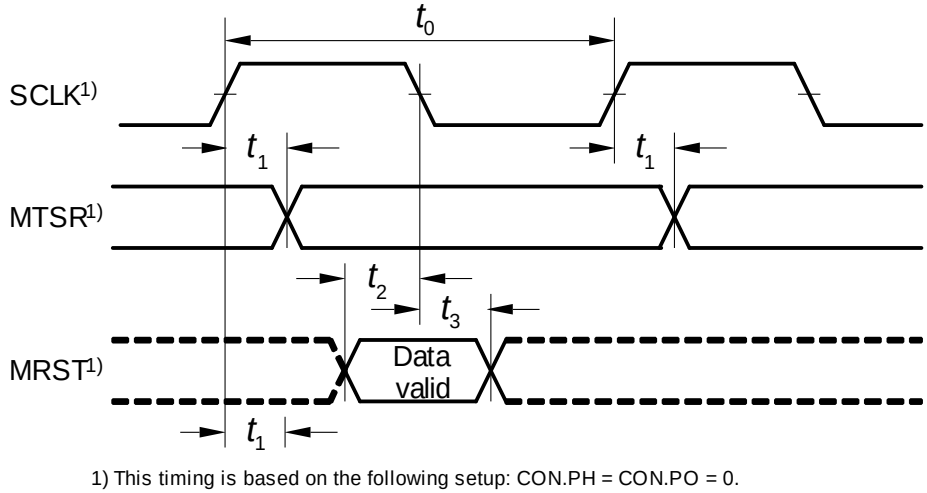
Table 22 provides the SSC master mode timing in the XC835/836.

Table 22 SSC Master Mode Timing[1] (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
SCLK clock period	t_0	CC	2 * T_{SSC}[2]	–	ns
MTSR delay from SCLK	t_1	CC	0	3	ns
MRST set-up to SCLK	t_2	SR	32	–	ns
MRST hold from SCLK	t_3	SR	0	–	ns

1) Not subject to production test, verified by design/characterisation.

2) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When f_{CPU} = 24 MHz, t_0 = 83.3 ns. T_{CPU} is the CPU clock period.



1) This timing is based on the following setup: CON.PH = CON.PO = 0.

SSC_Tmg1

Figure 15 SSC Master Mode Timing

4.3 Quality Declaration

Table 25 shows the characteristics of the quality parameters in the XC835/836.

Table 25 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Operation Lifetime when the device is used at the three stated T_J [1]	t_{OP1}	-	1500	hours	T_J = 150°C
		-	15000	hours	T_J = 110°C
		-	1500	hours	T_J = -40°C
Operation Lifetime when the device is used at the stated T_J [1]	t_{OP2}	-	131400	hours	T_J = 27°C
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	-	2000	V	Conforming to EIA/JESD22-A114-B [2]
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM}	-	500	V	Conforming to JESD22-C101-C [2]

1) This lifetime refers only to the time when device is powered-on.

2) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.