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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 30MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 16 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 5x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-TSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | 20-TSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc832m101fdh20fp |

Movable function for the I2C, USART, SPI, and SCTimer/PWM pin functions can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

Do not assign more than one output to any pin. However, more than one input can be assigned to a pin. Once any function is assigned to a pin, the pin's GPIO functionality is disabled.

Pin PIO0_4 triggers a wake-up from Deep power-down mode. If the part must wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin.

The JTAG functions TDO, TDI, TCK, TMS, and $\overline{\text{TRST}}$ are selected on pins PIO0_0 to PIO0_4 by hardware when the part is in boundary scan mode.

**Table 3. Pin description**

| Symbol | TSSOP20 | HVQFN33 | | Reset state[1] | Type | Description |
|---|---|---|---|---|---|---|
| PIO0_0/ TDO | 19 | 24 | [2] | I; PU | IO | **PIO0_0 —** General-purpose port 0 input/output 0.<br>In ISP mode, this is the U0_RXD pin.<br>In boundary scan mode: TDO (Test Data Out). |
| PIO0_1/ CLKIN/TDI | 12 | 16 | [2] | I; PU | IO | **PIO0_1 —** General-purpose port 0 input/output 1.<br>In boundary scan mode: TDI (Test Data In). |
| | | | | | I | **CLKIN —** External clock input. |
| SWDIO/PIO0_2/ TMS | 8 | 7 | [4] | I; PU | IO | **SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select). |
| | | | | | I/O | **PIO0_2 —** General-purpose port 0 input/output 2. |
| SWCLK/PIO0_3/ TCK | 7 | 6 | [4] | I; PU | I | **SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin.<br>In boundary scan mode: TCK (Test Clock). |
| | | | | | IO | **PIO0_3 —** General-purpose port 0 input/output 3. |
| PIO0_4/ADC_11/ TRSTN/WAKEUP | 6 | 4 | [3] | I; PU | IO | **PIO0_4 —** General-purpose port 0 input/output 4.<br>In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset).<br>In ISP mode, this pin is the U0_TXD pin.<br>This pin triggers a wake-up from Deep power-down mode. If the part must wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin. This pin should be pulled HIGH externally before entering Deep power-down mode. A LOW-going pulse as short as 50 ns causes the chip to exit Deep power-down mode and wakes up the part. |
| | | | | | A | **ADC_11 —** ADC input 11. |

**Table 3. Pin description**

| Symbol | TSSOP20 | HVQFN33 | | Reset state[1] | Type | Description |
|---|---|---|---|---|---|---|
| RESET/PIO0_5 | 5 | 3 | [7] | I; PU | IO | **RESET —** External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.<br>In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO or for any movable function if an external RESET function is not needed and the Deep power-down mode is not used. |
| | | | | | I | **PIO0_5 —** General-purpose port 0 input/output 5. |
| PIO0_6/ADC_1 | - | 23 | [10] | I; PU | IO | **PIO0_6 —** General-purpose port 0 input/output 6. |
| | | | | | A | **ADC_1 —** ADC input 1. |
| PIO0_7/ADC_0 | - | 22 | [2] | I; PU | IO | **PIO0_7 —** General-purpose port 0 input/output 7. |
| | | | | | A | **ADC_0 —** ADC input 0. |
| PIO0_8/XTALIN | 14 | 18 | [8] | I; PU | IO | **PIO0_8 —** General-purpose port 0 input/output 8. |
| | | | | | A | **XTALIN —** Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.95 V. |
| PIO0_9/XTALOUT | 13 | 17 | [8] | I; PU | IO | **PIO0_9 —** General-purpose port 0 input/output 9. |
| | | | | | A | **XTALOUT —** Output from the oscillator circuit. |
| PIO0_10/I2C0_SCL | 10 | 9 | [6] | Inactive | I; F | **PIO0_10 —** General-purpose port 0 input/output 10 (open-drain). |
| | | | | | | **I2C0_SCL —** Open-drain $I^2C$-bus clock input/output. High-current sink if $I^2C$ Fast-mode Plus is selected in the I/O configuration register. |
| PIO0_11/I2C0_SDA | 9 | 8 | [6] | Inactive | I; F | **PIO0_11 —** General-purpose port 0 input/output 11 (open-drain). |
| | | | | | | **I2C0_SDA —** Open-drain $I^2C$-bus data input/output. High-current sink if $I^2C$ Fast-mode Plus is selected in the I/O configuration register. |
| PIO0_12 | 4 | 2 | [4] | I; PU | IO | **PIO0_12 —** General-purpose port 0 input/output 12. ISP entry pin. A LOW level on this pin during reset starts the ISP command handler. |
| PIO0_13/ADC_10 | 3 | 1 | [2] | I; PU | IO | **PIO0_13 —** General-purpose port 0 input/output 13. |
| | | | | | A | **ADC_10 —** ADC input 10. |
| PIO0_14/ADC_2 | 20 | 25 | [2] | I; PU | IO | **PIO0_14 —** General-purpose port 0 input/output 14. |
| | | | | | A | **ADC_2 —** ADC input 2. |

# 8. Functional description

## 8.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 30 MHz using a two-stage pipeline. The core revision is r0p1.

Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

## 8.2 On-chip flash program memory

The LPC83x contain up to 32 KB of on-chip flash program memory. The flash memory supports a 64 Byte page size with page write and erase.

## 8.3 On-chip SRAM

The LPC83x contain a total of 4 KB on-chip static RAM data memory.

## 8.4 On-chip ROM

The on-chip ROM contains the bootloader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.

## 8.5 Memory map

The LPC83x incorporates several distinct memory regions. Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The ARM private peripheral bus includes the ARM core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.

Each oscillator, except the low-frequency oscillator, can be used for more than one purpose as required in a particular application.

Following reset, the LPC83x operates from the IRC until switched by software allowing the part to run without any external crystal and the bootloader code to operate at a known frequency.

See Figure 8 for an overview of the LPC83x clock generation.

#### 8.21.1.1 Internal RC Oscillator (IRC)

The IRC may be used as the clock source for the WWDT, and/or as the clock that drives the PLL and then the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1.5 % accuracy over the entire voltage and temperature range.

The IRC can be used as a clock source for the CPU with or without using the PLL. The IRC frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

Upon power-up or any chip reset, the LPC83x use the IRC as the clock source. Software may later switch to one of the other available clock sources.

#### 8.21.1.2 Crystal Oscillator (SysOsc)

The crystal oscillator can be used as the clock source for the CPU, with or without using the PLL.

The SysOsc operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

#### 8.21.1.3 Internal Low-power Oscillator and Watchdog Oscillator (WDOsc)

The nominal frequency of the WDOsc is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over silicon process variations is ± 40%.

The WDOsc is a dedicated oscillator for the windowed WWDT.

The internal low-power 10 kHz (± 40% accuracy) oscillator serves as the clock input to the WKT. This oscillator can be configured to run in all low-power modes.

### 8.21.2 Clock input

An external clock source can be supplied on the selected CLKIN pin directly to the PLL input. When selecting a clock signal for the CLKIN pin, follow the specifications for digital I/O pins in Table 8 “Static characteristics, supply pins” and Table 16 “Dynamic characteristics: I/O pins[1]”.

An 1.8 V external clock source can be supplied on the XTALIN pins to the system oscillator limiting the voltage of this signal (see Section 14.1).

The maximum frequency for both clock signals is 25 MHz.

### 8.21.3 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within

its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is nominally 100 μs.

### 8.21.4 Clock output

The LPC83x features a clock output function that routes the IRC, the SysOsc, the watchdog oscillator, or the main clock to the CLKOUT function. The CLKOUT function can be connected to any digital pin through the switch matrix.

### 8.21.5 Wake-up process

The LPC83x begin operation at power-up by using the IRC as the clock source allowing chip operation to resume quickly. If the SysOsc, the external clock source, or the PLL are needed by the application, software must enable these features and wait for them to stabilize before they are used as a clock source.

### 8.21.6 Power control

The LPC83x supports the ARM Cortex-M0 Sleep mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing to fine-tune power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

#### 8.21.6.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

#### 8.21.6.2 Deep-sleep mode

In Deep-sleep mode, the LPC83x core is in Sleep mode and all peripheral clocks and all clock sources are off except for the IRC and watchdog oscillator or low-power oscillator if selected. The IRC output is disabled. In addition, all analog blocks are shut down and the flash is in standby mode. In Deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC83x can wake up from Deep-sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI, or the I2C blocks (in slave mode).

### 8.22.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the ISP entry pin can be disabled without enabling CRP.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using the ISP entry pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

| CAUTION | |
|---|---|
|  | If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device. |

In addition to the three CRP levels, sampling of the ISP entry pin for valid user code can be disabled.

### 8.22.4 APB interface

The APB peripherals are located on one APB bus.

### 8.22.5 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0+ to the flash memory, the main static RAM, the CRC, the DMA, the ROM, and the APB peripherals.

## 8.23 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The Micro Trace Buffer is implemented on the LPC83x.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC83x is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode on pins PIO0_0 to PIO0_3 (see Table 3).

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

**Remark:** The JTAG interface cannot be used for debug purposes.

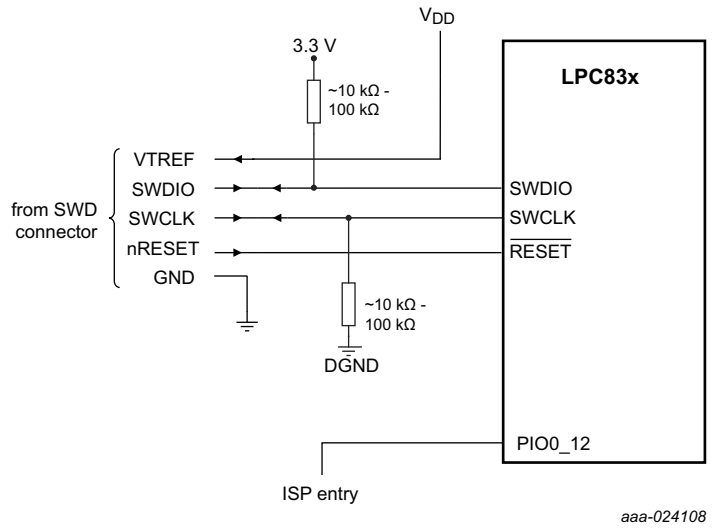



**Fig 10. Connecting the SWD pins to a standard SWD connector**

# 9. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*[1]

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage (core and external rail) | | [2] | −0.5 | +4.6 | V |
| $V_{ref}$ | reference voltage | on pin VREFP | | −0.5 | $V_{DD}$ | V |
| $V_I$ | input voltage | 5 V tolerant I/O pins; $V_{DD} \geq 1.8$ V | [3][4] | −0.5 | +5.5 | V |
| | | on I2C open-drain pins PIO0_10, PIO0_11 | [5] | −0.5 | +5.5 | V |
| | | 3 V tolerant I/O pin PIO0_6 | [6] | −0.5 | +3.6 | V |
| $V_{IA}$ | analog input voltage | | [7][8][9] | −0.5 | +4.6 | V |
| $V_{i(xtal)}$ | crystal input voltage | | [2] | −0.5 | +2.5 | V |
| $I_{DD}$ | supply current | per supply pin | | - | 100 | mA |
| $I_{SS}$ | ground current | per ground pin | | - | 100 | mA |
| $I_{latch}$ | I/O latch-up current | $-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C | | - | 100 | mA |
| $T_{stg}$ | storage temperature | | [9] | −65 | +150 | °C |
| $T_{j(max)}$ | maximum junction temperature | | | - | 150 | °C |
| $P_{tot(pack)}$ | total power dissipation (per package) | based on package heat transfer, not device power consumption | | - | 1.5 | W |
| $V_{esd}$ | electrostatic discharge voltage | human body model; all pins | [10] | - | 3500 | V |
| | | charged device model; HVQFN33 package | | - | 1200 | V |

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to $V_{SS}$ unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 7) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except true open-drain pins PIO0_10 and PIO0_11 and except the 3 V tolerant pin PIO0_6.

[4] Including the voltage on outputs in 3-state mode.

[5] $V_{DD}$ present or not present. Compliant with the $I^2C$-bus standard. 5.5 V can be applied to this pin when $V_{DD}$ is powered down.

[6] $V_{DD}$ present or not present.

[7] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than $10^6$ s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[8] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[9] Dependent on package type.

[10] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

# 10. Thermal characteristics

The average chip junction temperature, $T_j$ (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- $T_{amb}$ = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- $P_D$ = sum of internal and I/O power dissipation

The internal power dissipation is the product of $I_{DD}$ and $V_{DD}$. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

**Table 6. Thermal resistance**

| Symbol | Parameter | Conditions | Max/min | Unit |
|---|---|---|---|---|
| **HVQFN33 package** | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction-to-ambient | JEDEC (4.5 in × 4 in); still air | 40 +/- 15 % | °C/W |
| | | single-layer (4.5 in × 3 in); still air | 114 +/- 15 % | °C/W |
| $R_{th(j-c)}$ | thermal resistance from junction-to-case | | 18 +/- 15 % | °C/W |

## 11.2 Supply pins

**Table 8. Static characteristics, supply pins**

*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | supply current | Active mode; code `while(1){}` executed from flash; | | | | | |
| | | system clock = 12 MHz; default mode; $V_{DD}$ = 3.3 V | [2][3][4] [6][7] | - | 1.85 | - | mA |
| | | system clock = 12 MHz; low-current mode; $V_{DD}$ = 3.3 V | [2][3][4] [6][7] | - | 1.04 | - | mA |
| | | system clock = 30 MHz; default mode; $V_{DD}$ = 3.3 V | [2][3][6] [7][9] | - | 3.95 | - | mA |
| | | system clock = 30 MHz; low-current mode; $V_{DD}$ = 3.3 V | [2][3][6] [7][9] | - | 3.2 | - | mA |
| | | Sleep mode | | | | | |
| | | system clock = 12 MHz; default mode; $V_{DD}$ = 3.3 V | [2][3][4] [6][7] | - | 1.35 | - | mA |
| | | system clock = 12 MHz; low-current mode; $V_{DD}$ = 3.3 V | [2][3][4] [6][7] | - | 0.8 | - | mA |
| | | system clock = 30 MHz; default mode; $V_{DD}$ = 3.3 V | [2][3][9] [6][7] | - | 2.55 | - | mA |
| | | system clock = 30 MHz; low-current mode; $V_{DD}$ = 3.3 V | [2][3][9] [6][7] | - | 2.1 | - | mA |
| $I_{DD}$ | supply current | Deep-sleep mode; $V_{DD}$ = 3.3 V; $T_{amb}$ = 25 °C | [2][3][10] | - | 158 | 300 | µA |
| | | $T_{amb}$ = 85 °C | | - | - | 400 | µA |
| $I_{DD}$ | supply current | Power-down mode; $V_{DD}$ = 3.3 V $T_{amb}$ = 25 °C | [2][3][10] | - | 1.6 | 10 | µA |
| | | $T_{amb}$ = 85 °C | | - | - | 50 | µA |
| $I_{DD}$ | supply current | Deep power-down mode; $V_{DD}$ = 3.3 V; 10 kHz low-power oscillator and self-wake-up timer (WKT) disabled $T_{amb}$ = 25 °C | [2][11] | - | 0.2 | 1 | µA |
| | | $T_{amb}$ = 85 °C | | - | - | 4 | µA |

**Table 8. Static characteristics, supply pins** *…continued*

*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | supply current | Deep power-down mode; $V_{DD}$ = 3.3 V; 10 kHz low-power oscillator and self-wake-up timer (WKT) enabled | | - | 1.1 | - | μA |
| | | Deep power-down mode; $V_{DD}$ = 3.3 V; external clock input WKTCLKIN @ 10 kHz with self-wake-up timer enabled | | - | 0.4 | - | μA |
| | | Deep power-down mode; $V_{DD}$ = 3.3 V; external clock input WKTCLKIN @ 32 kHz with self-wake-up timer enabled | | - | 0.7 | - | μA |

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] $T_{amb}$ = 25 °C.

[3] $I_{DD}$ measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] System oscillator enabled; IRC disabled; system PLL disabled.

[6] BOD disabled.

[7] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to USART, CLKOUT, and IOCON disabled in system configuration block.

[8] IRC enabled; system oscillator disabled; system PLL enabled.

[9] IRC disabled; system oscillator enabled; system PLL enabled.

[10] All oscillators and analog blocks turned off.

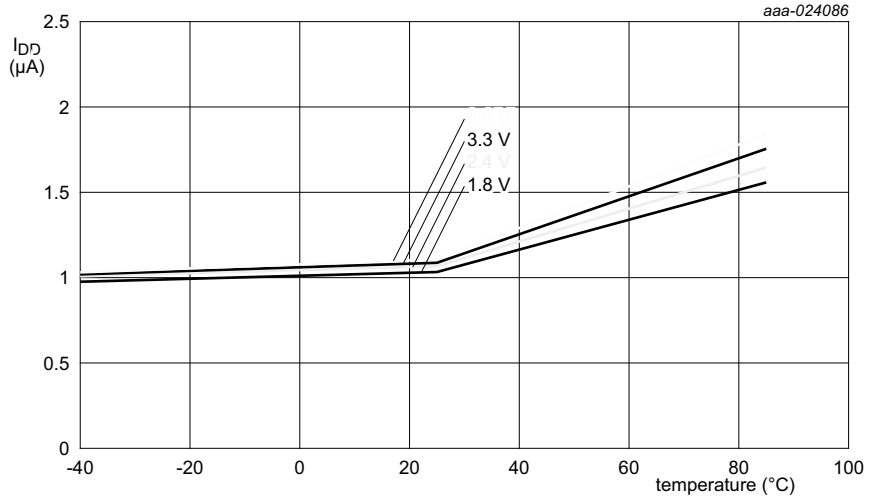
[11] WAKEUP pin pulled HIGH externally.

## 11.3 Electrical pin characteristics

**Table 9. Static characteristics, electrical pin characteristics**

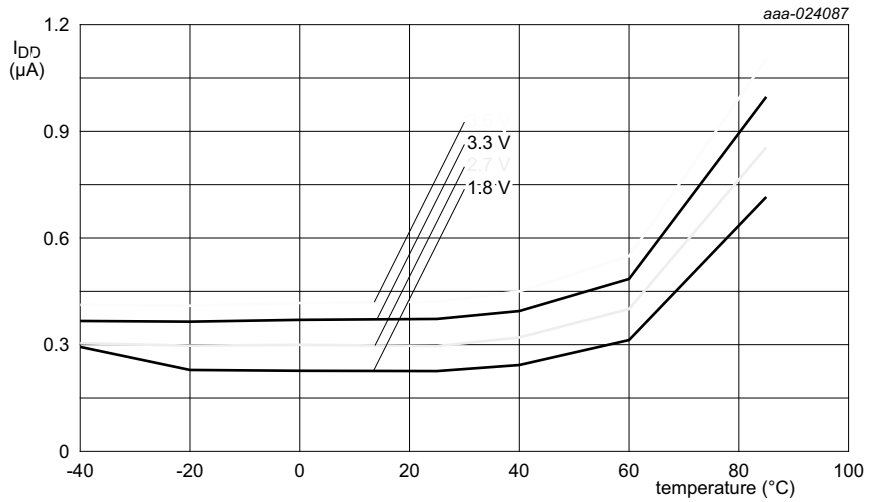
*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Standard port pins configured as digital pins, RESET** | | | | | | | |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0 V; on-chip pull-up resistor disabled | | - | 0.5 | 10[2] | nA |
| $I_{IH}$ | HIGH-level input current | $V_I = V_{DD}$; on-chip pull-down resistor disabled | | - | 0.5 | 10[2] | nA |
| $I_{OZ}$ | OFF-state output current | $V_O$ = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled | | - | 0.5 | 10[2] | nA |
| $V_I$ | input voltage | $V_{DD} \geq$ 1.8 V; 5 V tolerant pins except PIO0_12 | [4] [6] | 0 | - | 5 | V |
| | | $V_{DD}$ = 0 V | | 0 | - | 3.6 | V |
| $V_O$ | output voltage | output active | | 0 | - | $V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{DD}$ | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | | - | - | $0.3V_{DD}$ | V |
| $V_{hys}$ | hysteresis voltage | | | - | 0.4 | - | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = 4 mA; 2.5 V <= $V_{DD}$ <= 3.6 V | | $V_{DD} - 0.4$ | - | - | V |
| | | $I_{OH}$ = 3 mA; 1.8 V <= $V_{DD}$ < 2.5 V | | $V_{DD} - 0.4$ | - | - | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 4 mA; 2.5 V <= $V_{DD}$ <= 3.6 V | | - | - | 0.4 | V |
| | | $I_{OL}$ = 3 mA; 1.8 V <= $V_{DD}$ < 2.5 V | | - | - | 0.4 | V |
| $I_{OH}$ | HIGH-level output current | $V_{OH} = V_{DD} - 0.4$ V; 2.5 V ≤ $V_{DD}$ ≤ 3.6 V | | 4 | - | - | mA |
| | | 1.8 V ≤ $V_{DD}$ < 2.5 V | | 3 | - | - | mA |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V 2.5 V ≤ $V_{DD}$ ≤ 3.6 V | | 4 | - | - | mA |
| | | 1.8 V ≤ $V_{DD}$ < 2.5 V | | 3 | - | - | mA |
| $I_{OHS}$ | HIGH-level short-circuit output current | $V_{OH}$ = 0 V | [7] | - | - | 45 | mA |
| $I_{OLS}$ | LOW-level short-circuit output current | $V_{OL} = V_{DD}$ | [7] | - | - | 50 | mA |
| $I_{pd}$ | pull-down current | $V_I$ = 5 V | | 10 | 50 | 150 | μA |
| $I_{pu}$ | pull-up current | $V_I$ = 0 V; 2.0 V ≤ $V_{DD}$ ≤ 3.6 V | | 15 | 50 | 85 | μA |
| | | 1.8 V ≤ $V_{DD}$ < 2.0 V | | 10 | 50 | 85 | |
| | | $V_{DD} < V_I$ < 5 V | | 0 | 0 | 0 | μA |
| **High-drive output pin configured as digital pin (PIO0_2, PIO0_3, PIO0_12, PIO0_16)** | | | | | | | |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0 V; on-chip pull-up resistor disabled | | - | 0.5 | 10[2] | nA |
| $I_{IH}$ | HIGH-level input current | $V_I = V_{DD}$; on-chip pull-down resistor disabled | | - | 0.5 | 10[2] | nA |
| $I_{OZ}$ | OFF-state output current | $V_O$ = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled | | - | 0.5 | 10[2] | nA |



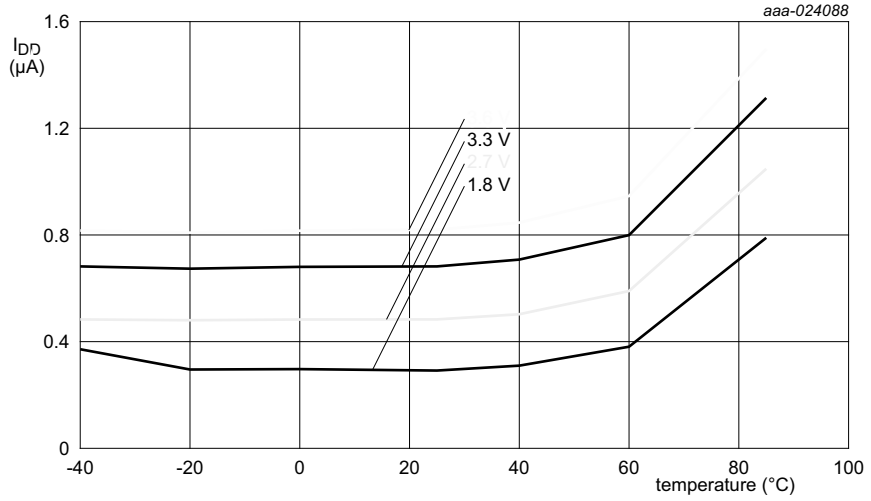

WKT running with internal 10 kHz low-power oscillator.

**Fig 18. Deep power-down mode: Typical supply current $I_{DD}$ versus temperature for different supply voltages $V_{DD}$ (internal clock)**



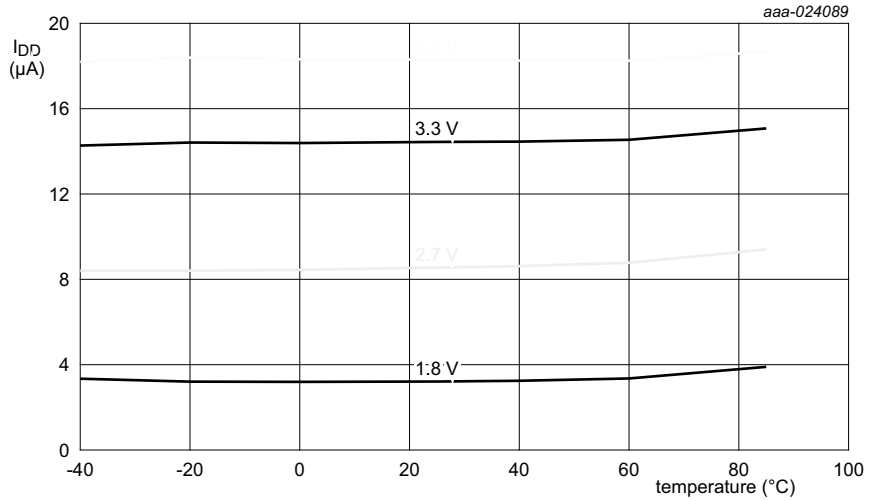

WKT running with external 10 kHz clock. Clock input waveform: square wave with rise time and fall time of 5 ns.

**Fig 19. Deep power-down mode: Typical supply current $I_{DD}$ versus temperature for different supply voltages $V_{DD}$ (external 10 kHz input clock)**



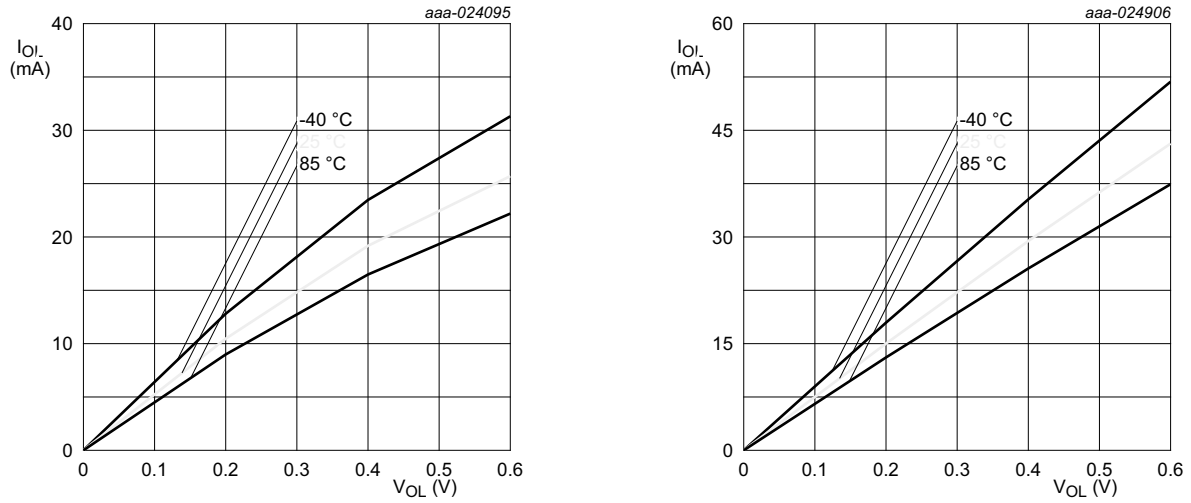

WKT running with external 32 kHz clock. Clock input waveform: square wave with rise time and fall time of 5 ns.

**Fig 20. Deep power-down mode: Typical supply current $I_{DD}$ versus temperature for different supply voltages $V_{DD}$ (external 32 kHz input clock)**




WKT running with external 1 MHz clock. Clock input waveform: square wave with rise time and fall time of 5 ns.

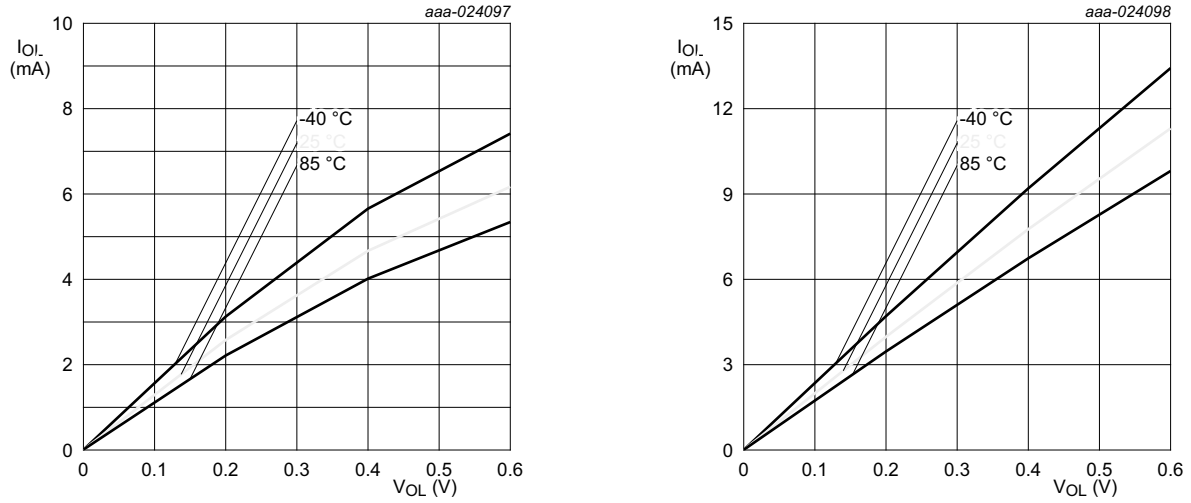
**Fig 21. Deep power-down mode: Typical supply current $I_{DD}$ versus temperature for different supply voltages $V_{DD}$ (external 1 MHz input clock)**




Conditions: $V_{DD}$ = 1.8 V; on pins PIO0_10 and PIO0_11.

Conditions: $V_{DD}$ = 3.3 V; on pins PIO0_10 and PIO0_11.

**Fig 25. $I^2C$-bus pins (high current sink): Typical LOW-level output current $I_{OL}$ versus LOW-level output voltage $V_{OL}$**




Conditions: $V_{DD}$ = 1.8 V; standard port pins and high-drive pin PIO0_12.

Conditions: $V_{DD}$ = 3.3 V; standard port pins and high-drive pin PIO0_12.

**Fig 26. Typical LOW-level output current $I_{OL}$ versus LOW-level output voltage $V_{OL}$**

**Table 12. Flash characteristics**

*$T_{amb}$ = −40 °C to +85 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{ret}$ | retention time | powered | | 10 | 20 | - | years |
| | | not powered | | 20 | 40 | - | years |
| $t_{er}$ | erase time | page or multiple consecutive pages, sector or multiple consecutive sectors | | 95 | 100 | 105 | ms |
| $t_{prog}$ | programming time | | [2] | 0.95 | 1 | 1.05 | ms |

[1] Number of program/erase cycles.

[2] Programming times are given for writing 64 bytes to the flash. $T_{amb}$ <= +85 °C.

## 12.3 External clock for the oscillator in slave mode

**Remark:** The input voltage on the XTALIN and XTALOUT pins must be ≤ 1.95 V (see Table 7). For connecting the oscillator to the XTAL pins, also see Section 12.3.

**Table 13. Dynamic characteristic: external clock (XTALIN input)**

*$T_{amb}$ = −40 °C to +85 °C; $V_{DD}$ over specified ranges.[1]*

| Symbol | Parameter | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|
| $f_{osc}$ | oscillator frequency | 1 | - | 25 | MHz |
| $T_{cy(clk)}$ | clock cycle time | 40 | - | 1000 | ns |
| $t_{CHCX}$ | clock HIGH time | $T_{cy(clk)} \times 0.4$ | - | - | ns |
| $t_{CLCX}$ | clock LOW time | $T_{cy(clk)} \times 0.4$ | - | - | ns |
| $t_{CLCH}$ | clock rise time | - | - | 5 | ns |
| $t_{CHCL}$ | clock fall time | - | - | 5 | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

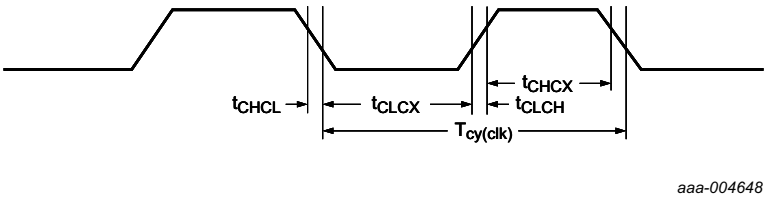



**Fig 31. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)**

## 12.4 Internal oscillators

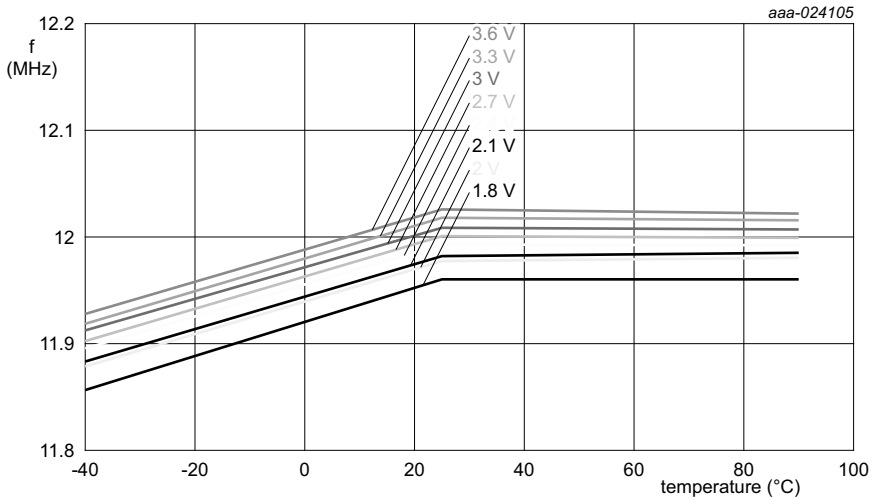
**Table 14. Dynamic characteristics: IRC**

*$T_{amb}$ = −40 °C to +85 °C; 2.7 V ≤ $V_{DD}$ ≤ 3.6 V*[1]

| Symbol | Parameter | Conditions | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{osc(RC)}$ | internal RC oscillator frequency | - | 11.82 | 12 | 12.18 | MHz |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.




Conditions: Frequency values are typical values. 12 MHz ± 1.5 % accuracy is guaranteed for 2.7 V ≤ $V_{DD}$ ≤ 3.6 V. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1.5 % accuracy specification for voltages below 2.7 V.

**Fig 32. Typical Internal RC oscillator frequency versus temperature**

**Table 15. Dynamic characteristics: Watchdog oscillator**

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{osc(int)}$ | internal oscillator frequency | DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register; | [2] | - | 9.4 | - | kHz |
| | | DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register | [2] | - | 2300 | - | kHz |

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature ($T_{amb}$ = −40 °C to +85 °C) is ±40 %.

### 12.4.1 I/O pins

**Table 16. Dynamic characteristics: I/O pins[1]**
*$T_{amb}$ = −40 °C to +85 °C; 3.0 V ≤ $V_{DD}$ ≤ 3.6 V.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_r$ | rise time | pin configured as output | | 3.0 | - | 5.0 | ns |
| $t_f$ | fall time | pin configured as output | | 2.5 | - | 5.0 | ns |

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

### 12.4.2 WKTCLKIN pin (wake-up clock input)

**Table 17. Dynamic characteristics: WKTCLKIN pin**
*$T_{amb}$ = −40 °C to +85 °C; 1.8 V ≤ $V_{DD}$ ≤ 3.6 V.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{clk}$ | clock frequency | deep power-down mode and power-down mode | [1] | - | 1 | MHz |
| | | deep-sleep, sleep, and active mode | [1] | - | 10 | MHz |
| $t_{CHCX}$ | clock HIGH time | - | | 50 | - | ns |
| $t_{CLCX}$ | clock LOW time | - | | 50 | - | ns |

[1] Assuming a square-wave input clock.

### 12.4.3 SCTimer/PWM

**Table 18. SCTimer/PWM output dynamic characteristics**
*$T_{amb}$ = −40 °C to +85 °C; 2.4 V <= $V_{DD}$ <= 3.6 V; $C_L$ = 10 pF. Simulated skew (over process, voltage, and temperature) of any two SCTimer/PWM output signals routed to standard I/O pins; sampled at the 50 % level of the falling or rising edge; values guaranteed by design.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{sk(o)}$ | output skew time | - | - | - | 4 | ns |

### 12.4.4 I²C-bus

**Table 19. Dynamic characteristic: I²C-bus pins[1]**
*$T_{amb}$ = −40 °C to +85 °C; values guaranteed by design.[2]*

| Symbol | Parameter | | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | | Standard-mode | 0 | 100 | kHz |
| | | | Fast-mode | 0 | 400 | kHz |
| | | | Fast-mode Plus; on pins PIO0_10 and PIO0_11 | 0 | 1 | MHz |
| $t_f$ | fall time | [4][5][6][7] | of both SDA and SCL signals<br>Standard-mode | - | 300 | ns |
| | | | Fast-mode | 20 + 0.1 × $C_b$ | 300 | ns |
| | | | Fast-mode Plus; on pins PIO0_10 and PIO0_11 | - | 120 | ns |

### 12.4.6 USART interface

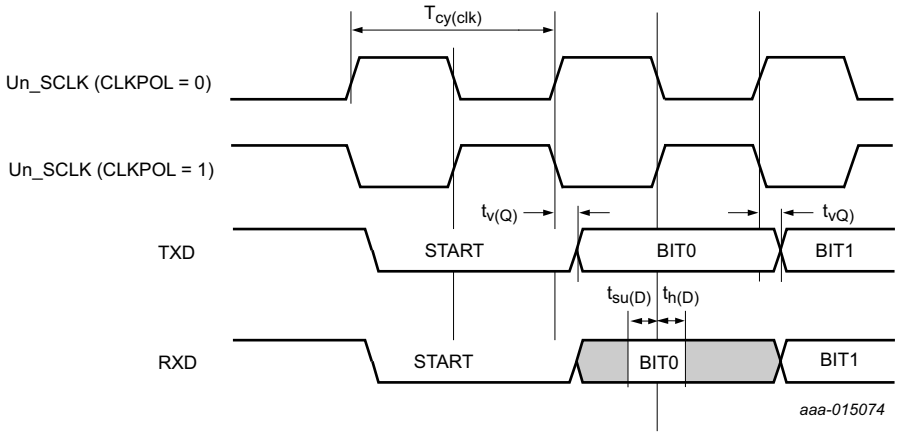
The maximum USART bit rate is 10 Mbit/s in synchronous mode master mode and 10 Mbit/s in synchronous slave mode.

**Remark:** USART functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

**Table 21. USART dynamic characteristics**

*$T_{amb}$ = −40 °C to +85 °C; 1.8 V <= $V_{DD}$ <= 3.6 V unless noted otherwise; $C_L$ = 10 pF; input slew = 10 ns. Simulated parameters sampled at the 30 %/70 % level of the falling or rising edge; values guaranteed by design.*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| **USART master (in synchronous mode)** | | | | | |
| $t_{su(D)}$ | data input set-up time | 3.0 V <= $V_{DD}$ <= 3.6 V | 31 | - | ns |
| | | 1.8 V <= $V_{DD}$ < 3.0 V | 37 | | |
| $t_{h(D)}$ | data input hold time | | 0 | - | ns |
| $t_{v(Q)}$ | data output valid time | | 0 | 5 | ns |
| **USART slave (in synchronous mode)** | | | | | |
| $t_{su(D)}$ | data input set-up time | | 6 | - | ns |
| $t_{h(D)}$ | data input hold time | | 2 | - | ns |
| $t_{v(Q)}$ | data output valid time | 3.0 V <= $V_{DD}$ <= 3.6 V | 0 | 28 | ns |
| | | 1.8 V <= $V_{DD}$ < 3.0 V | 0 | 37 | ns |




In master mode, $T_{cy(clk)}$ = U_PCLK/BRGVAL.

**Fig 36. USART timing**

# 19. Revision history

**Table 29. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| LPC83X v.1.2 | 20180404 | Product data sheet | 201804004I | LPC83X v.1.1 |
| Modifications: | • Updated table note 2 of Section 12.1 “Power-up ramp conditions”. | | | |
| LPC83X v.1.1 | 20161003 | Product data sheet | - | LPC83X v.1 |
| Modifications: | • Updated Section 2 “Features and benefits”: DMA with 18 channels and 8 trigger inputs.<br>• Updated features of Section 8.12 “DMA controller”: DMA with 18 channels and 8 trigger inputs.<br>• Added text to Table 4 “Movable functions (assign to pins PIO0_0 to PIO0_28 through switch matrix)”:<br>– SPI0_SSEL1 Slave select 0 for SPI1. Slave select 1 for SPI0.<br>– SPI0_SSEL2 Slave select 0 for SPI2. Slave select 2 for SPI0.<br>– SPI0_SSEL3 Slave select 0 for SPI3. Slave select 3 for SPI0.<br>• Changed the cross reference in the remark of Section 12.3 “External clock for the oscillator in slave mode” to Table 7 “General operating conditions”.<br>• Updated Figure 2 “HVQFN33 package marking”. Removed the number 14 from the inner block.<br>• Updated table note section 2 in Table 5 “Limiting values” to make the reference to Table 7 “General operating conditions”. | | | |
| LPC83X v.1 | 20160805 | Product data sheet | - | - |