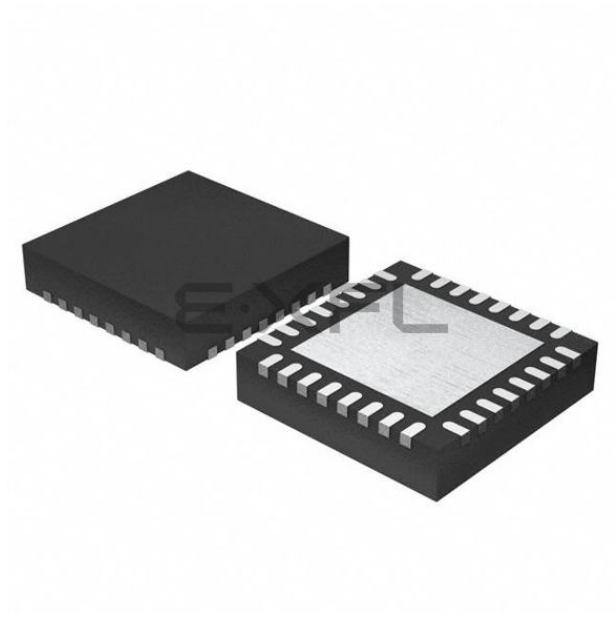

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc834m101fhi33y

8.8.1 Standard I/O pad configuration

Figure 7 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output.
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled.
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Digital input: Programmable input digital filter selectable on all pins.
- Analog input: Selected through the switch matrix.

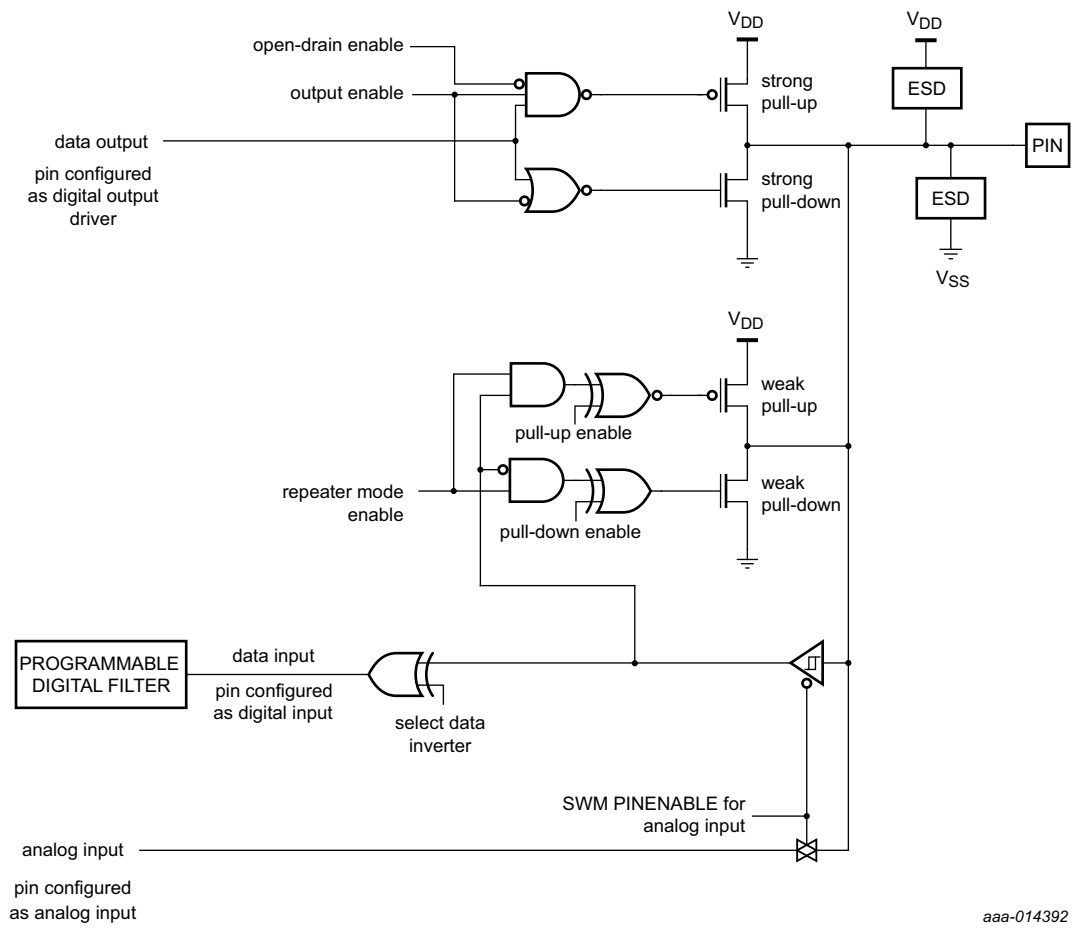


Fig 7. Standard I/O pad configuration

8.9 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, SCTimer/PWM, and I^2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 4.

Functions that need specialized pads like the oscillator pins XTALIN and XTALOUT can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Table 3. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

8.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC83x use accelerated GPIO functions:

- GPIO registers are on the ARM Cortex-M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 15 MHz.
- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and RESET/PIO0_5, the switch matrix enables the GPIO port pin function by default.

8.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to GPIO inputs with internal pull-up resistors enabled after reset - except for the I^2C-bus true open-drain pins PIO0_10 and PIO0_11.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 7).
- Direction (input/output) can be set and cleared individually.
- Pin direction bits can be toggled.

8.11 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, with software, to create complex state machines based on pin inputs.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are on the IO+ bus for fast single-cycle access.

- Eight states.
- Four inputs. Each input is configurable through an input multiplexer to use one of four external pins (connected through the switch matrix) or one of four internal sources. The maximum input signal frequency is 25 MHz.
- Six outputs. Connected to pins through the switch matrix.

- Counter/timer features:
  - Each SCTimer is configurable as two 16-bit counters or one 32-bit counter.
  - Counters can be clocked by the system clock or selected input.
  - Configurable as up counters or up-down counters.
  - Configurable number of match and capture registers. Up to eight match and capture registers total.
  - Upon match create the following events: interrupt; stop, limit, halt the timer or change counting direction; toggle outputs.
  - Counter value can be loaded into capture register triggered by a match or input/output toggle.
- PWM features:
  - Counters can be used with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to six single-edge or dual-edge PWM outputs with independent duty cycle and common PWM cycle length.
- Event creation features:
  - The following conditions define an event: a counter match condition, an input (or output) condition such as a rising or falling edge or level, a combination of match and/or input/output condition.
  - Selected events can limit, halt, start, or stop a counter or change its direction.
  - Events trigger state changes, output toggles, interrupts, and DMA transactions.
  - Match register 0 can be used as an automatic limit.
  - In bidirectional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- State control features:
  - A state is defined by events that can happen in the state while the counter is running.
  - A state changes into another state as a result of an event.
  - Each event can be assigned to one or more states.
  - State variable allows sequencing across multiple counter cycles.
- One SCTimer match output can be selected as ADC hardware trigger input.

8.16.2 SCTimer/PWM input MUX (INPUT MUX)

Each input of the SCTimer/PWM is connected to a programmable multiplexer which allows to connect one of multiple internal or external sources to the input. The available sources are the same for each SCTimer/PWM input and can be selected from four pins configured through the switch matrix, the ADC threshold compare interrupt, and the ARM core signals ARM_TXEV and DEBUG_HALTED.

- The WKT can be used for waking up the part from any reduced power mode, including Deep power-down mode, or for general-purpose timing.

8.20 Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12 bit and fast conversion rates of up to 1.2 MSamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources.

The ADC includes a hardware threshold compare function with zero-crossing detection.

Remark: For best performance, select VREFP and VREFN at the same voltage levels as V_{DD} and V_{SS}. When selecting VREFP and VREFN different from VDD and VSS, ensure that the voltage midpoints are the same:

(VREFP-VREFN)/2 + VREFN = V_{DD}/2

8.20.1 Features

- 12-bit successive approximation analog to digital converter.
- 12-bit conversion rate of up to 1.2 MSamples/s.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and zero-crossing detection.
- Power-down mode and low-power operating mode.
- Measurement range VREFN to VREFP (not to exceed V_{DD} voltage level).
- Burst conversion mode for single or multiple inputs.
- Hardware calibration mode.

its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is nominally 100 μs.

8.21.4 Clock output

The LPC83x features a clock output function that routes the IRC, the SysOsc, the watchdog oscillator, or the main clock to the CLKOUT function. The CLKOUT function can be connected to any digital pin through the switch matrix.

8.21.5 Wake-up process

The LPC83x begin operation at power-up by using the IRC as the clock source allowing chip operation to resume quickly. If the SysOsc, the external clock source, or the PLL are needed by the application, software must enable these features and wait for them to stabilize before they are used as a clock source.

8.21.6 Power control

The LPC83x supports the ARM Cortex-M0 Sleep mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing to fine-tune power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

8.21.6.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

8.21.6.2 Deep-sleep mode

In Deep-sleep mode, the LPC83x core is in Sleep mode and all peripheral clocks and all clock sources are off except for the IRC and watchdog oscillator or low-power oscillator if selected. The IRC output is disabled. In addition, all analog blocks are shut down and the flash is in standby mode. In Deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC83x can wake up from Deep-sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI, or the I2C blocks (in slave mode).

11.2 Supply pins

Table 8. Static characteristics, supply pins

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash;					
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V	[2][3][4] [6][7]	-	1.85	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][4] [6][7]	-	1.04	-	mA
		system clock = 30 MHz; default mode; V_{DD} = 3.3 V	[2][3][6] [7][9]	-	3.95	-	mA
		system clock = 30 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][6] [7][9]	-	3.2	-	mA
		Sleep mode					
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V	[2][3][4] [6][7]	-	1.35	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][4] [6][7]	-	0.8	-	mA
		system clock = 30 MHz; default mode; V_{DD} = 3.3 V	[2][3][9] [6][7]	-	2.55	-	mA
		system clock = 30 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][9] [6][7]	-	2.1	-	mA
I_{DD}	supply current	Deep-sleep mode; V_{DD} = 3.3 V; T_{amb} = 25 °C	[2][3][10]	-	158	300	µA
		T_{amb} = 85 °C		-	-	400	µA
I_{DD}	supply current	Power-down mode; V_{DD} = 3.3 V T_{amb} = 25 °C	[2][3][10]	-	1.6	10	µA
		T_{amb} = 85 °C		-	-	50	µA
I_{DD}	supply current	Deep power-down mode; V_{DD} = 3.3 V; 10 kHz low-power oscillator and self-wake-up timer (WKT) disabled T_{amb} = 25 °C	[2][11]	-	0.2	1	µA
		T_{amb} = 85 °C		-	-	4	µA

[5] V_{DD} supply voltage must be present.

[6] 3-state outputs go into 3-state mode in Deep power-down mode.

[7] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[8] Pull-up and pull-down currents are measured across the weak internal pull-up/pull-down resistors. See Figure 11.

[9] To V_{SS}.

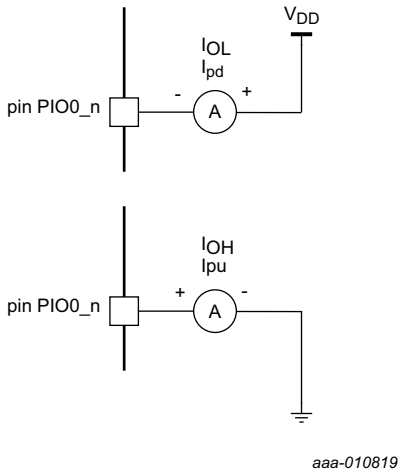
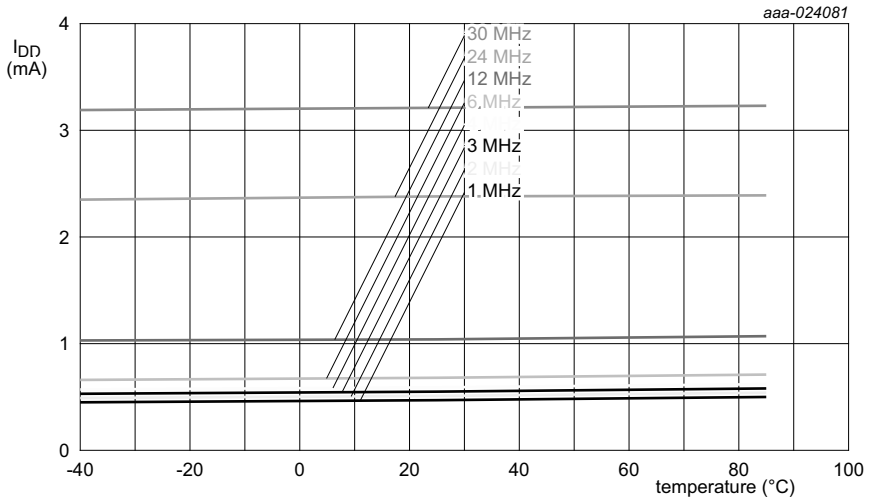


Fig 11. Pin input/output current measurement



Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL =0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

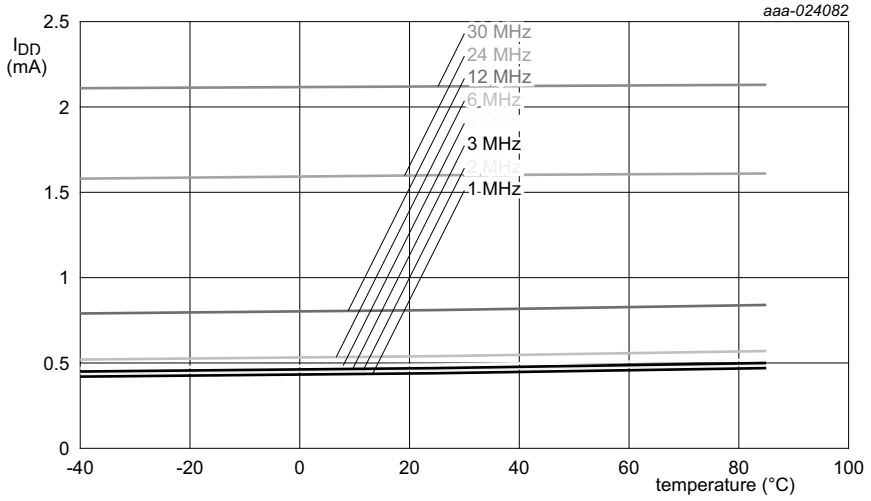
1 MHz - 6 MHz: external clock; IRC, PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz: IRC enabled; PLL enabled.

30 MHz: system oscillator enabled; PLL enabled.

Fig 13. Active mode: Typical supply current I_{DD} versus temperature



Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL =0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

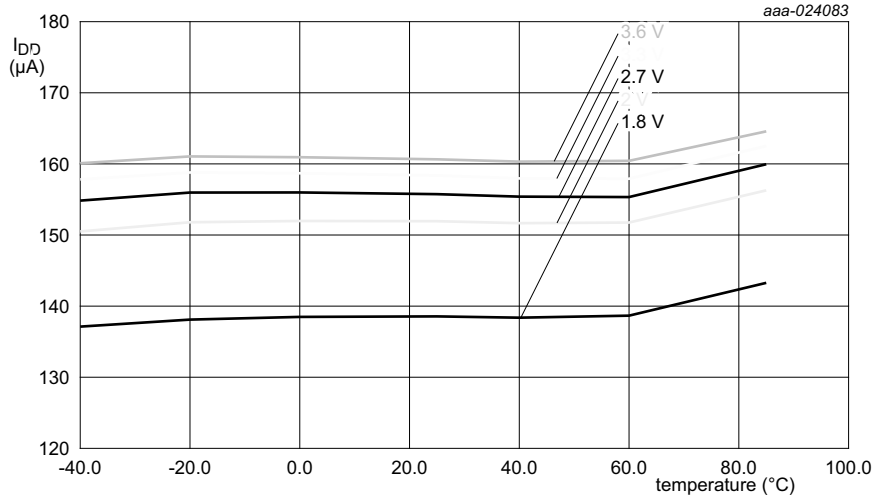
1 MHz - 6 MHz: external clock; IRC, PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz: IRC enabled; PLL enabled.

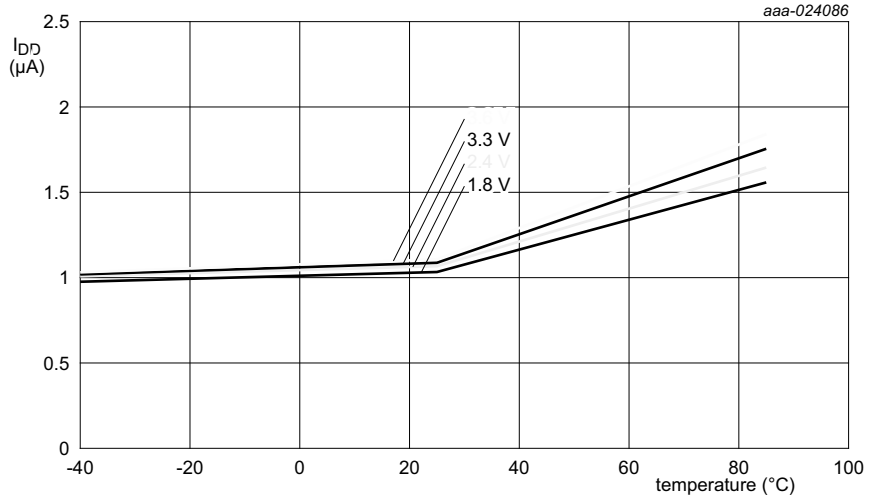
30 MHz: system oscillator enabled; PLL enabled.

Fig 14. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies



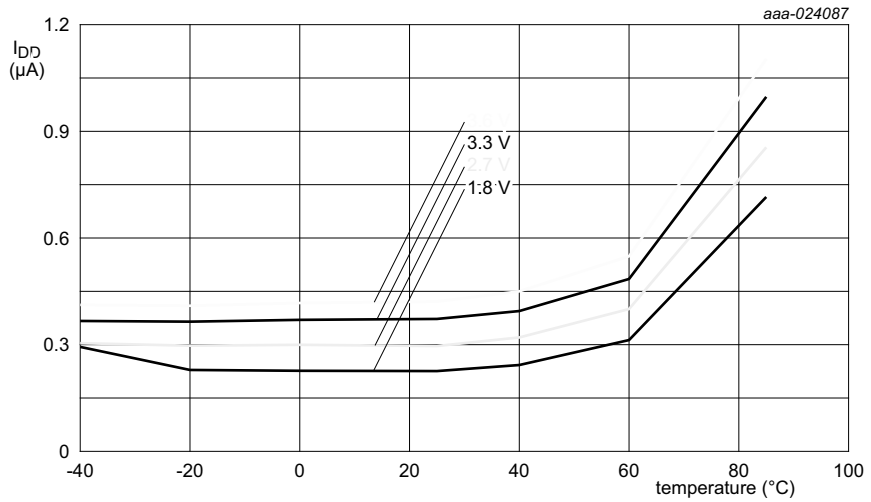
Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 15. Deep sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



WKT running with internal 10 kHz low-power oscillator.

Fig 18. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (internal clock)



WKT running with external 10 kHz clock. Clock input waveform: square wave with rise time and fall time of 5 ns.

Fig 19. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (external 10 kHz input clock)

11.6 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG. and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code accessing the peripheral is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 30 MHz.

Table 10. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in µA			Notes
	System clock frequency =			
	n/a	12 MHz	30 MHz	
IRC	261	-	-	System oscillator running; PLL off; independent of main clock frequency; IRC output disabled.
System oscillator at 12 MHz	274	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator	2	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	39	-	-	Independent of main clock frequency.
Main PLL	-	301	-	-
CLKOUT	-	67	150	Main clock divided by 4 in the CLKOUTDIV register.
ROM	-	27	68	-
GPIO + pin interrupt/pattern match	-	95	233	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
SWM	-	59	145	-
IOCON	-	45	110	-
SCTimer/PWM	-	168	411	-
MRT	-	89	220	-
WWDT	-	29	71	-
I2C0	-	54	132	-
SPI0	-	55	136	-
SPI1	-	55	136	-
USART0	-	50	124	-

Table 19. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +85 °C; values guaranteed by design.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

12.4.5 SPI interfaces

In master mode, the maximum supported bit rate is limited by the maximum system clock to 30 Mbit/s. In slave mode, assuming a set-up time of 3 ns for the external device and neglecting any PCB trace delays, the maximum supported bit rate is 1/(2 x (26 ns + 3 ns)) = 17 Mbit/s at 3.0 V <= VDD <= 3.6 V and 13 Mbit/s at 1.8 V <= VDD < 3.0 V. The actual bit rate depends on the delays introduced by the external trace and the external device.

Remark: SPI functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 20. SPI dynamic characteristics

T_{amb} = −40 °C to +85 °C; C_L = 20 pF; input slew = 1 ns. Simulated parameters sampled at the 30 % and 70 % level of the rising or falling edge; values guaranteed by design. Delays introduced by the external trace or external device are not considered.

Symbol	Parameter	Conditions	Min	Max	Unit
SPI master					
t_{DS}	data set-up time	1.8 V <= V_{DD} <= 3.6 V	2	-	ns
t_{DH}	data hold time	1.8 V <= V_{DD} <= 3.6 V	6	-	ns
$t_{v(Q)}$	data output valid time	1.8 V <= V_{DD} <= 3.6 V	-3	4	ns
SPI slave					
t_{DS}	data set-up time	1.8 V <= V_{DD} <= 3.6 V	2	-	ns
t_{DH}	data hold time	1.8 V <= V_{DD} <= 3.6 V	4	-	ns
$t_{v(Q)}$	data output valid time	3.0 V <= V_{DD} <= 3.6 V	0	26	ns
		1.8 V <= V_{DD} < 3.0 V	0	35	ns

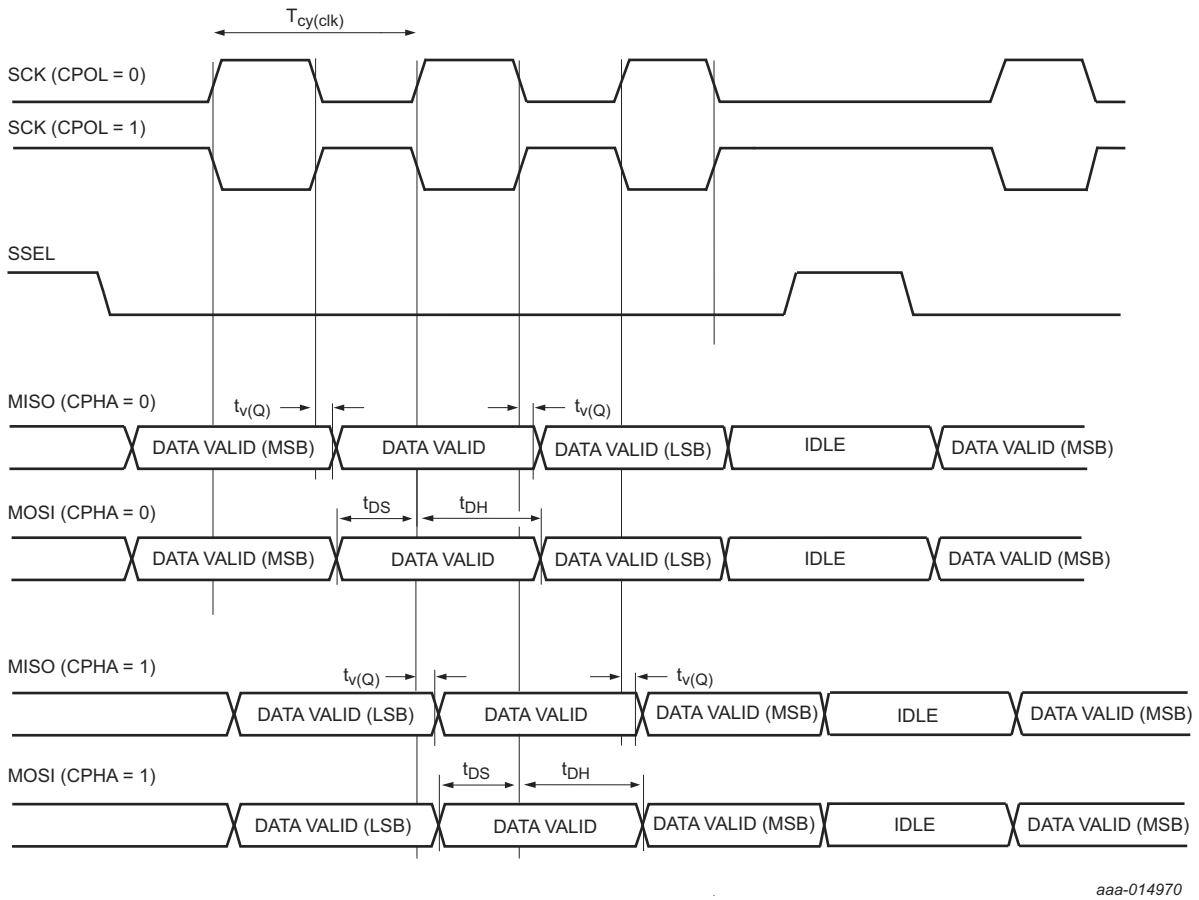


Fig 35. SPI slave timing

13.2 ADC

Table 23. 12-bit ADC static characteristics

T_{amb} = −40 °C to +85 °C unless noted otherwise; V_{DD} = 2.4 V to 3.6 V; VREFP = V_{DD}; VREFN = V_{SS}.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DD}	V
V_{ref}	reference voltage	on pin VREFP		2.4	-	V_{DD}	V
C_{ia}	analog input capacitance			-	-	0.32	pF
$f_{clk(ADC)}$	ADC clock frequency	2.7 V <= V_{DD} <= 3.6 V	[2]	-	-	30	MHz
		2.4 V <= V_{DD} < 2.7 V	[3]	-	-	25	MHz
f_s	sampling frequency	2.7 V <= V_{DD} <= 3.6 V	[2]	-	-	1.2	Msamples/s
		2.4 V <= V_{DD} < 2.7 V	[3]	-	-	1	Msamples/s
E_D	differential linearity error	T_{amb} = 85 °C	[5][4]	-	+/- 2.5	-	LSB
$E_{L(adj)}$	integral non-linearity	T_{amb} = 85 °C	[6][4]	-	+/- 2.5	-	LSB
E_O	offset error	T_{amb} = 85 °C	[7][4]	-	+/- 4.5	-	LSB
$V_{err(fs)}$	full-scale error voltage	1.2 Msamples/s; T_{amb} = 85 °C	[8][4]	-	+/- 0.5	-	%
Z_i	input impedance	f_s = 1.2 Msamples/s	[1][9] [10]	0.1	-	-	MΩ

[1] The input resistance of ADC channel 0 is higher than for all other channels. See Figure 37.

[2] In the ADC TRM register, set VRANGE = 0 (default).

[3] In the ADC TRM register, set VRANGE = 1 (default).

[4] Based on characterization. Not tested in production.

[5] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 38.

[6] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 38.

[7] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 38.

[8] The full-scale error voltage or gain error (E_G) is the difference between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 38.

[9] T_{amb} = 25 °C; maximum sampling frequency f_s = 2 Msamples/s and analog input capacitance C_{ia} = 0.1 pF.

[10] Input impedance Z_i is inversely proportional to the sampling frequency and the total input capacity including C_{ia} and C_{io}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 8 for C_{io}.

14. Application information

14.1 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended to couple the input through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

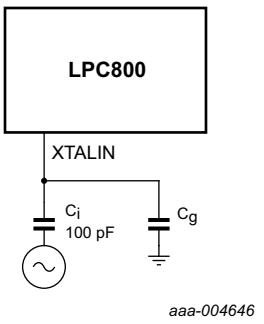


Fig 39. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled with a capacitor of 100 pF (Figure 39), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 40 and in Table 24 and Table 25. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} must be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 40 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 24).

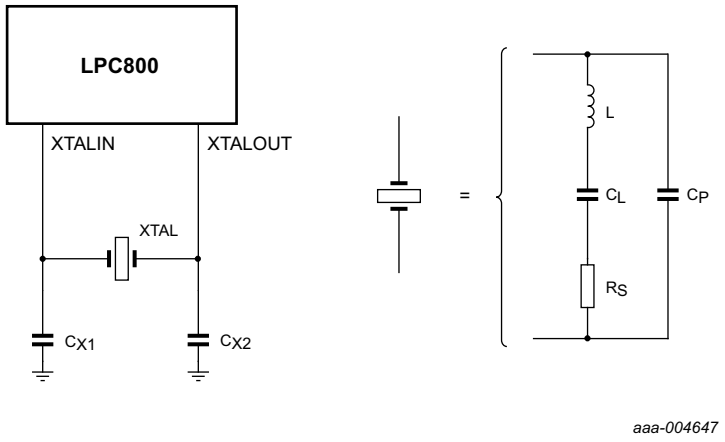


Fig 40. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 24. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 25. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

14.2 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1},C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in

17. Abbreviations

Table 28. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General-Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SMBus	System Management Bus
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

18. References

[1] I2C-bus specification *UM10204*.

[2] Technical note ADC design guidelines: http://www.nxp.com/documents/technical_note/TN00009.pdf

20. Legal information

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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