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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, POR, WDT |
| Number of I/O | 12 |
| Program Memory Size | 768B (512 x 12) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 25 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.5V ~ 15V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 20-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16hv540-04i-ss |

## 1.0 GENERAL DESCRIPTION

The PIC16HV540 from Microchip Technology is a low-cost, high-performance, 8-bit, fully-static, EPROM-based CMOS microcontroller. It is pin and software compatible with the PIC16C5X family of devices. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle except for program branches, which take two cycles. The PIC16HV540 delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly orthogonal resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy-to-use and easy-to-remember instruction set reduces development time significantly.

The PIC16HV540 is the first One-Time-Programmable (OTP) microcontroller with an on-chip 3 volt and 5 volt regulator. This eliminates the need for an external regulator in many applications powered from 9 Volt or 12 Volt batteries or unregulated 6 volt, 9 volt or 12 volt mains adapters. The PIC16HV540 is ideally suited for applications that require very low standby current at high voltages. These typically require expensive low current regulators.

The PIC16HV540 is equipped with special features that reduce system cost and power requirements. The Power-On Reset (POR) and Device Reset Timer (DRT) eliminate the need for external reset circuitry. There are four oscillator configurations to choose from, including the power-saving LP (Low Power) oscillator, cost saving RC oscillator, and XT and HS for crystal oscillators. Power saving SLEEP mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The UV erasable CERDIP packaged versions are ideal for code development, while the cost-effective OTP versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers, while benefiting from the OTP's flexibility.

The PIC16HV540 is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer, and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

### 1.1 Applications

The PIC16HV540 fits in low-power battery applications such as CO and smoke detection, toys, games, security systems and automobile modules. The EPROM technology makes customizing of application programs (transmitter codes, receiver frequencies, etc.) extremely fast and convenient. The small footprint package, for through hole or surface mounting, make this microcontroller suitable for applications with space limitations. Low-cost, low-power, high-performance, ease of use and I/O flexibility make the PIC16HV540 very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, coprocessor applications).

### 1.2 Enhanced Features

#### 1.2.1 REGULATED I/O PORTA INDEPENDENT OF CORE REGULATOR

PORTA I/O pads and OSC2 output are powered by the regulated internal voltage $V_{IO}$. A maximum of 10mA per output is allowed, or a total of 40mA. The core itself is powered from the independently regulated supply $V_{REG}$.

#### 1.2.2 HIGH VOLTAGE I/O PORTB

All eight PORTB I/Os are high voltage I/O. The inputs will tolerate input voltages as high as the $V_{DD}$ and outputs will swing from $V_{SS}$ to the $V_{DD}$. The input threshold voltages vary with supply voltage. (See Electrical Characteristics.)

#### 1.2.3 WAKE-UP ON PIN CHANGE ON PORTB [0:3]

Four of the PORTB inputs latch the status of the pin at the onset of sleep mode. A level change on the inputs resets the device, implementing wake up on pin change (via warm reset). The $\overline{\text{PCWUF}}$ bit in the status register is reset to indicate that a pin change caused the reset condition. Any pin change (glitch insensitive) of the opposite level of the initial value wakes up the device. This option can be enabled/disabled in OPTION2 register. (See OPTION2 Register, Register 4-3.)

#### 1.2.4 WAKE-UP ON PIN CHANGE WITH A SLOWLY-RISING VOLTAGE ON PORTB [7]

PORTB [7] also implements wake up from sleep, however this input is specifically adapted so that a slowly **rising** voltage does not cause excessive power consumption. This input can be used with external RC circuits for long sleep periods without using the internal timer and prescaler. This option is also enabled/disabled in OPTION2 register. (The enable/disable bit is shared with the other 4 wake-up inputs.) The $\overline{\text{PCWUF}}$ bit in the status register is also shared with the other four wake-up inputs.

#### 1.2.5 LOW-VOLTAGE (BROWN-OUT) DETECTION

A low voltage (Brown-out) detect circuit optionally resets the device at a voltage level higher than that at which the PICmicro® device stops operating. The nominal trip voltages are 3.1 volts (for 5 volt operation) and 2.2 volt (for 3 volt operation), respectively. The core remains in the reset state as long as this condition holds (as if a $\overline{\text{MCLR}}$ external reset was given). The Brown-out trip level is user selectable, with built-in interlocks. The Brown-out detector is disabled at power-up and is activated by clearing the appropriate bit ($\overline{\text{BODEN}}$) in OPTION2 register.

### 1.2.6 INCREASED STACK DEPTH

The stack depth is 4 levels to allow modular program implementation by using functions and subroutines.

### 1.2.7 ENHANCED WATCHDOG TIMER (WDT) OPERATION

The WDT is enabled by setting FUSE 2 in the configuration word. The WDT setting is latched and the fuse disabled during SLEEP mode to reduce current consumption.

If the WDT is disabled by FUSE 2, it can be enabled/disabled under program control using bit 4 in OPTION2 Register (SWDTEN). The software WDT control is disabled at power-up.

The current consumption of the on-chip oscillator (used for the watchdog, oscillator startup timer and sleep timer) is less than 1μA (typical) at 3 Volt operation.

### 1.2.8 REDUCED EXTERNAL RC OSCILLATOR STARTUP TIME

If the RC oscillator option is selected in the Configuration word (FOSC1=1 and FOSCO=1), the oscillator startup time is 1.0 ms nominal instead of 18 ms nominal. This is applicable after power-up (POR), either WDT interrupt or wake-up, external reset on MCLR, PCWU (wake on pin change) and Brown-out.

### 1.2.9 LOW-VOLTAGE OPERATION OF THE ENTIRE CPU DURING SLEEP

The voltage regulator can automatically lower the voltage to the core from 5 Volt to 3 Volt during sleep, resulting in reduced current consumption. This is an option bit (SL) in the OPTION2 register.

### 1.2.10 GLITCH FILTERS ON WAKE-UP PINS AND MCLR

Glitch sensitive inputs for wake-up on pin change are filtered to reduce susceptibility to interference. A similar filter reduces false reset on MCLR.

### 1.2.11 PROGRAMMABLE CLOCK GENERATOR

When used in RC mode, the CLKOUT pin can be used as a programmable clock output. The output is connected to TMR0, bit 0 and by setting the prescaler, clock out frequencies of CLKIN/8 to CLKIN/1024 can be generated. The CLKOUT pin can also be used as a general purpose output by modifying TMR0, bit 0.

**TABLE 1-1: PIC16HV540 DEVICE**

| | | PIC16HV540 |
|---|---|---|
| **Clock** | Maximum Frequency (MHz) | 20 |
| **Memory** | EPROM Program Memory | 512 |
| | RAM Data Memory (bytes) | 25 |
| **Peripherals** | Timer Module(s) | TMR0 |
| **Packages** | I/O Pins | 12 |
| | Voltage Range (Volts) | 3.5V-15V |
| | Number of Instructions | 33 |
| | Packages | 18-pin DIP<br>SOIC<br>20-pin SSOP |

All PICmicro® devices have Power-on Reset, selectable WDT, selectable code protect and high I/O current capability.

### 4.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bits for program memories larger than 512 words.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable while the $\overline{PCWUF}$ bit is a read/write bit. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS register because these instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions, which do affect STATUS bits, see Section 8.0, Instruction Set Summary.

**REGISTER 4-1: STATUS REGISTER (ADDRESS:03h)**

| R/W-0 | R/W-0 | R/W-0 | R-1 | R-1 | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| $\overline{PCWUF}$ | PA1 | PA0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C |
| bit7 | | | | | | | bit0 |

R = Readable bit
W = Writable bit
- n = Value at POR reset

bit 7: **$\overline{PCWUF}$**: Pin Change Reset bit
1 = After Power-up Reset (POR) or SLEEP command
0 = After a wake-up on pin change event

bit 6-5: **Not Applicable**

bit 4: **$\overline{TO}$**: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: **$\overline{PD}$**: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (for `ADDWF` and `SUBWF` instructions)
**ADDWF**
1 = A carry from the 4th low order bit of the result occurred
0 = A carry from the 4th low order bit of the result did not occur
**SUBWF**
1 = A borrow from the 4th low order bit of the result did not occur
0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C**: Carry/$\overline{borrow}$ bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)

| **ADDWF** | **SUBWF** | **RRF or RLF** |
|---|---|---|
| 1 = A carry occurred | 1 = A borrow did not occur | Load bit with LSb or MSb, respectively |
| 0 = A carry did not occur | 0 = A borrow occurred | |

## 4.4 OPTION Register

The OPTION register is a 6-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the OPTION instruction, the contents of the W register will be transferred to the OPTION register. A RESET sets the OPTION<5:0> bits.

Example 4-1 illustrates how to initialize the OPTION register.

**EXAMPLE 4-1: INSTRUCTIONS FOR INITIALIZING OPTION REGISTER**

```
movlw   '0000 0111'b   ; load OPTION setup value into W
OPTION                 ; initialize OPTION register
```

**REGISTER 4-2: OPTION REGISTER**

| U-0 | U-0 | W-1 | W-1 | W-1 | W-1 | W-1 | W-1 |
|---|---|---|---|---|---|---|---|
| — | — | T0CS | T0SE | PSA | PS2 | PS1 | PS0 |
| bit7 | | | | | | | 0 |

W = Writable bit
U = Unimplemented bit
- n = Value at POR reset

bit 7-6: **Unimplemented**

bit 5: **T0CS**: Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3: **PSA**: Prescaler Assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0: **PS<2:0>**: Prescaler Rate Select bits

| Bit Value | Timer0 Rate | WDT Rate |
|---|---|---|
| 000 | 1 : 2 | 1 : 1 |
| 001 | 1 : 4 | 1 : 2 |
| 010 | 1 : 8 | 1 : 4 |
| 011 | 1 : 16 | 1 : 8 |
| 100 | 1 : 32 | 1 : 16 |
| 101 | 1 : 64 | 1 : 32 |
| 110 | 1 : 128 | 1 : 64 |
| 111 | 1 : 256 | 1 : 128 |

## 4.5 OPTION2 Register

The OPTION2 register is a 6-bit wide, write-only register which contains various control bits to configure the added features on the PIC16HV540. A Power-on Reset sets the OPTION2<5:0> bits.

Example 4-2 illustrates how to initialize the OPTION2 register.

| **Note:** | All Power-on Resets will disable the Brown-out Detect circuit. All subsequent resets will not disable the Brown-out Detect if enabled. |
|---|---|

**EXAMPLE 4-2: INSTRUCTIONS FOR INITIALIZING OPTION2 REGISTER**

```
movlw    '0001 0111'b   ; load OPTION2 setup value into W
tris     0x07            ; initialize OPTION2 register
```

**REGISTER 4-3: OPTION2 REGISTER (TRIS 07H)**

| U-0 | U-0 | W-1 | W-1 | W-1 | W-1 | W-1 | W-1 |
|---|---|---|---|---|---|---|---|
| — | — | $\overline{\text{PCWU}}$ | $\overline{\text{SWDTEN}}$ | RL | SL | BODL | $\overline{\text{BODEN}}$ |
| bit7 | | | | | | | 0 |

W = Writable bit
U = Unimplemented bit
- n = Value at POR reset

bit 7-6: **Unimplemented**

bit 5: **$\overline{\text{PCWU}}$**: Wake-up on Pin Change
1 = Disabled
0 = Enabled

bit 4: **$\overline{\text{SWDTEN}}$**: Software Controlled WDT Enable bit
1 = WDT is turned off it the WDTEN configuration bit = 0
0 = WDT is on if the WDTEN configuration bit = 0; if WDTEN bit = 1, then SWDTEN is 'don't care'

bit 3: **RL**: Regulated Voltage Level Select bit
1 = 5 volt
0 = 3 volt

bit 2: **SL:** Sleep Voltage Level Select bit
1 = **RL** bit setting
0 = 3 volt

bit 1: **BODL**: Brown-out Voltage Level Select bit
1 = **RL** bit setting, but **SL** during SLEEP
0 = 3 volt

bit 0: **$\overline{\text{BODEN}}$**: Brown-out Enabled
1 = Disabled
0 = Enabled

**NOTES:**

## 6.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT) (WDT postscaler not implemented on PIC16C52), respectively (Section 6.1.2). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x`, etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

### 6.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on the fly” during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

**EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)**

```
1. CLRWDT                ;Clear WDT
2. CLRF     TMR0         ;Clear TMR0 & Prescaler
3. MOVLW    '00xx1111'b  ;These 3 lines (5, 6, 7)
4. OPTION                ; are required only if
                         ; desired
5. CLRWDT                ;PS<2:0> are 000 or 001
6. MOVLW    '00xx1xxx'b  ;Set Postscaler to
7. OPTION                ; desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A `CLRWDT` instruction should be executed before switching the prescaler.

**EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)**

```
CLRWDT                   ;Clear WDT and
                         ;prescaler
MOVLW   'xxxx0xxx'       ;Select TMR0, new
                         ;prescale value and
                         ;clock source
OPTION
```

## 6.3 Programmable Clock Generator

When the PIC16HV540 is programmed to operate in the RC oscillator mode, the CLKOUT pin is connected to the compliment state of TMR0<0>. Use of the prescaler rate select bits PSA:PS0 in the OPTION register will provide for frequencies of CLKIN/8 to CLKIN/1024 on the CLKOUT pin.

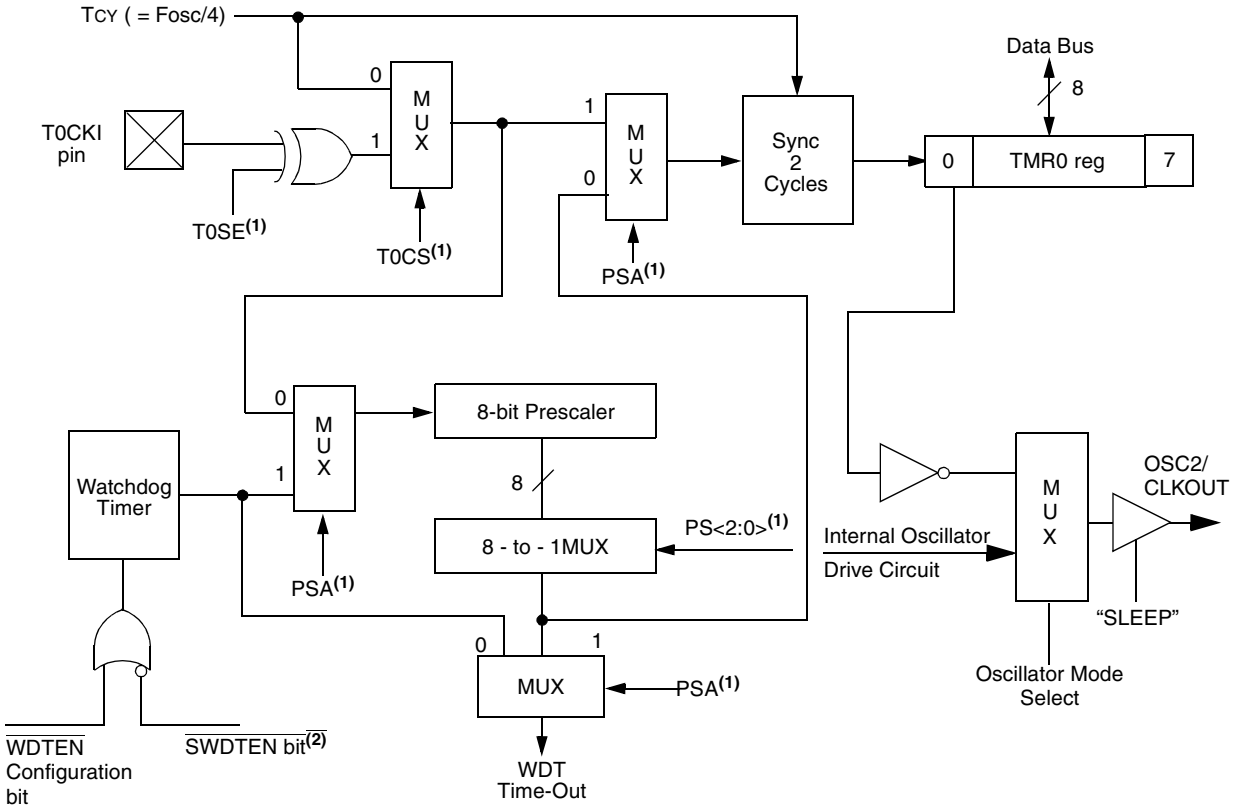
**EXAMPLE 6-3:**

| Fosc | PRESCALER SETTING/CLKOUT FREQUENCY | |
|---|---|---|
| | CLKIN/1024 | CLKIN/8 |
| 1Mhz | 976 Hz | 125 kHz |
| 2Mhz | 1953 Hz | 250 kHz |
| 3Mhz | 2930 Hz | 375 kHz |
| 4Mhz | 3906 Hz | 500 kHz |

In addition to this mode of operation, TMR0<0> can be toggled via the bcf and bsf bit type instructions. For this mode, the T0CS bit in the OPTION register must be set to 1. This setting configures TMR0 to increment on the T0CKI pin. To set the CLKOUT pin high, a bcf TMR0,0 instruction is used and to set the CLKOUT pin low, the bsf TMR0,0 instruction is used. The T0CKI pin should be pulled high or low to prevent false state changes on the CLKOUT pin.

**FIGURE 6-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER**




**Note 1:** T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

**2:** $\overline{\text{SWDTEN}}$ is a bit in the OPTION2 register.

## 7.2 Oscillator Configurations

### 7.2.1 OSCILLATOR TYPES

The PIC16HV540 can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

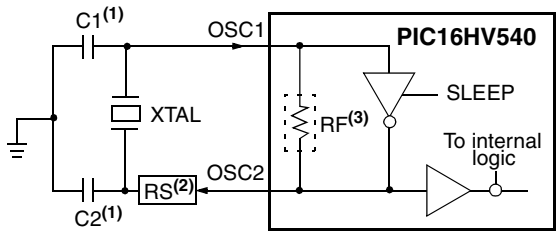
- LP: Low Power Crystal
- XT: Crystal/Resonator
- HS: High Speed Crystal/Resonator
- RC: Resistor/Capacitor

| | |
|---|---|
| **Note:** | Not all oscillator selections available for all parts. See Section 7.1. |

### 7.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 7-1). The PIC16HV540 oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source drive the OSC1/CLKIN pin (Figure 7-2).

**FIGURE 7-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)**




**Note 1:** See Capacitor Selection tables for recommended values of C1 and C2.
**2:** A series resistor (RS) may be required for AT strip cut crystals.
**3:** RF varies with the crystal chosen (approx. value = 10 MΩ).

**FIGURE 7-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)**

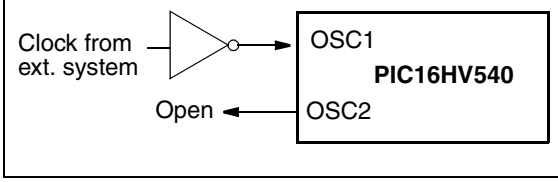



**TABLE 7-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC16HV540**

| Osc Type | Resonator Freq | Cap. Range C1 | Cap. Range C2 |
|---|---|---|---|
| XT | 455 kHz<br>2.0 MHz<br>4.0 MHz | 68-100 pF<br>15-33 pF<br>10-22 pF | 68-100 pF<br>15-33 pF<br>10-22 pF |
| HS | 8.0 MHz<br>16.0 MHz | 10-22 pF<br>10 pF | 10-22 pF<br>10 pF |

**Note:** These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

**TABLE 7-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC16HV540**

| Osc Type | Resonator Freq | Cap.Range C1 | Cap. Range C2 |
|---|---|---|---|
| LP | 32 kHz(1) | 15 pF | 15 pF |
| XT | 100 kHz<br>200 kHz<br>455 kHz<br>1 MHz<br>2 MHz<br>4 MHz | 15-30 pF<br>15-30 pF<br>15-30 pF<br>15-30 pF<br>15 pF<br>15 pF | 200-300 pF<br>100-200 pF<br>15-100 pF<br>15-30 pF<br>15 pF<br>15 pF |
| HS | 4 MHz<br>8 MHz<br>20 MHz | 15 pF<br>15 pF<br>15 pF | 15 pF<br>15 pF<br>15 pF |

**Note 1:** For $V_{DD}$ > 4.5V, C1 = C2 ≈ 30 pF is recommended.
**2:** These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

| | |
|---|---|
| **Note:** | If you change from this device to another device, please verify oscillator characteristics in your application. |

### 7.11 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

| | |
|---|---|
| **Note:** | Microchip does not recommend code protecting windowed devices. |

### 7.12 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

| | |
|---|---|
| **Note:** | Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code. |

## 8.0 INSTRUCTION SET SUMMARY

Each PIC16HV540 instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type, and one or more operands which further specify the operation of the instruction. The PIC16HV540 instruction set summary in Table 8-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 8-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

**TABLE 8-1: OPCODE FIELD DESCRIPTIONS**

| Field | Description |
|---|---|
| f | Register file address (0x00 to 0x7F) |
| W | Working register (accumulator) |
| b | Bit address within an 8-bit file register |
| k | Literal field, constant data or label |
| x | Don't care location (= 0 or 1)<br>The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools. |
| d | Destination select;<br>d = 0 (store result in W)<br>d = 1 (store result in file register 'f')<br>Default is d = 1 |
| label | Label name |
| TOS | Top of Stack |
| PC | Program Counter |
| WDT | Watchdog Timer Counter |
| TO | Time-Out bit |
| PD | Power-Down bit |
| dest | Destination, either the W register or the specified register file location |
| [ ] | Options |
| ( ) | Contents |
| → | Assigned to |
| < > | Register bit field |
| ∈ | In the set of |
| italics | User defined term (font is courier) |

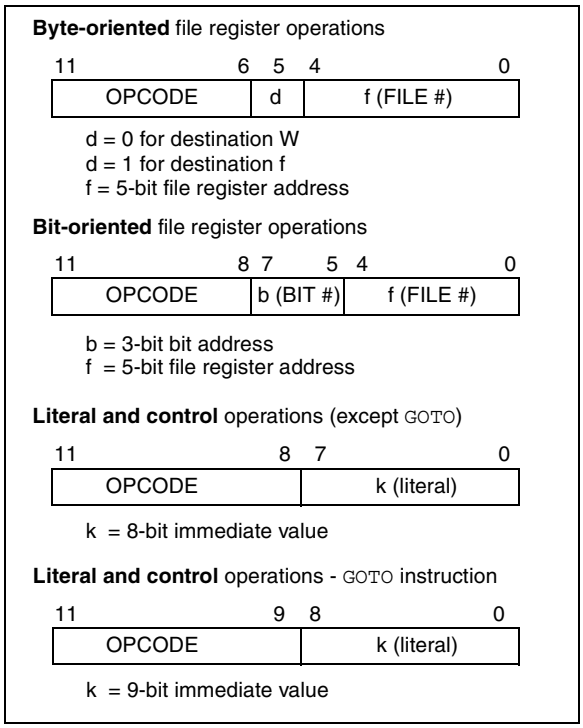
All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Figure 8-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

**FIGURE 8-1: GENERAL FORMAT FOR INSTRUCTIONS**



**ADDWF** **Add W and f**

Syntax: [ *label* ] ADDWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) + (f) → (dest)

Status Affected: C, DC, Z

Encoding:

| | | |
|---|---|---|
| 0001 | 11df | ffff |

Description: Add the contents of the W register and register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
ADDWF   FSR, 0
```
Before Instruction
W = 0x17
FSR = 0xC2
After Instruction
W = 0xD9
FSR = 0xC2

**ANDLW** **And literal with W**

Syntax: [ *label* ] ANDLW k

Operands: $0 \le k \le 255$

Operation: (W).AND. (k) → (W)

Status Affected: Z

Encoding:

| | | |
|---|---|---|
| 1110 | kkkk | kkkk |

Description: The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
ANDLW   0x5F
```
Before Instruction
W = 0xA3
After Instruction
W = 0x03

**ANDWF** **AND W with f**

Syntax: [ *label* ] ANDWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) .AND. (f) → (dest)

Status Affected: Z

Encoding:

| | | |
|---|---|---|
| 0001 | 01df | ffff |

Description: The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
ANDWF   FSR,    1
```
Before Instruction
W = 0x17
FSR = 0xC2
After Instruction
W = 0x17
FSR = 0x02

**BCF** **Bit Clear f**

Syntax: [ *label* ] BCF f,b

Operands: $0 \le f \le 31$
$0 \le b \le 7$

Operation: 0 → (f<b>)

Status Affected: None

Encoding:

| | | |
|---|---|---|
| 0100 | bbbf | ffff |

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example:
```
BCF     FLAG_REG,  7
```
Before Instruction
FLAG_REG = 0xC7
After Instruction
FLAG_REG = 0x47

**SLEEP** **Enter SLEEP Mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT;
0 → WDT prescaler;
1 → $\overline{TO}$;
0 → $\overline{PD}$
1→ $\overline{PCWUF}$

Status Affected: $\overline{TO}$, $\overline{PD}$, $\overline{PCWUF}$

Encoding:

| | | |
|---|---|---|
| 0000 | 0000 | 0011 |

Description: Time-out status bit ($\overline{TO}$) is set. The power down status bit ($\overline{PD}$) is cleared. The WDT and its prescaler are cleared.

The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.

Words: 1

Cycles: 1

Example:
```
SLEEP
```

**SUBWF** **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – (W) → (dest)

Status Affected: C, DC, Z

Encoding:

| | | |
|---|---|---|
| 0000 | 10df | ffff |

Description: Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example 1:
```
SUBWF   REG1, 1
```
Before Instruction
```
REG1    =   3
W       =   2
C       =   ?
```
After Instruction
```
REG1    =   1
W       =   2
C       =   1     ; result is positive
```
Example 2:

Before Instruction
```
REG1    =   2
W       =   2
C       =   ?
```
After Instruction
```
REG1    =   0
W       =   2
C       =   1     ; result is zero
```
Example 3:

Before Instruction
```
REG1    =   1
W       =   2
C       =   ?
```
After Instruction
```
REG1    =   FF
W       =   2
C       =   0     ; result is negative
```

## 10.0 ELECTRICAL CHARACTERISTICS - PIC16HV540

**Absolute Maximum Ratings†**

Ambient temperature under bias ..... –20°C to +85°C

Storage temperature ..... –65°C to +150°C

Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... 0 to +16V

Voltage on $\overline{MCLR}$ with respect to $V_{SS}$ ..... 0 to +14V

Voltage on all other pins with respect to $V_{SS}$ ..... –0.6V to ($V_{DD}$ + 0.6V)

Total power dissipation(1) ..... 800 mW

Max. current out of $V_{SS}$ pin ..... 150 mA

Max. current into $V_{DD}$ pin ..... 100 mA

Max. current into an input pin (T0CKI only) ..... ±500 µA

Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) ..... ±20 mA

Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DD}$) ..... ±20 mA

Max. output current sunk by any I/O pin ..... 25 mA

Max. output current sourced by any I/O pin ..... 10 mA

Max. output current sourced by a single I/O port A or B ..... 40 mA

Max. output current sourced by a single I/O port A or B ..... 50 mA

**Note 1:** Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

**2:** Voltage spikes below $V_{SS}$ at the $\overline{MCLR}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to $V_{SS}$.

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## 10.2 DC Characteristics: PIC16HV540-04, 20 (Commercial) PIC16HV540-04I, 20I (Industrial)

| DC Characteristics<br>All Pins Except<br>Power Supply Pins | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C (commercial)<br>–40°C ≤ TA ≤ +85°C (industrial) | | | | |
|---|---|---|---|---|---|---|
| **Characteristic** | **Sym.** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| **Input Low Voltage** | VIL | | | | | |
| I/O Ports PORTA | | VSS | — | 0.10 VREG | V | Pin at Hi-impedance |
| $\overline{MCLR}$ (Schmitt Trigger) | | VSS | — | 0.10 VREG | V | |
| T0CKI (Schmitt Trigger) | | VSS | — | 0.10 VREG | V | |
| OSC1 (Schmitt Trigger) | | VSS | — | 0.10 VREG | V | RC option only(4) |
| OSC1 | | VSS | — | 0.3 VREG | V | HS, XT, and LP options |
| I/O Ports PORTB | | VSS | — | 0.10 VREG | V | |
| **Input High Voltage** | VIH | | | | | |
| I/O Ports PORTA | | 0.25 VREG+0.8V | — | VREG | V | For all VREG |
| $\overline{MCLR}$ (Schmitt Trigger) | | 0.85 VREG | — | VDD | V | |
| T0CKI (Schmitt Trigger) | | 0.85 VREG | — | VDD | V | |
| OSC1 (Schmitt Trigger) | | 4.5V | — | VDD | V | RC option only (VDD = 15V)(4) |
| OSC1 | | 4.5V | — | VDD | V | HS, XT, and LP options (VDD = 15V) |
| I/O Ports PORTB | | 0.25 VREG+0.8V | — | VDD | V | |
| Hysteresis of Schmitt Trigger inputs | VHYS | 0.15 VREG* | — | — | V | |
| **Input Leakage Current(3)** | IIL | | | | | |
| I/O Ports PORTA | | -1.0 | 0.5 | +1.0 | µA | VSS ≤ VPIN ≤ VIO, Pin at Hi-impedance |
| I/O Ports PORTB | | -1.0 | 0.5 | +1.0 | µA | VSS ≤ VPIN ≤ VDD |
| $\overline{MCLR}$ | | -5.0 | | +5.0 | µA | VPIN = VSS +0.25V(2) |
| | | | 0.5 | +3.0 | µA | VPIN = VDD(2) |
| T0CKI | | -3.0 | 0.5 | +3.0 | µA | VSS ≤ VPIN ≤ VDD |
| OSC1 | | -3.0 | 0.5 | +3.0 | µA | VSS ≤ VPIN ≤ VDD, HS, XT, and LP options |
| **Output Low Voltage** | VOL | | | | | |
| I/O Ports PORTA | | — | — | 0.6 | V | VDD = 15V, VREG = 5V, IOL = 8.7 mA |
| | | | | | | VDD = 15V, VREG = 3V, IOL = 5.0 mA |
| OSC2/CLKOUT | | — | — | 0.6 | V | VDD = 15V, VREG = 5V, IOL = 1.2 mA, (RC option only) |
| | | | | | | VDD = 15V, VREG = 3V, IOL = 1.0 mA, (RC option only) |
| I/O Ports PORTB | | — | — | 0.6 | V | VDD = 15V, VREG = 5V, IOL = 3.0 mA |
| | | | | | | VDD = 10V, VREG = 3V, IOL = 3.0 mA |
| **Output High Voltage** | VOH | | | | | |
| I/O ports(3) PORTA | | VREG-0.7 | — | — | V | VDD = 15V, VIO = 3V, IOH = -2.0 mA |
| | | | | | | VDD = 15V, VIO = 5V, IOH = -3.0 mA |
| OSC2/CLKOUT | | VREG-0.7 | — | — | V | VDD = 15V, VIO = 3V, IOH = -0.5 mA (RC option only) |
| | | | | | | VDD = 15V, VIO = 5V, IOH = -1.0 mA (RC option only) |
| I/O Ports PORTB | | VDD-0.7 | — | — | V | VDD = 15V, VIO = 5V, IOH = -5.4 mA |
| **Threshold Voltage** | | | | | | |
| I/O Ports PORTB [7] | VLEV | VDD-1.5 | VDD-1.0 | VDD-0.5 | V | VDD = 15V |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**2:** The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**3:** Negative current is defined as coming out of the pin.

**4:** For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16HV540 be driven with external clock in RC mode.

## 11.0 DC AND AC CHARACTERISTICS - PIC16HV540

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean – 3σ) respectively, where σ is standard deviation.

**FIGURE 11-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE**

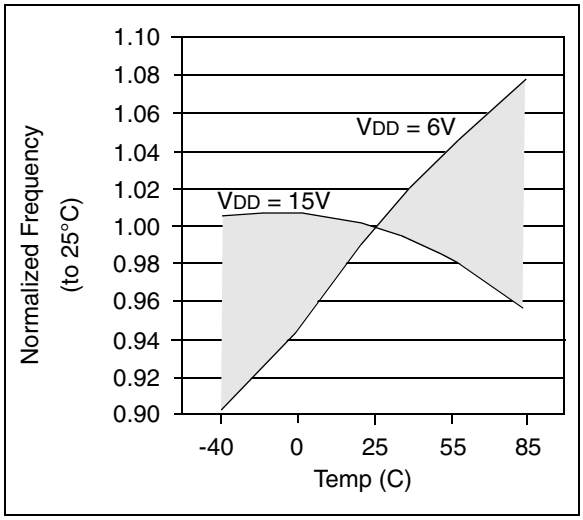



**TABLE 11-1: RC OSCILLATOR FREQUENCIES**

| CEXT | REXT | Average FOSC, VIO = 5V | |
|---|---|---|---|
| | | 25°C, VDD = 6V | 25°C, VDD = 15V |
| 20 pF | 3.3k | 4986.7 kHz | **(1)** |
| | 5k | 4233.3 kHz | **(1)** |
| | 10k | 2656.7 kHz | 5150.0 kHz |
| | 24k | 1223.3 kHz | 3286.7 kHz |
| | 100k | 325.7 kHz | 955.7 kHz |
| | 390k | 79.0 kHz | 250.7 kHz |
| 100 pF | 3.3k | 1916.7 kHz | **(1)** |
| | 5k | 1593.3 kHz | **(1)** |
| | 10k | 995.7 kHz | 2086.7 kHz |
| | 24k | 448.3 kHz | 1210.0 kHz |
| | 100k | 116.0 kHz | 355.7 kHz |
| | 390k | 28.3 kHz | 89.7 kHz |
| 300 pF | 3.3k | 744 kHz | **(1)** |
| | 5k | 620.3 kHz | **(1)** |
| | 10k | 382.0 kHz | 817.3 kHz |
| | 24k | 169.7 kHz | 483.0 kHz |
| | 100k | 44.1 kHz | 135.7 kHz |
| | 390k | 10.6 kHz | 34.4 kHz |

**Note 1:** This combination of R, C and VDD draws too much current and prohibits oscillator operation.

**FIGURE 11-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD (CEXT = 20pF)**

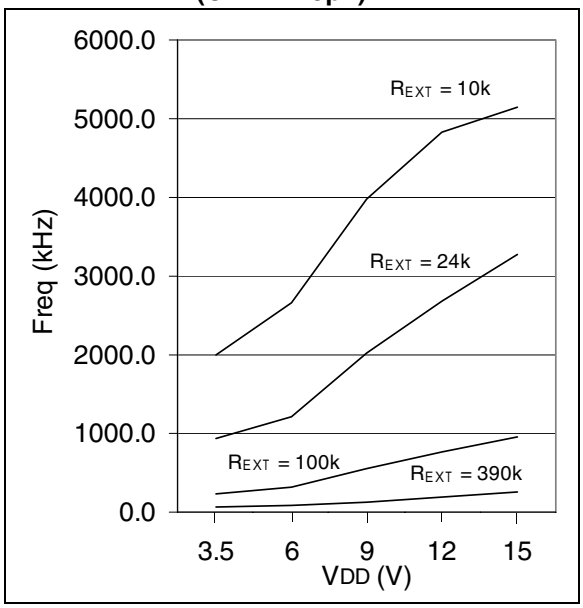



**FIGURE 11-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD (CEXT = 100pF)**

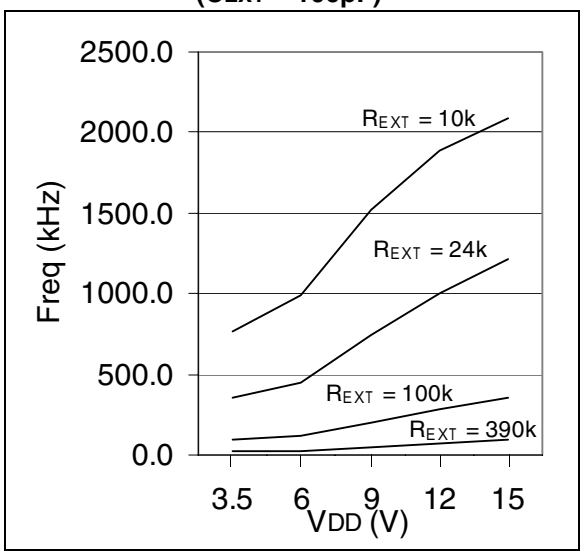


**FIGURE 11-10: MAXIMUM IPD vs. VDD, WATCHDOG TIMER DISABLED (VIO = 3V)**

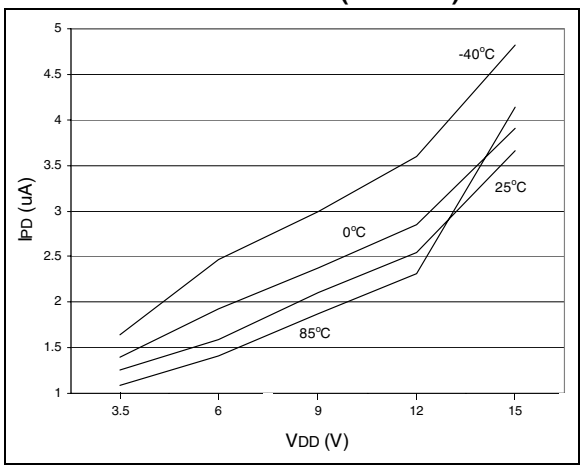



**FIGURE 11-11: TYPICAL IPD vs. VDD, WATCHDOG TIMER ENABLED (VIO = 3V)**

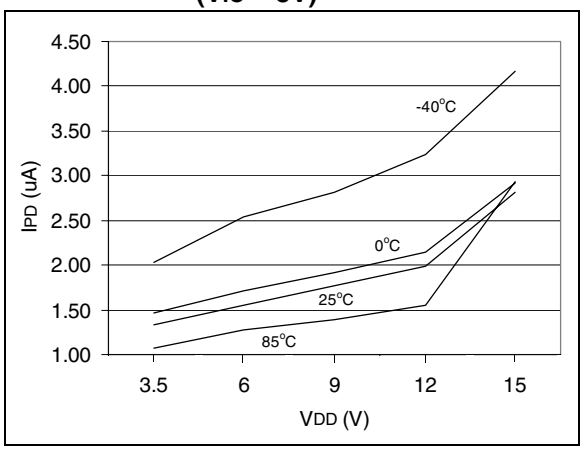



**FIGURE 11-12: MAXIMUM IPD vs. VDD, WATCHDOG TIMER ENABLED (VIO = 3V)**

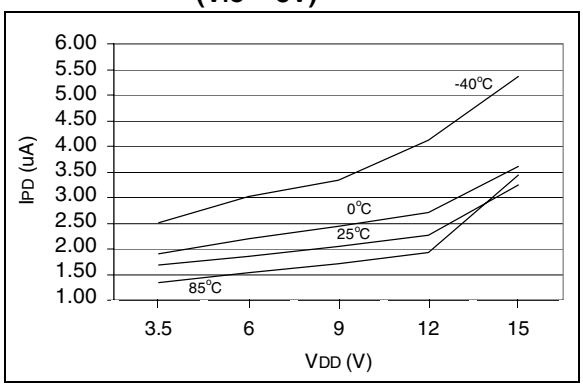



**FIGURE 11-13: MAXIMUM IDD vs. FREQUENCY, WATCHDOG TIMER DISABLED, RC MODE (VDD = 15V, VIO = 5V, -40°C TO +85°C)**

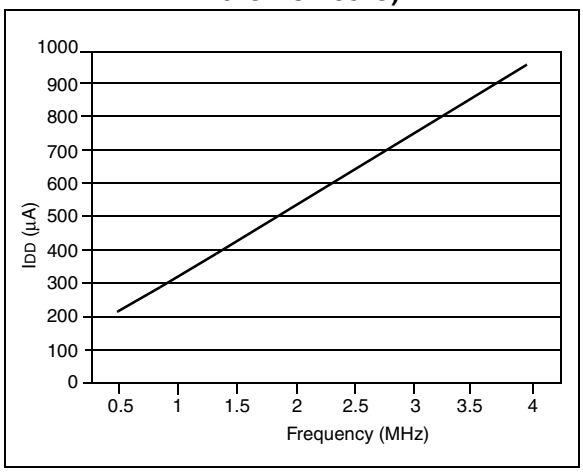



**FIGURE 11-14: MAXIMUM IDD vs. FREQUENCY, WATCHDOG TIMER ENABLED, RC MODE (VDD = 15V, VIO = 5V)**

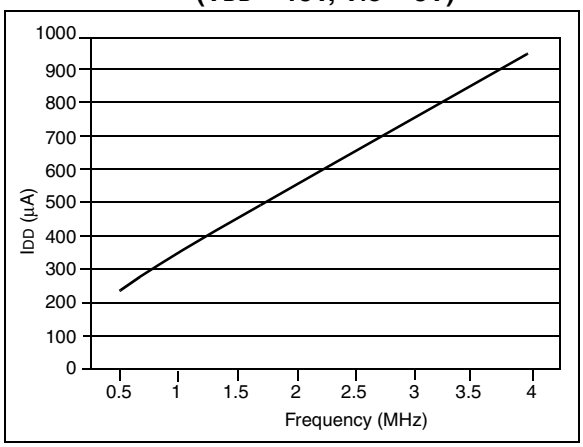
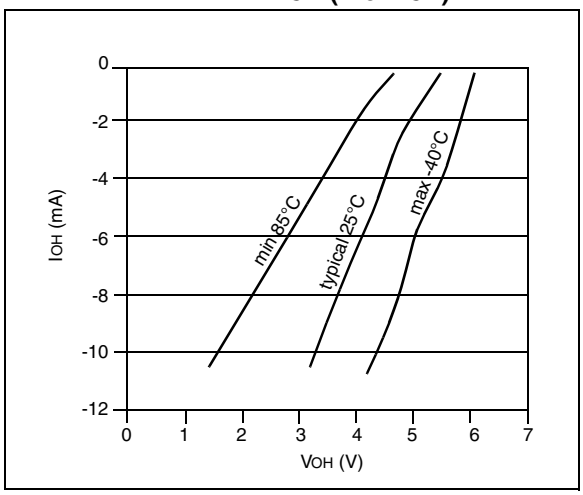
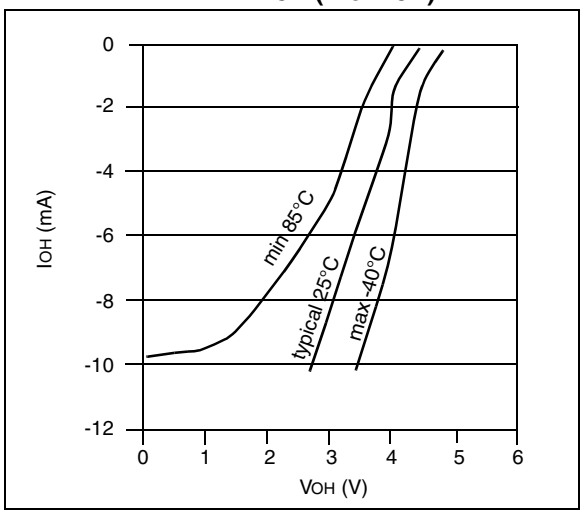


**FIGURE 11-15: IOH vs. VOH ON PORTA, VDD = 15V (VIO = 5V)**




**Note:** Current being applied is being applied simultaneously to all 4 PORTA pins.

**FIGURE 11-16: IOH vs. VOH ON PORTA, VDD = 5V (VIO = 5V)**




**Note:** Current being applied is being applied simultaneously to all 4 PORTA pins.

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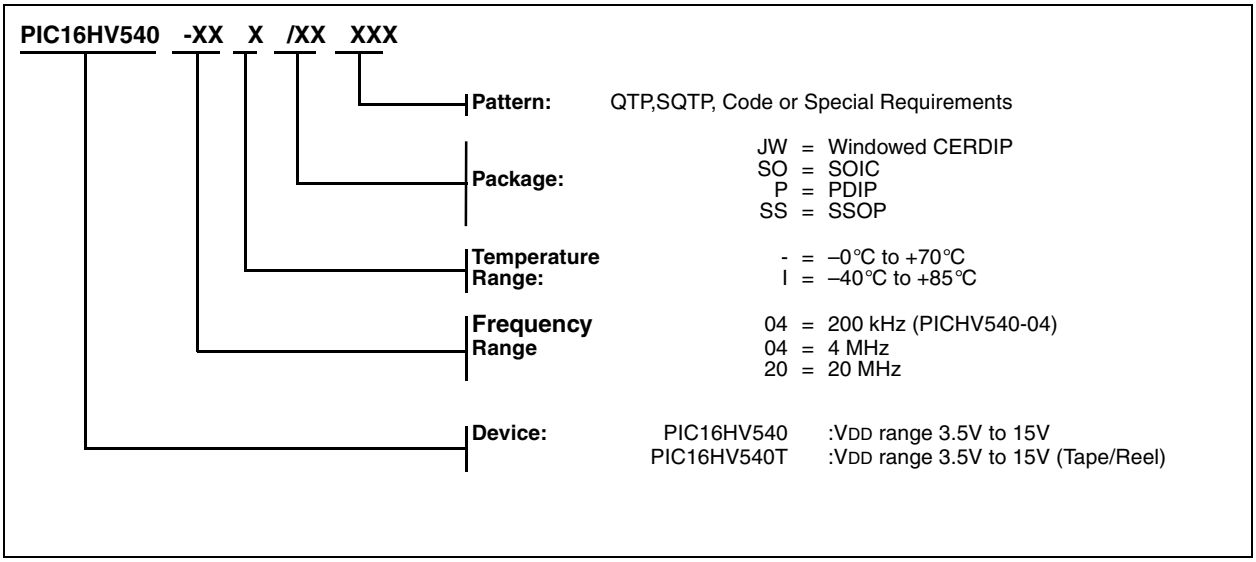
## PIC16HV540 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

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