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What is "Embedded - Microcontrollers"?

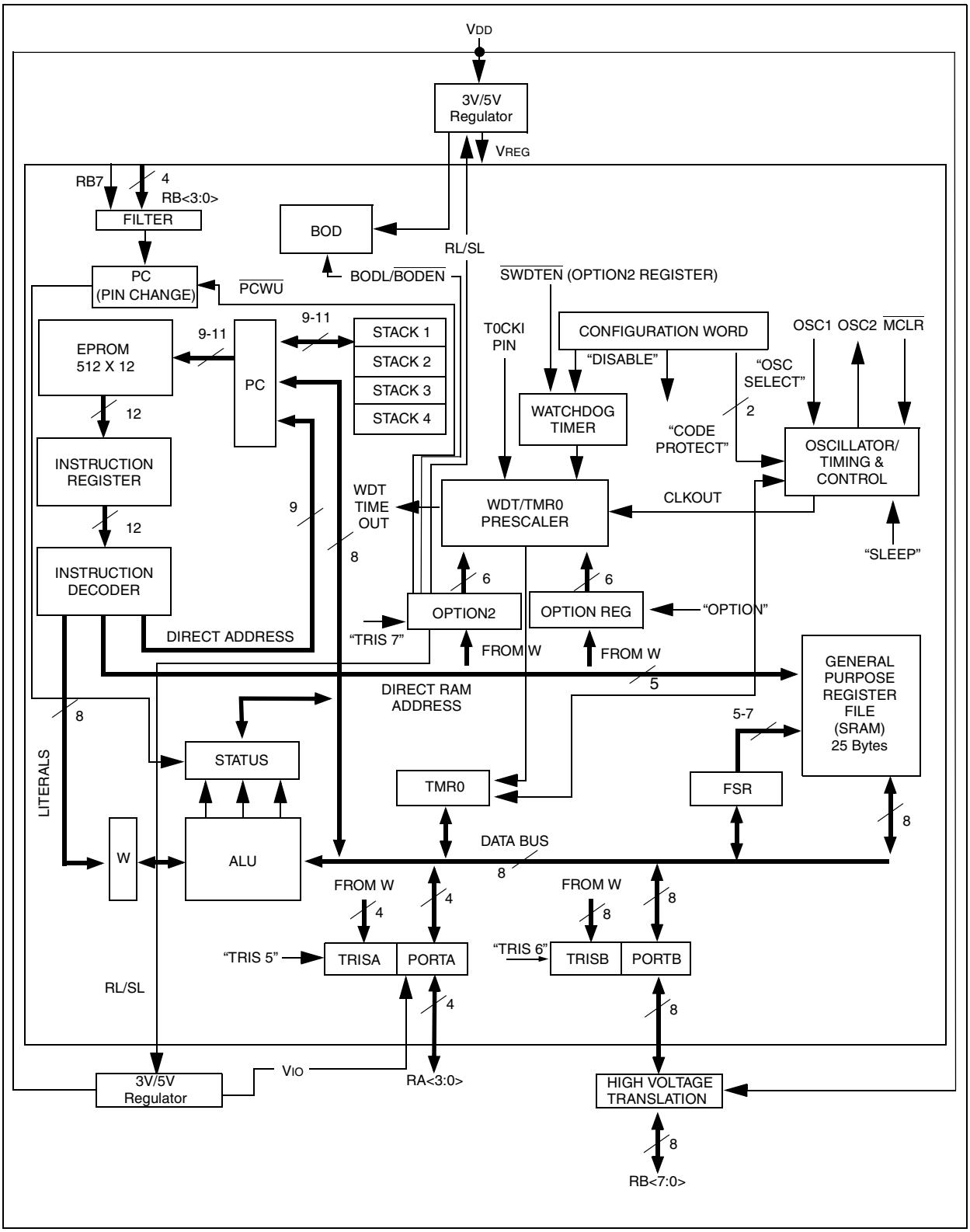
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 15V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16hv540-20-ss

NOTES:

FIGURE 3-1: PIC16HV540 BLOCK DIAGRAM



4.5 OPTION2 Register

The OPTION2 register is a 6-bit wide, write-only register which contains various control bits to configure the added features on the PIC16HV540. A Power-on Reset sets the OPTION2<5:0> bits.

Example 4-2 illustrates how to initialize the OPTION2 register.

Note:	All Power-on Resets will disable the Brown-out Detect circuit. All subsequent resets will not disable the Brown-out Detect if enabled.

EXAMPLE 4-2: INSTRUCTIONS FOR INITIALIZING OPTION2 REGISTER

```
movlw    '0001 0111'b    ; load OPTION2 setup value into W
tris     0x07            ; initialize OPTION2 register
```

REGISTER 4-3: OPTION2 REGISTER (TRIS 07H)

U-0	U-0	W-1	W-1	W-1	W-1	W-1	W-1
—	—	$\overline{\text{PCWU}}$	$\overline{\text{SWDTEN}}$	RL	SL	BODL	$\overline{\text{BODEN}}$
bit7							0

W = Writable bit
U = Unimplemented bit
- n = Value at POR reset

bit 7-6: **Unimplemented**

bit 5: **$\overline{\text{PCWU}}$**: Wake-up on Pin Change
1 = Disabled
0 = Enabled

bit 4: **$\overline{\text{SWDTEN}}$**: Software Controlled WDT Enable bit
1 = WDT is turned off it the WDTEN configuration bit = 0
0 = WDT is on if the WDTEN configuration bit = 0; if WDTEN bit = 1, then SWDTEN is 'don't care'

bit 3: **RL**: Regulated Voltage Level Select bit
1 = 5 volt
0 = 3 volt

bit 2: **SL:** Sleep Voltage Level Select bit
1 = **RL** bit setting
0 = 3 volt

bit 1: **BODL**: Brown-out Voltage Level Select bit
1 = **RL** bit setting, but **SL** during SLEEP
0 = 3 volt

bit 0: **$\overline{\text{BODEN}}$**: Brown-out Enabled
1 = Disabled
0 = Enabled

4.8 Indirect Data Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 4-3: INDIRECT ADDRESSING

- Register file 05 contains the value 10h
- Register file 06 contains the value 0Ah
- Load the value 05 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 06)
- A read of the INDR register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 4-4.

EXAMPLE 4-4: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

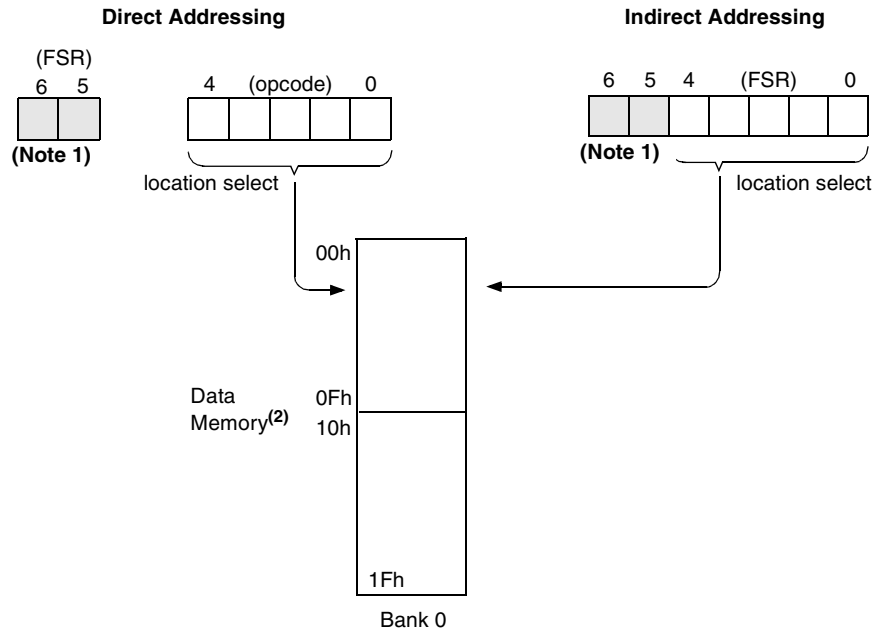
```
            movlw   0x10    ;initialize pointer
            movwf   FSR     ; to RAM
NEXT        clrf    INDF    ;clear INDF register
            incf    FSR,F   ;inc pointer
            btfsc   FSR,4   ;all done?
            goto    NEXT    ;NO, clear next
CONTINUE
            :               ;YES, continue
```

The FSR is a 5-bit (PIC16HV540) wide register. It is used in conjunction with the INDF register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

PIC16HV540: Do not use banking. FSR<6:5> are unimplemented and read as '1's.

FIGURE 4-4: DIRECT/INDIRECT ADDRESSING



Note 1: Bits 5 and 6 are unimplemented and read as 1's.

2: For register map detail, see Section 4.2.

FIGURE 5-1: BLOCK DIAGRAM OF PORTA<0:3> PINS

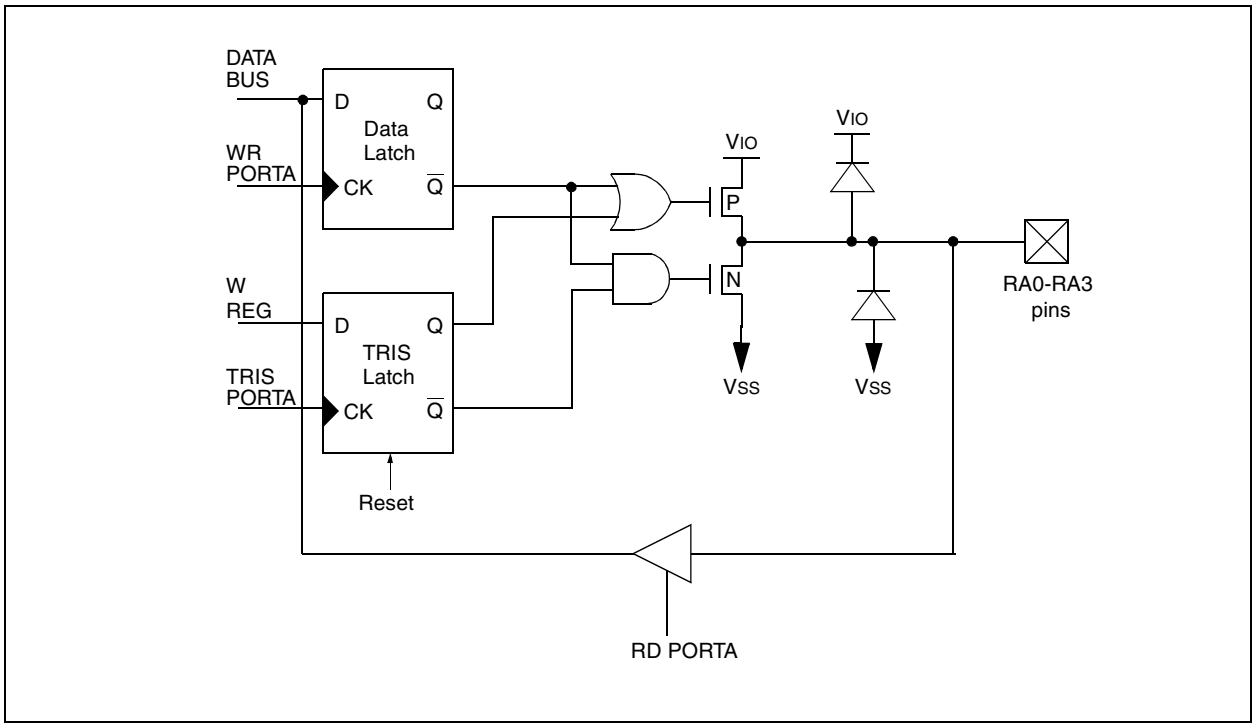


FIGURE 5-2: BLOCK DIAGRAM OF PORTB<0:3> PINS

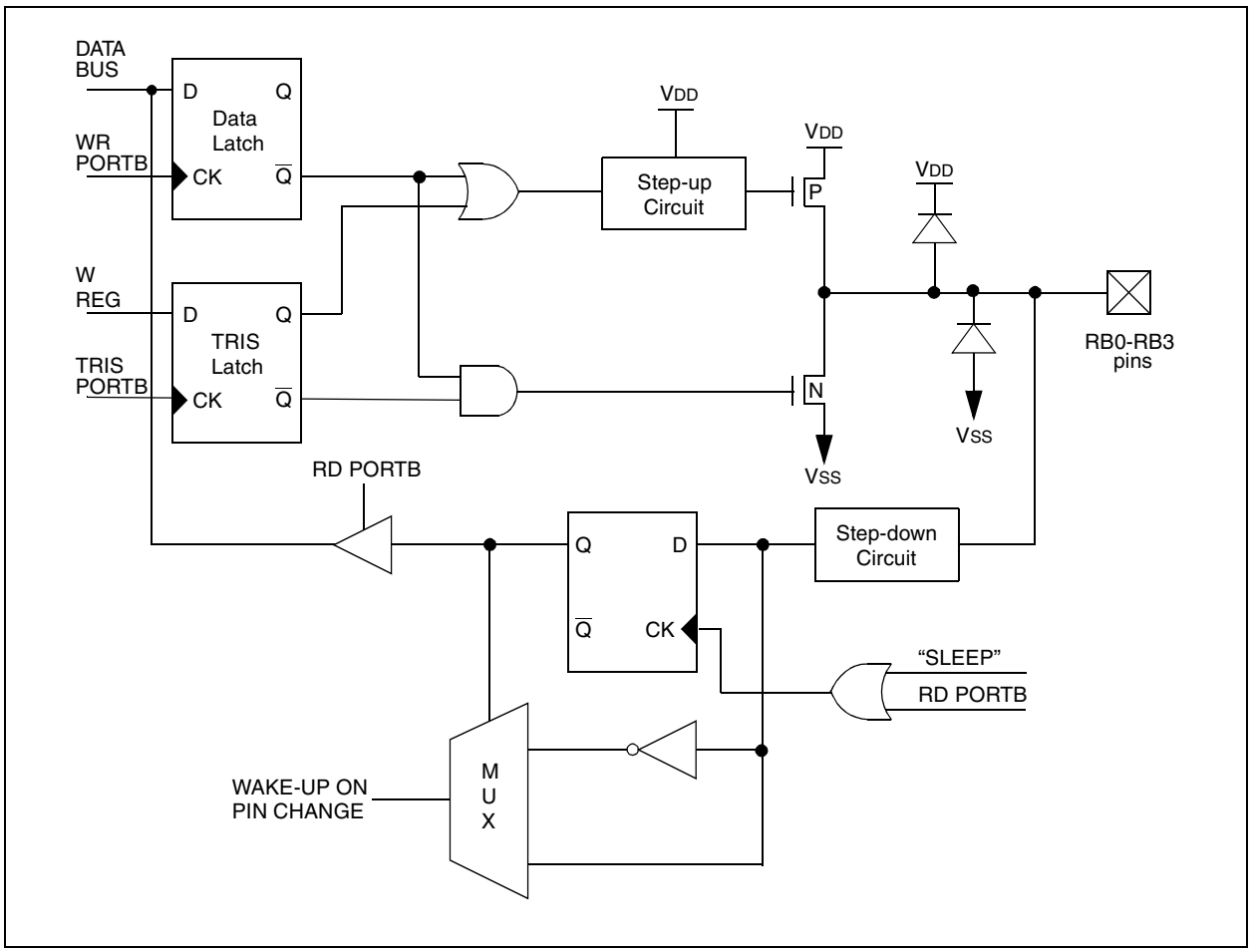


TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{\text{MCLR}}$ and WDT Reset	Value on Wake-up on Pin Change	Value on Brown-Out Reset
N/A	TRIS	I/O control registers (TRISA, TRISB)								1111 1111	1111 1111	1111 1111	1111 1111
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu	---- uuuu	---- xxxx
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu	uuuu uuuu	xxxx xxxx
03h	STATUS	$\overline{\text{PCWUF}}$	PA1	PA0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	100x xxxx	100q quuu	000u uuuu	x00x xxxx
N/A	OPTION2	—	—	$\overline{\text{PCWU}}$	$\overline{\text{SWDTEN}}$	RL	SL	BODL	$\overline{\text{BODEN}}$	--11 1111	--uu uuuu	--uu uuuu	--xx xxxx

Legend: Shaded boxes = unimplemented, read as '0', —= unimplemented, read as '0', x = unknown, u = unchanged.

5.5 I/O Programming Considerations

5.5.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

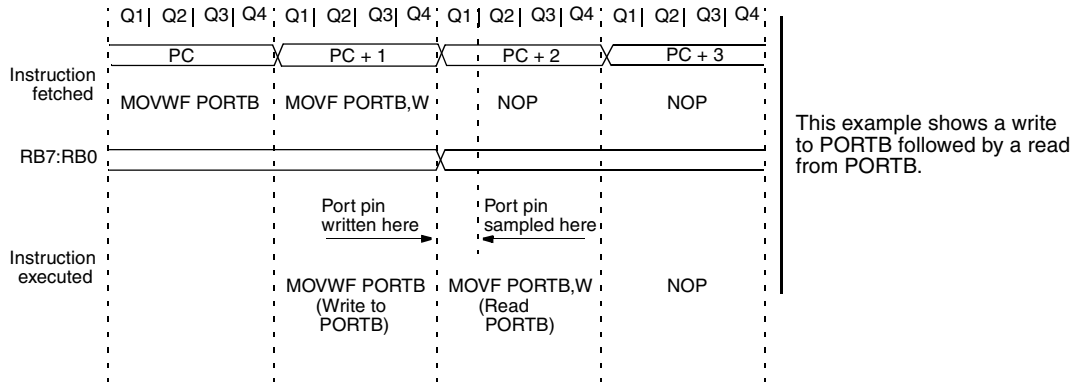
EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                    PORT latch  PORT pins
;                     ----------  ----------
  BCF   PORTB, 7    ;01pp pppp   11pp pppp
  BCF   PORTB, 6    ;10pp pppp   11pp pppp
  MOVLW 03Fh        ;
  TRIS  PORTB       ;10pp pppp   10pp pppp
;
;Note that the user may have expected the pin
;values to be 00pp pppp. The 2nd BCF caused
;RB7 to be latched as the pin value (High).
```

5.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-5). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 5-5: SUCCESSIVE I/O OPERATION



NOTES:

6.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (TOSC) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

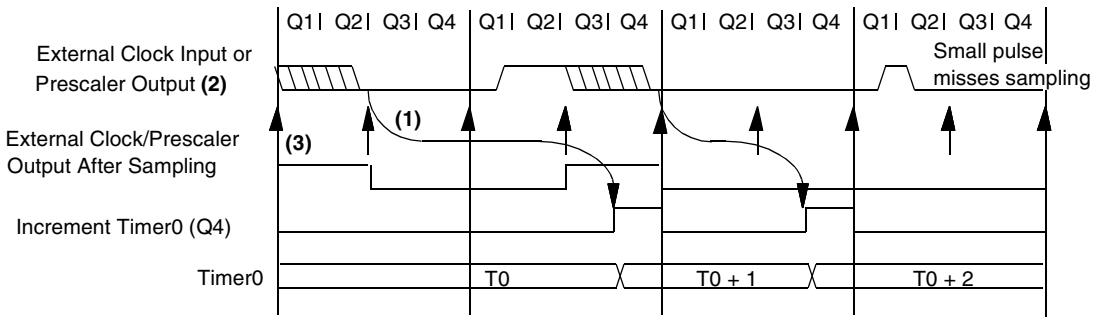
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-5). Therefore, it is necessary for T0CKI to be high for at least 2TOSC (and a small RC delay of 20 ns) and low for at least 2TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

6.1.2 TIMER0 INCREMENT DELAY

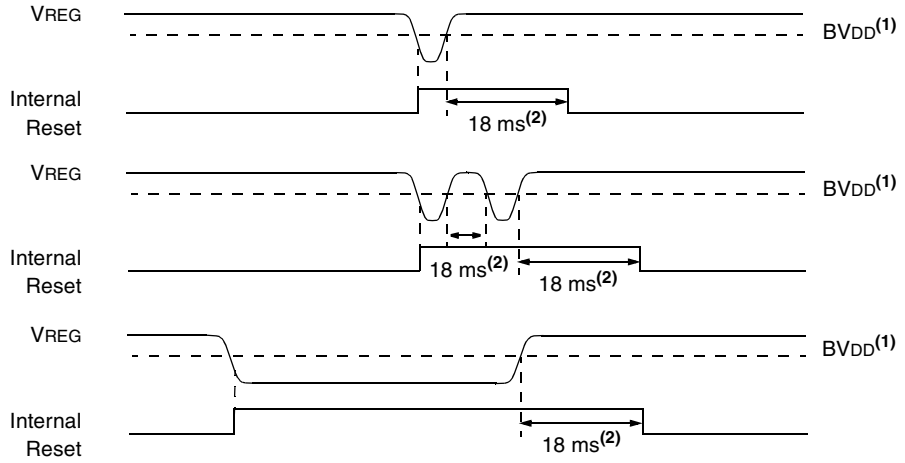
Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 6-5: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on Timer0 input = ± 4Tosc max.
2: External clock if no prescaler selected, Prescaler output otherwise.
3: The arrows indicate the points in time where sampling occurs.

FIGURE 7-11: BROWN-OUT SITUATIONS



Note 1: BVDD depends on selection of bit 'RL' in OPTION2 SFR.

2: DRT time depends on which oscillator mode is selected and which reset state the part is in.

7.7 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a `SLEEP` instruction. During normal operation or SLEEP, a WDT Reset or Wake-up Reset generates a device RESET.

The $\overline{TO}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset.

The Watchdog Timer is enabled/disabled by a device configuration bit (see Figure 7-1). If the WDT is enabled, software execution may not disable this function. When the WDTEN configuration bit is cleared, the $\overline{SWDTEN}$ bit, OPTION2<4>, enables/disables the operation of the WDT.

7.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

Under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

7.7.2 WDT PROGRAMMING CONSIDERATIONS

The `CLRWDT` instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The `SLEEP` instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.

7.8 Internal Voltage Regulators

The PIC16HV540 has 2 internal voltage regulators. The PORTA I/O pads and OSC2 are powered by one internal voltage regulator V_{IO}, while the second internal voltage regulator V_{REG}, powers the PICmicro® device core. Both regulated voltage levels can be synchronously switched in the active modes between 3V and 5V through bit "RL" in the OPTION2 register. In addition, the "SL" bit in the OPTION2 register can be used to control the core's regulated voltage level during SLEEP mode. V_{REG} regulates the 15V power applied to the V_{DD} pin.

The on-chip Brown-out Detect circuitry monitors the CPU regulated voltage V_{REG}, for determining if a brown-out reset is generated (see Section 7.6 for more details on the BOD).

The regulator circuits are identical in functional nature but only the V_{IO} regulator voltage can be measured, externally (See Section 10.1 for V_{IO} parameters). The operational voltage range and pin loading requirements must be considered to ensure proper system operation. For example, if 3V regulation is implemented during the SLEEP mode and 40mA is being sourced from PORTA, the V_{IO} regulation voltage may approach the specified minimum voltage. This may be an issue to consider for connections to external circuitry. Likewise, if zero current is sourced from the PORTA pins, the regulation

BSF — Bit Set f

Syntax:	[*label*] BSF f,b
Operands:	$0 \le f \le 31$ $0 \le b \le 7$
Operation:	$1 \rightarrow$ (f<b>)
Status Affected:	None
Encoding:	`0101` `bbbf` `ffff`
Description:	Bit 'b' in register 'f' is set.
Words:	1
Cycles:	1
Example:	`BSF FLAG_REG, 7`

Before Instruction
FLAG_REG = 0x0A

After Instruction
FLAG_REG = 0x8A

BTFSC — Bit Test f, Skip if Clear

Syntax:	[*label*] BTFSC f,b
Operands:	$0 \le f \le 31$ $0 \le b \le 7$
Operation:	skip if (f<b>) = 0
Status Affected:	None
Encoding:	`0110` `bbbf` `ffff`
Description:	If bit 'b' in register 'f' is 0 then the next instruction is skipped. If bit 'b' is 0 then the next instruction fetched during the current instruction execution is discarded, and an NOP is executed instead, making this a 2 cycle instruction.
Words:	1
Cycles:	1(2)

Example:

```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```

Before Instruction
PC = address (HERE)

After Instruction
if FLAG<1> = 0,
PC = address (TRUE);
if FLAG<1> = 1,
PC = address (FALSE)

BTFSS — Bit Test f, Skip if Set

Syntax:	[*label*] BTFSS f,b
Operands:	$0 \le f \le 31$ $0 \le b < 7$
Operation:	skip if (f<b>) = 1
Status Affected:	None
Encoding:	`0111` `bbbf` `ffff`
Description:	If bit 'b' in register 'f' is '1' then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and an NOP is executed instead, making this a 2 cycle instruction.
Words:	1
Cycles:	1(2)

Example:

```
HERE    BTFSS   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```

Before Instruction
PC = address (HERE)

After Instruction
If FLAG<1> = 0,
PC = address (FALSE);
if FLAG<1> = 1,
PC = address (TRUE)

COMF — Complement f

Syntax: [*label*] COMF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(\bar{f}) \rightarrow$ (dest)

Status Affected: Z

Encoding:

0010	01df	ffff

Description: The contents of register 'f' are complemented. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: `COMF REG1,0`

Before Instruction
REG1 = 0x13

After Instruction
REG1 = 0x13
W = 0xEC

DECF — Decrement f

Syntax: [*label*] DECF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – 1 → (dest)

Status Affected: Z

Encoding:

0000	11df	ffff

Description: Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: `DECF CNT, 1`

Before Instruction
CNT = 0x01
Z = 0

After Instruction
CNT = 0x00
Z = 1

DECFSZ — Decrement f, Skip if 0

Syntax: [*label*] DECFSZ f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – 1 → d; skip if result = 0

Status Affected: None

Encoding:

0010	11df	ffff

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

If the result is 0, the next instruction, which is already fetched, is discarded and an NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1(2)

Example:

```
HERE      DECFSZ   CNT, 1
          GOTO     LOOP
CONTINUE  •
          •
          •
```

Before Instruction
PC = address (HERE)

After Instruction
CNT = CNT - 1;
if CNT = 0,
PC = address (CONTINUE);
if CNT ≠ 0,
PC = address (HERE+1)

GOTO — Unconditional Branch

Syntax: [*label*] GOTO k

Operands: $0 \le k \le 511$

Operation: k → PC<8:0>;
STATUS<6:5> → PC<10:9>

Status Affected: None

Encoding:

101k	kkkk	kkkk

Description: GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two cycle instruction.

Words: 1

Cycles: 2

Example: `GOTO THERE`

After Instruction
PC = address (THERE)

MOVF — Move f

Syntax:	[*label*] MOVF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(f) → (dest)
Status Affected:	Z
Encoding:	0010 | 00df | ffff
Description:	The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.
Words:	1
Cycles:	1
Example:	`MOVF FSR, 0`

After Instruction
W = value in FSR register

MOVLW — Move Literal to W

Syntax:	[*label*] MOVLW k
Operands:	$0 \le k \le 255$
Operation:	k → (W)
Status Affected:	None
Encoding:	1100 | kkkk | kkkk
Description:	The eight bit literal 'k' is loaded into the W register. The don't cares will assemble as 0s.
Words:	1
Cycles:	1
Example:	`MOVLW 0x5A`

After Instruction
W = 0x5A

MOVWF — Move W to f

Syntax:	[*label*] MOVWF f
Operands:	$0 \le f \le 31$
Operation:	(W) → (f)
Status Affected:	None
Encoding:	0000 | 001f | ffff
Description:	Move data from the W register to register 'f'.
Words:	1
Cycles:	1
Example:	`MOVWF TEMP_REG`

Before Instruction
TEMP_REG = 0xFF
W = 0x4F

After Instruction
TEMP_REG = 0x4F
W = 0x4F

NOP — No Operation

Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Encoding:	0000 | 0000 | 0000
Description:	No operation.
Words:	1
Cycles:	1
Example:	`NOP`

OPTION — Load OPTION Register

Syntax:	[*label*] OPTION
Operands:	None
Operation:	(W) → OPTION
Status Affected:	None
Encoding:	0000 | 0000 | 0010
Description:	The content of the W register is loaded into the OPTION register.
Words:	1
Cycles:	1

Example

```
OPTIO
  N
```

Before Instruction
W = 0x07

After Instruction
OPTION = 0x07

RETLW — Return with Literal in W

Syntax:	[*label*] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Encoding:	1000 | kkkk | kkkk
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.
Words:	1
Cycles:	2

Example:

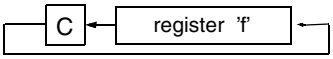
```
        CALL TABLE ;W contains
                   ;table offset
                   ;value.
        •          ;W now has table
        •          ;value.
        •
TABLE   ADDWF PC   ;W = offset
        RETLW k1   ;Begin table
        RETLW k2   ;
        •
        •
        •
        RETLW kn   ; End of table
```

Before Instruction
W = 0x07

After Instruction
W = value of k8

RLF — Rotate Left f through Carry

Syntax:	[*label*] RLF f,d
Operands:	0 ≤ f ≤ 31 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Encoding:	0011 | 01df | ffff
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.



Words:	1
Cycles:	1

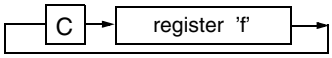
Example: `RLF REG1,0`

Before Instruction
REG1 = 1110 0110
C = 0

After Instruction
REG1 = 1110 0110
W = 1100 1100
C = 1

RRF — Rotate Right f through Carry

Syntax:	[*label*] RRF f,d
Operands:	0 ≤ f ≤ 31 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Encoding:	0011 | 00df | ffff
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.



Words:	1
Cycles:	1

Example: `RRF REG1,0`

Before Instruction
REG1 = 1110 0110
C = 0

After Instruction
REG1 = 1110 0110
W = 0111 0011
C = 0

SWAPF — Swap Nibbles in f

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f<3:0>) → (dest<7:4>);
(f<7:4>) → (dest<3:0>)

Status Affected: None

Encoding:

0011	10df	ffff

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Example `SWAPF REG1, 0`

Before Instruction
REG1 = 0xA5

After Instruction
REG1 = 0xA5
W = 0X5A

TRIS — Load TRIS Register

Syntax: [*label*] TRIS f

Operands: f = 5, 6 or 7

Operation: (W) → TRIS register f

Status Affected: None

Encoding:

0000	0000	0fff

Description: TRIS register 'f' (f = 5, 6, or 7*) is loaded with the contents of the W register

Words: 1

Cycles: 1

Example `TRIS PORTA`

Before Instruction
W = 0XA5

After Instruction
TRISA = 0XA5

*A TRIS 7 operation will update the OPTION2 SFR.

XORLW — Exclusive OR literal with W

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Encoding:

1111	kkkk	kkkk

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: `XORLW 0xAF`

Before Instruction
W = 0xB5

After Instruction
W = 0x1A

XORWF — Exclusive OR W with f

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (dest)

Status Affected: Z

Encoding:

0001	10df	ffff

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example `XORWF REG,1`

Before Instruction
REG = 0xAF
W = 0xB5

After Instruction
REG = 0x1A
W = 0xB5

TABLE 9-1: DEVELOPMENT TOOLS FROM MICROCHIP

		PIC12CXXX	PIC14000	PIC16C5X	PIC16C6X	PIC16CXXX	PIC16F62X	PIC16C7X	PIC16C7XX	PIC16C8X	PIC16F8XX	PIC16C9XX	PIC17C4X	PIC17C7XX	PIC18CXX2	24CXX/ 25CXX/ 93CXX	HCSXXX	MCRFXXX	MCP2510
Software Tools	MPLAB® Integrated Development Environment	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				
Software Tools	MPLAB® C17 Compiler												✓	✓					
Software Tools	MPLAB® C18 Compiler														✓				
Software Tools	MPASM/MPLINK	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Emulators	MPLAB®-ICE	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓				
Emulators	PICMASTER/PICMASTER-CE	✓	✓	✓	✓	✓		✓	✓	✓		✓	✓	✓					
Emulators	ICEPIC™ Low-Cost In-Circuit Emulator	✓		✓	✓	✓		✓	✓	✓		✓							
Debugger	MPLAB®-ICD In-Circuit Debugger				✓*			✓*			✓								
Programmers	PICSTART® Plus Low-Cost Universal Dev. Kit	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓				
Programmers	PRO MATE® II Universal Programmer	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Demo Boards and Eval Kits	SIMICE	✓		✓															
Demo Boards and Eval Kits	PICDEM-1			✓		✓		✓†		✓			✓						
Demo Boards and Eval Kits	PICDEM-2				✓†			✓†							✓				
Demo Boards and Eval Kits	PICDEM-3											✓							
Demo Boards and Eval Kits	PICDEM-14A		✓																
Demo Boards and Eval Kits	PICDEM-17													✓					
Demo Boards and Eval Kits	KEELOQ® Evaluation Kit																✓		
Demo Boards and Eval Kits	KEELOQ Transponder Kit																✓		
Demo Boards and Eval Kits	microID™ Programmer's Kit																	✓	
Demo Boards and Eval Kits	125 kHz microID Developer's Kit																	✓	
Demo Boards and Eval Kits	125 kHz Anticollision microID Developer's Kit																	✓	
Demo Boards and Eval Kits	13.56 MHz Anticollision microID Developer's Kit																	✓	
Demo Boards and Eval Kits	MCP2510 CAN Developer's Kit																		✓

* Contact the Microchip Technology Inc. web site at www.microchip.com for information on how to use the MPLAB®-ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77
** Contact Microchip Technology Inc. for availability date.
† Development tool is available on select devices.

10.0 ELECTRICAL CHARACTERISTICS - PIC16HV540

Absolute Maximum Ratings†

Ambient temperature under bias ..... –20°C to +85°C

Storage temperature ..... –65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} ..... 0 to +16V

Voltage on $\overline{MCLR}$ with respect to V_{SS} ..... 0 to +14V

Voltage on all other pins with respect to V_{SS} ..... –0.6V to (V_{DD} + 0.6V)

Total power dissipation(1) ..... 800 mW

Max. current out of V_{SS} pin ..... 150 mA

Max. current into V_{DD} pin ..... 100 mA

Max. current into an input pin (T0CKI only) ..... ±500 μA

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA

Max. output current sunk by any I/O pin ..... 25 mA

Max. output current sourced by any I/O pin ..... 10 mA

Max. output current sourced by a single I/O port A or B ..... 40 mA

Max. output current sourced by a single I/O port A or B ..... 50 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

10.4 Timing Diagrams and Specifications

FIGURE 10-2: EXTERNAL CLOCK TIMING - PIC16HV540

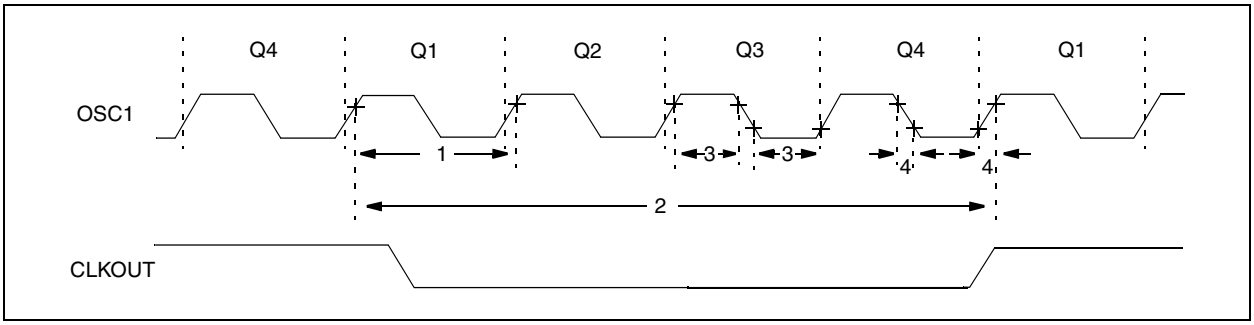


TABLE 10-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16HV540

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)						
Parameter No.	**Sym.**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
	FOSC	External CLKIN Frequency(2)	DC	—	4.0	MHz	RC osc mode
			DC	—	2.0	MHz	HS osc mode
			DC	—	4.0	MHz	XT osc mode
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4.0	MHz	RC osc mode
			0.1	—	2.0	MHz	HS osc mode
			0.1	—	4.0	MHz	XT osc mode
			5	—	200	kHz	LP osc mode
1	TOSC	External CLKIN Period(2)	250	—	—	ns	RC osc mode
			250	—	—	ns	HS osc mode
			250	—	—	ns	XT osc mode
			5.0	—	—	µs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	HS osc mode
			250	—	10,000	ns	XT osc mode
			50	—	200	µs	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	µs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at VREG = 5V, VDD = 9V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 11-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD (CEXT = 300pF)

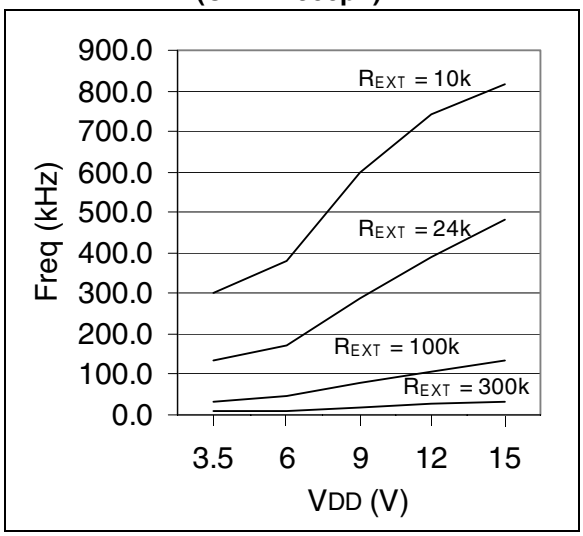


FIGURE 11-5: TYPICAL IPD vs. VDD, WATCHDOG TIMER DISABLED (VIO = 5V)

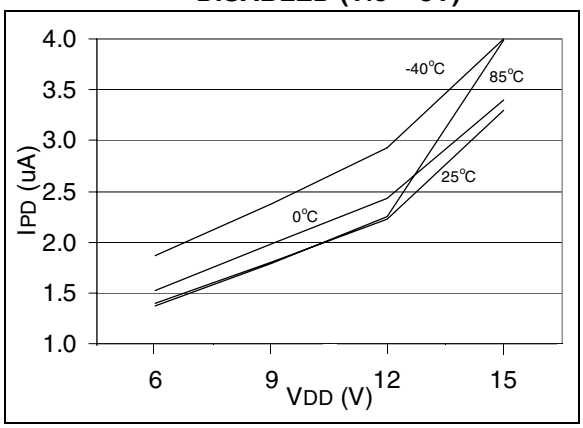


FIGURE 11-6: MAXIMUM IPD vs. VDD, WATCHDOG TIMER DISABLED (VIO = 5V)

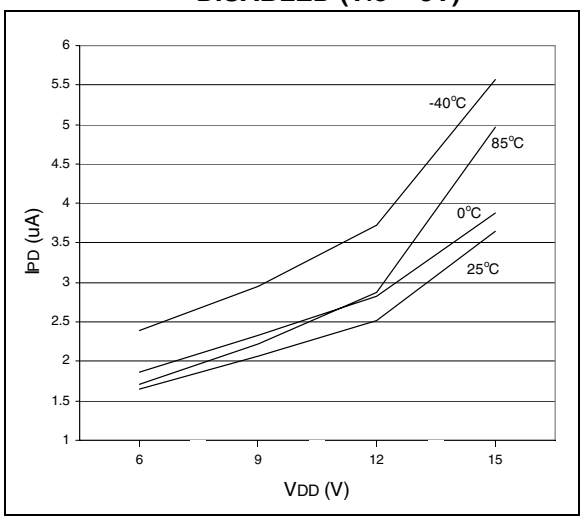


FIGURE 11-7: TYPICAL IPD vs. VDD, WATCHDOG TIMER ENABLED (VIO = 5V)

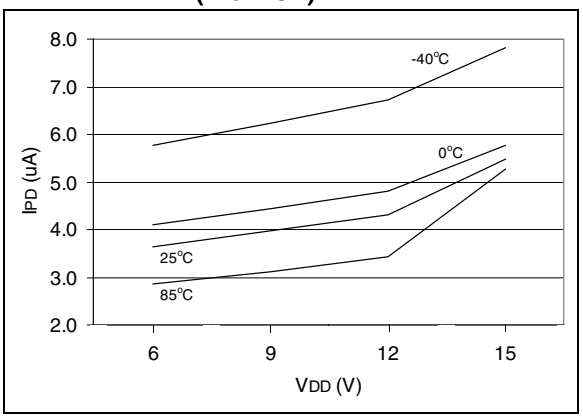


FIGURE 11-8: MAXIMUM IPD vs. VDD, WATCHDOG TIMER ENABLED (VIO = 5V)

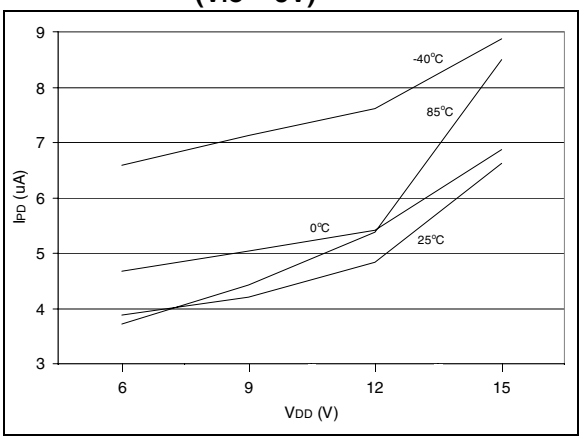
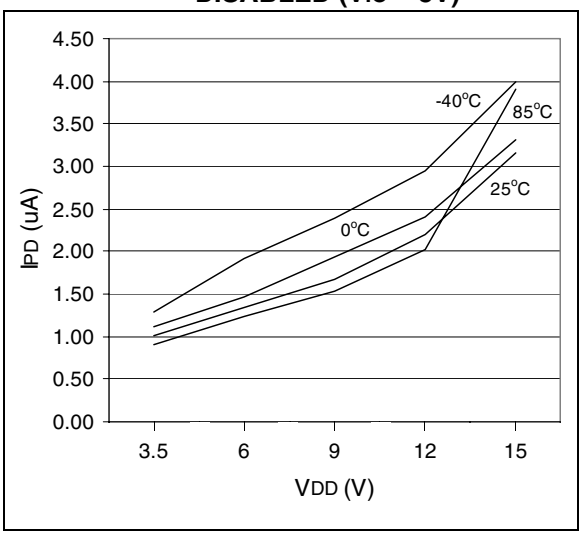


FIGURE 11-9: TYPICAL IPD vs. VDD, WATCHDOG TIMER DISABLED (VIO = 3V)



PIC16HV540 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PIC16HV540 -XX X /XX XXX

Pattern:	QTP,SQTP, Code or Special Requirements	
Package:	JW =	Windowed CERDIP
	SO =	SOIC
	P =	PDIP
	SS =	SSOP
Temperature Range:	- =	–0°C to +70°C
	I =	–40°C to +85°C
Frequency Range	04 =	200 kHz (PICHV540-04)
	04 =	4 MHz
	20 =	20 MHz
Device:	PIC16HV540	:VDD range 3.5V to 15V
	PIC16HV540T	:VDD range 3.5V to 15V (Tape/Reel)

Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 786-7277.
3. The Microchip Worldwide Site (www.microchip.com)

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