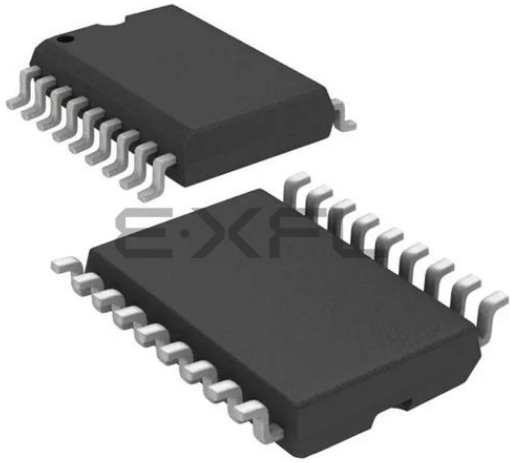

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Details	
Product Status	Discontinued at Digi-Key
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 15V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16hv540t-04-so

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1.0 GENERAL DESCRIPTION

The PIC16HV540 from Microchip Technology is a low-cost, high-performance, 8-bit, fully-static, EPROM-based CMOS microcontroller. It is pin and software compatible with the PIC16C5X family of devices. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle except for program branches, which take two cycles. The PIC16HV540 delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly orthogonal resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy-to-use and easy-to-remember instruction set reduces development time significantly.

The PIC16HV540 is the first One-Time-Programmable (OTP) microcontroller with an on-chip 3 volt and 5 volt regulator. This eliminates the need for an external regulator in many applications powered from 9 Volt or 12 Volt batteries or unregulated 6 volt, 9 volt or 12 volt mains adapters. The PIC16HV540 is ideally suited for applications that require very low standby current at high voltages. These typically require expensive low current regulators.

The PIC16HV540 is equipped with special features that reduce system cost and power requirements. The Power-On Reset (POR) and Device Reset Timer (DRT) eliminate the need for external reset circuitry. There are four oscillator configurations to choose from, including the power-saving LP (Low Power) oscillator, cost saving RC oscillator, and XT and HS for crystal oscillators. Power saving SLEEP mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The UV erasable CERDIP packaged versions are ideal for code development, while the cost-effective OTP versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers, while benefiting from the OTP's flexibility.

The PIC16HV540 is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer, and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1 Applications

The PIC16HV540 fits in low-power battery applications such as CO and smoke detection, toys, games, security systems and automobile modules. The EPROM technology makes customizing of application programs (transmitter codes, receiver frequencies, etc.) extremely fast and convenient. The small footprint package, for through hole or surface mounting, make this microcontroller suitable for applications with space limitations. Low-cost, low-power, high-performance, ease of use and I/O flexibility make the PIC16HV540 very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, coprocessor applications).

1.2 Enhanced Features

1.2.1 REGULATED I/O PORTA INDEPENDENT OF CORE REGULATOR

PORTA I/O pads and OSC2 output are powered by the regulated internal voltage V_{IO}. A maximum of 10mA per output is allowed, or a total of 40mA. The core itself is powered from the independently regulated supply V_{REG}.

1.2.2 HIGH VOLTAGE I/O PORTB

All eight PORTB I/Os are high voltage I/O. The inputs will tolerate input voltages as high as the V_{DD} and outputs will swing from V_{SS} to the V_{DD}. The input threshold voltages vary with supply voltage. (See Electrical Characteristics.)

1.2.3 WAKE-UP ON PIN CHANGE ON PORTB [0:3]

Four of the PORTB inputs latch the status of the pin at the onset of sleep mode. A level change on the inputs resets the device, implementing wake up on pin change (via warm reset). The $\overline{\text{PCWUF}}$ bit in the status register is reset to indicate that a pin change caused the reset condition. Any pin change (glitch insensitive) of the opposite level of the initial value wakes up the device. This option can be enabled/disabled in OPTION2 register. (See OPTION2 Register, Register 4-3.)

1.2.4 WAKE-UP ON PIN CHANGE WITH A SLOWLY-RISING VOLTAGE ON PORTB [7]

PORTB [7] also implements wake up from sleep, however this input is specifically adapted so that a slowly **rising** voltage does not cause excessive power consumption. This input can be used with external RC circuits for long sleep periods without using the internal timer and prescaler. This option is also enabled/disabled in OPTION2 register. (The enable/disable bit is shared with the other 4 wake-up inputs.) The $\overline{\text{PCWUF}}$ bit in the status register is also shared with the other four wake-up inputs.

1.2.5 LOW-VOLTAGE (BROWN-OUT) DETECTION

A low voltage (Brown-out) detect circuit optionally resets the device at a voltage level higher than that at which the PICmicro® device stops operating. The nominal trip voltages are 3.1 volts (for 5 volt operation) and 2.2 volt (for 3 volt operation), respectively. The core remains in the reset state as long as this condition holds (as if a $\overline{\text{MCLR}}$ external reset was given). The Brown-out trip level is user selectable, with built-in interlocks. The Brown-out detector is disabled at power-up and is activated by clearing the appropriate bit ($\overline{\text{BODEN}}$) in OPTION2 register.

1.2.6 INCREASED STACK DEPTH

The stack depth is 4 levels to allow modular program implementation by using functions and subroutines.

1.2.7 ENHANCED WATCHDOG TIMER (WDT) OPERATION

The WDT is enabled by setting FUSE 2 in the configuration word. The WDT setting is latched and the fuse disabled during SLEEP mode to reduce current consumption.

If the WDT is disabled by FUSE 2, it can be enabled/disabled under program control using bit 4 in OPTION2 Register (SWDTEN). The software WDT control is disabled at power-up.

The current consumption of the on-chip oscillator (used for the watchdog, oscillator startup timer and sleep timer) is less than 1μA (typical) at 3 Volt operation.

1.2.8 REDUCED EXTERNAL RC OSCILLATOR STARTUP TIME

If the RC oscillator option is selected in the Configuration word (FOSC1=1 and FOSCO=1), the oscillator startup time is 1.0 ms nominal instead of 18 ms nominal. This is applicable after power-up (POR), either WDT interrupt or wake-up, external reset on MCLR, PCWU (wake on pin change) and Brown-out.

1.2.9 LOW-VOLTAGE OPERATION OF THE ENTIRE CPU DURING SLEEP

The voltage regulator can automatically lower the voltage to the core from 5 Volt to 3 Volt during sleep, resulting in reduced current consumption. This is an option bit (SL) in the OPTION2 register.

1.2.10 GLITCH FILTERS ON WAKE-UP PINS AND MCLR

Glitch sensitive inputs for wake-up on pin change are filtered to reduce susceptibility to interference. A similar filter reduces false reset on MCLR.

1.2.11 PROGRAMMABLE CLOCK GENERATOR

When used in RC mode, the CLKOUT pin can be used as a programmable clock output. The output is connected to TMR0, bit 0 and by setting the prescaler, clock out frequencies of CLKIN/8 to CLKIN/1024 can be generated. The CLKOUT pin can also be used as a general purpose output by modifying TMR0, bit 0.

TABLE 1-1: PIC16HV540 DEVICE

		PIC16HV540
Clock	Maximum Frequency (MHz)	20
Memory	EPROM Program Memory	512
	RAM Data Memory (bytes)	25
Peripherals	Timer Module(s)	TMR0
Packages	I/O Pins	12
	Voltage Range (Volts)	3.5V-15V
	Number of Instructions	33
	Packages	18-pin DIP SOIC 20-pin SSOP

All PICmicro® devices have Power-on Reset, selectable WDT, selectable code protect and high I/O current capability.

TABLE 3-1: PINOUT DESCRIPTION - PIC16HV540

Name	DIP, SOIC No.	SSOP No.	I/O/P Type	Input Levels	Description	
RA0	17	19	I/O	TTL	Independently regulated Bi-directional I/O port — VIO	
RA1	18	20	I/O	TTL		
RA2	1	1	I/O	TTL		
RA3	2	2	I/O	TTL		
RB0	6	7	I/O	TTL	High-voltage Bi-directional I/O port. Sourced from VDD.	Wake-up on pin change
RB1	7	8	I/O	TTL		
RB2	8	9	I/O	TTL		
RB3	9	10	I/O	TTL		
RB4	10	11	I/O	TTL		
RB5	11	12	I/O	TTL		
RB6	12	13	I/O	TTL		
RB7	13	14	I/O	TTL		Wake-up on SLOW rising pin change.
T0CKI	3	3	I	ST	Clock input to Timer 0. Must be tied to VSS or VDD, if not in use, to reduce current consumption.	
$\overline{MCLR}$/VPP	4	4	I	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device. Voltage on the $\overline{MCLR}$/VPP pin must not exceed VDD(1) to avoid unintended entering of programming mode.	
OSC1/CLKIN	16	18	I	ST	Oscillator crystal input/external clock source input.	
OSC2/CLKOUT	15	17	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2/CLKOUT output is connected to TMR0, bit 0. Frequencies of CLKIN/8 to CLKIN/1024 can be generated on this pin.	
VDD	14	15,16	P	—	Positive supply.	
VSS	5	5,6	P	—	Ground reference.	

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input.

Note 1: VDD during programming mode can not exceed parameter PD1 called out in the PIC16C5X Programming Specification (Literature number DS30190).

4.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bits for program memories larger than 512 words.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable while the $\overline{PCWUF}$ bit is a read/write bit. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS register because these instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions, which do affect STATUS bits, see Section 8.0, Instruction Set Summary.

REGISTER 4-1: STATUS REGISTER (ADDRESS:03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
$\overline{PCWUF}$	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7							bit0

R = Readable bit
W = Writable bit
- n = Value at POR reset

bit 7: **$\overline{PCWUF}$**: Pin Change Reset bit
1 = After Power-up Reset (POR) or SLEEP command
0 = After a wake-up on pin change event

bit 6-5: **Not Applicable**

bit 4: **$\overline{TO}$**: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: **$\overline{PD}$**: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (for `ADDWF` and `SUBWF` instructions)
ADDWF
1 = A carry from the 4th low order bit of the result occurred
0 = A carry from the 4th low order bit of the result did not occur
SUBWF
1 = A borrow from the 4th low order bit of the result did not occur
0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C**: Carry/$\overline{borrow}$ bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)

ADDWF	**SUBWF**	**RRF or RLF**
1 = A carry occurred	1 = A borrow did not occur	Load bit with LSb or MSb, respectively
0 = A carry did not occur	0 = A borrow occurred	

4.4 OPTION Register

The OPTION register is a 6-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the OPTION instruction, the contents of the W register will be transferred to the OPTION register. A RESET sets the OPTION<5:0> bits.

Example 4-1 illustrates how to initialize the OPTION register.

EXAMPLE 4-1: INSTRUCTIONS FOR INITIALIZING OPTION REGISTER

```
movlw   '0000 0111'b   ; load OPTION setup value into W
OPTION                 ; initialize OPTION register
```

REGISTER 4-2: OPTION REGISTER

U-0	U-0	W-1	W-1	W-1	W-1	W-1	W-1
—	—	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7							0

W = Writable bit
U = Unimplemented bit
- n = Value at POR reset

bit 7-6: **Unimplemented**

bit 5: **T0CS**: Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3: **PSA**: Prescaler Assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0: **PS<2:0>**: Prescaler Rate Select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{MCLR}$ and WDT Reset	Value on Wake-up on Pin Change	Value on Brown-Out Reset
N/A	TRIS	I/O control registers (TRISA, TRISB)								1111 1111	1111 1111	1111 1111	1111 1111
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu	---- uuuu	---- xxxx
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu	uuuu uuuu	xxxx xxxx
03h	STATUS	$\overline{PCWUF}$	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	100x xxxx	100q quuu	000u uuuu	x00x xxxx
N/A	OPTION2	—	—	$\overline{PCWU}$	$\overline{SWDTEN}$	RL	SL	BODL	$\overline{BODEN}$	--11 1111	--uu uuuu	--uu uuuu	--xx xxxx

Legend: Shaded boxes = unimplemented, read as '0', —= unimplemented, read as '0', x = unknown, u = unchanged.

5.5 I/O Programming Considerations

5.5.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                   PORT latch  PORT pins
;                    ----------  ----------
  BCF   PORTB, 7    ;01pp pppp   11pp pppp
  BCF   PORTB, 6    ;10pp pppp   11pp pppp
  MOVLW 03Fh        ;
  TRIS  PORTB       ;10pp pppp   10pp pppp
;
;Note that the user may have expected the pin
;values to be 00pp pppp. The 2nd BCF caused
;RB7 to be latched as the pin value (High).
```

5.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-5). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

NOTES:

7.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC16HV540 family of microcontrollers has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator selection
- Reset
- Power-On Reset (POR)
- Brown-out Detect
- Device Reset Timer (DRT)
- Wake-up from SLEEP on Pin Change
- Enhanced Watchdog Timer (WDT)
- SLEEP
- Code protection

The PIC16HV540 Family has a Watchdog Timer which can be shut off only through configuration bit WDTEN. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in reset until the crystal oscillator is stable. With this timer on-chip, most applications need no external reset circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake up from SLEEP through external reset or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

7.1 Configuration Bits

Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type and one bit is the Watchdog Timer enable bit. Nine bits are code protection bits (Figure 7-1) for the PIC16HV540 devices.

REGISTER 7-1: CONFIGURATION WORD FOR PIC16HV540

CP	CP	CP	CP	CP	CP	CP	CP	CP	WDTEN	FOSC1	FOSC0
bit11											bit0

Register:CONFIG
Address(1):0FFFh

bit 11-3: **CP:** Code Protection bits
1 = Code protection off
0 = Code protection on

bit 2: **WDTEN:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled (control is placed on the $\overline{\text{SWDTEN}}$ bit)

bit 1-0: **Fosc<1:0>:** Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Refer to the PIC16C5X Programming Specification (Literature number DS30190) to determine how to access the configuration word.

TABLE 7-3: RESET CONDITIONS FOR SPECIAL REGISTERS

Condition	PCL Addr: 02h	STATUS Addr: 03h
Power-on Reset	1111 1111	1001 1xxx
$\overline{MCLR}$ Reset (normal operation)	1111 1111	u00u uuuu(1)
$\overline{MCLR}$ Wake-up (from SLEEP)	1111 1111	1001 0uuu
WDT Reset (normal operation)	1111 1111	u000 1uuu(2)
WDT Wake-up (from SLEEP)	1111 1111	1000 0uuu
Wake-up from SLEEP on Pin Change	1111 1111	000u uuuu
Brown-out Reset	1111 1111	x00x xxxx

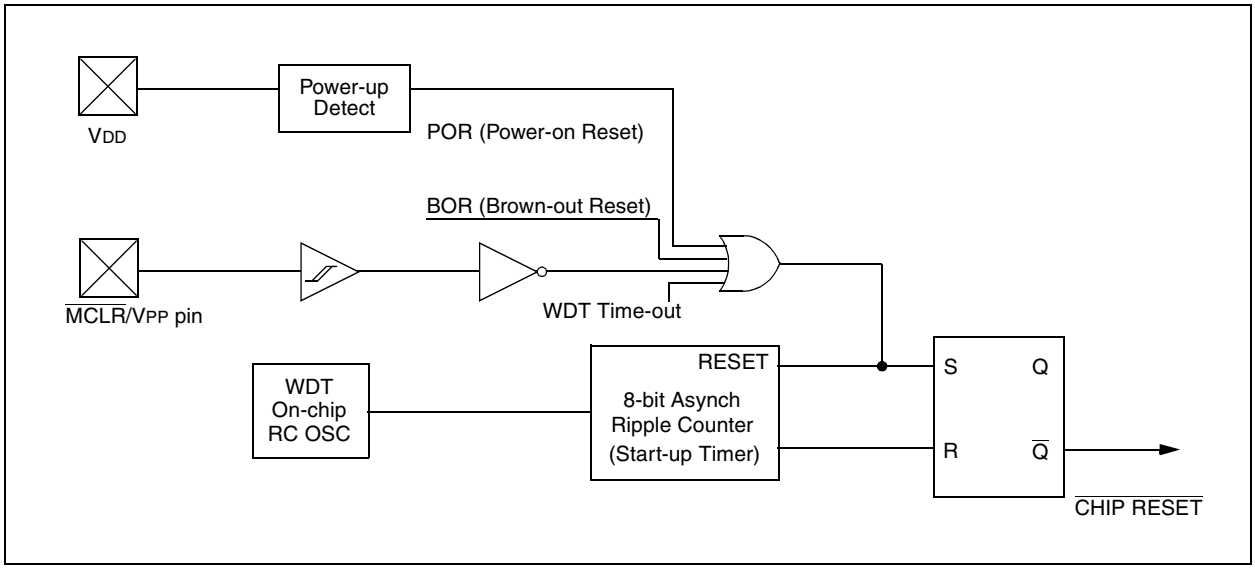
Legend: u = unchanged, x = unknown, - = unimplemented read as '0'.
Note 1: $\overline{TO}$ and $\overline{PD}$ bits retain their last value until one of the other reset conditions occur.
2: The CLRWDT instruction will set the $\overline{TO}$ and $\overline{PD}$ bits.

TABLE 7-4: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-On Reset	$\overline{MCLR}$ or WDT Reset	Wake-up on Pin Change	Brown-out Reset
W	N/A	xxxx xxxx	uuuu uuuu	uuuu uuuu	xxxx xxxx
TRIS	N/A	1111 1111	1111 1111	1111 1111	1111 1111
OPTION	N/A	--11 1111	--11 1111	--11 1111	--11 1111
OPTION2	N/A	--11 1111	--uu uuuu	--uu uuuu	--xx xxxx
INDF	00h	xxxx xxxx	uuuu uuuu	uuuu uuuu	xxxx xxxx
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu	xxxx xxxx
PCL(1)	02h	1111 1111	1111 1111	1111 1111	1111 1111
STATUS(1)	03h	1001 1xxx	100? ?uuu	000u uuuu	x00x xxxx
FSR	04h	111x xxxx	111u uuuu	111u uuuu	111x xxxx
PORTA	05h	---- xxxx	---- uuuu	---- uuuu	---- xxxx
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu	xxxx xxxx
General Purpose Register Files	07-1Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu	xxxx xxxx

Legend: u = unchanged, x = unknown, - = unimplemented, read as '0', q = see tables in Section 7.10 for possible values.
? = value depends on condition.
Note 1: See Table 7-3 for reset value for specific conditions.

FIGURE 7-6: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



7.9 Time-out Sequence and Power-down Status Bits (TO/PD/PCWUF)

The TO, PD and PCWUF bits in the STATUS register can be tested to determine if a RESET condition has been caused by a power-up condition, a MCLR, Watchdog Timer (WDT) Reset, WDT Wake-up Reset, or Wake-up from SLEEP on Pin Change.

TABLE 7-7: TO/PD/PCWUF STATUS AFTER RESET

PCWUF	TO	PD	RESET was caused by
1	1	1	Power-up (POR)
u	u	u	MCLR Reset (normal operation)(1)
u	1	0	MCLR Wake-up Reset (from SLEEP)
u	0	1	WDT Reset (normal operation)
u	0	0	WDT Wake-up Reset (from SLEEP)
0	u	u	Wake-up from SLEEP on Pin Change
x	x	x	Brown-out Reset

Legend: u = unchanged, x = unknown

Note 1: The TO and PD and PCWUF bits maintain their status (u) until a reset occurs. A low-pulse on the MCLR input does not change the TO and PD and PCWUF status bits.

These STATUS bits are only affected by events listed in Table 7-8.

TABLE 7-8: EVENTS AFFECTING TO/PD STATUS BITS

Event	PCWUF	TO	PD	Remarks
Power-up	1	1	1	
WDT Time-out	u	0	u	No effect on PD
SLEEP instruction	1	1	0	
CLRWDT instruction	u	1	1	
Wake-up from SLEEP on Pin Change	0	u	u	

Legend: u = unchanged

Note: A WDT time-out will occur regardless of the status of the TO bit. A SLEEP instruction will be executed, regardless of the status of the PD bit. Table 7-7 reflects the status of TO and PD after the corresponding event.

Table 7-3 lists the reset conditions for the special function registers, while Table 7-4 lists the reset conditions for all the registers.

7.10 Power-down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

7.10.1 SLEEP

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the TO bit (STATUS<4>) is set, the PD bit (STATUS<3>) is cleared, the PCWUF bit (STATUS<7>) is set and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the MCLR/VPP pin low.

For lowest current consumption while powered down, the T0CKI input should be at VDD or VSS and the MCLR/VPP pin must be at a logic high level (VIH MCLR).

7.10.2 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

1. An external reset input on MCLR/VPP pin.
2. A Watchdog Timer Time-out Reset (if WDT was enabled).
3. A change on input pins PORTB:<0-3,7> when Wake-up on Pin Change is enabled.
4. Brown-out Reset.

These events cause a device RESET. The TO and PD and PCWUF bits can be used to determine the cause of device RESET. The TO bit is cleared if a WDT time-out occurred (and caused wake-up). The PD bit, which is set on power-up, is cleared when SLEEP is invoked.

The PCWUF bit indicates a change in state while in SLEEP at pins PORTB:<0-3,7> (since the SLEEP state was entered).

The WDT is cleared when the device wakes from SLEEP, regardless of the wake-up source.

7.11 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note:	Microchip does not recommend code protecting windowed devices.

7.12 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

Note:	Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code.

SLEEP **Enter SLEEP Mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT;
0 → WDT prescaler;
1 → $\overline{TO}$;
0 → $\overline{PD}$
1→ $\overline{PCWUF}$

Status Affected: $\overline{TO}$, $\overline{PD}$, $\overline{PCWUF}$

Encoding:

0000	0000	0011

Description: Time-out status bit ($\overline{TO}$) is set. The power down status bit ($\overline{PD}$) is cleared. The WDT and its prescaler are cleared.

The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.

Words: 1

Cycles: 1

Example:
```
SLEEP
```

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – (W) → (dest)

Status Affected: C, DC, Z

Encoding:

0000	10df	ffff

Description: Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example 1:
```
SUBWF   REG1, 1
```
Before Instruction
```
REG1    =   3
W       =   2
C       =   ?
```
After Instruction
```
REG1    =   1
W       =   2
C       =   1     ; result is positive
```
Example 2:

Before Instruction
```
REG1    =   2
W       =   2
C       =   ?
```
After Instruction
```
REG1    =   0
W       =   2
C       =   1     ; result is zero
```
Example 3:

Before Instruction
```
REG1    =   1
W       =   2
C       =   ?
```
After Instruction
```
REG1    =   FF
W       =   2
C       =   0     ; result is negative
```


9.0 DEVELOPMENT SUPPORT

The PICmicro® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM Assembler
  - MPLAB-C17 and MPLAB-C18 C Compilers
  - MPLINK/MPLIB Linker/Librarian
- Simulators
  - MPLAB-SIM Software Simulator
- Emulators
  - MPLAB-ICE Real-Time In-Circuit Emulator
  - PICMASTER®/PICMASTER-CE In-Circuit Emulator
  - ICEPIC™
- In-Circuit Debugger
  - MPLAB-ICD for PIC16F877
- Device Programmers
  - PRO MATE® II Universal Programmer
  - PICSTART® Plus Entry-Level Prototype Programmer
- Low-Cost Demonstration Boards
  - SIMICE
  - PICDEM-1
  - PICDEM-2
  - PICDEM-3
  - PICDEM-17
  - SEEVAL®
  - KEELOQ®

9.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a Windows®-based application which contains:

- Multiple functionality
  - editor
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
- A full featured editor
- A project manager
- Customizable tool bar and key mapping
- A status bar
- On-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PICmicro tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - object code

The ability to use MPLAB with Microchip's simulator, MPLAB-SIM, allows a consistent platform and the ability to easily switch from the cost-effective simulator to the full featured emulator with minimal retraining.

9.2 MPASM Assembler

MPASM is a full featured universal macro assembler for all PICmicro MCU's. It can produce absolute code directly in the form of HEX files for device programmers, or it can generate relocatable objects for MPLINK.

MPASM has a command line interface and a Windows shell and can be used as a standalone application on a Windows 3.x or greater system. MPASM generates relocatable object files, Intel standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file which contains source lines and generated machine code, and a COD file for MPLAB debugging.

MPASM features include:

- MPASM and MPLINK are integrated into MPLAB projects.
- MPASM allows user defined macros to be created for streamlined assembly.
- MPASM allows conditional assembly for multi purpose source files.
- MPASM directives allow complete control over the assembly process.

9.3 MPLAB-C17 and MPLAB-C18 C Compilers

The MPLAB-C17 and MPLAB-C18 Code Development Systems are complete ANSI 'C' compilers and integrated development environments for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

10.0 ELECTRICAL CHARACTERISTICS - PIC16HV540

Absolute Maximum Ratings†

Ambient temperature under bias ..... –20°C to +85°C

Storage temperature ..... –65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} ..... 0 to +16V

Voltage on $\overline{MCLR}$ with respect to V_{SS} ..... 0 to +14V

Voltage on all other pins with respect to V_{SS} ..... –0.6V to (V_{DD} + 0.6V)

Total power dissipation(1) ..... 800 mW

Max. current out of V_{SS} pin ..... 150 mA

Max. current into V_{DD} pin ..... 100 mA

Max. current into an input pin (T0CKI only) ..... ±500 µA

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA

Max. output current sunk by any I/O pin ..... 25 mA

Max. output current sourced by any I/O pin ..... 10 mA

Max. output current sourced by a single I/O port A or B ..... 40 mA

Max. output current sourced by a single I/O port A or B ..... 50 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

10.3 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

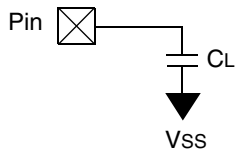
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

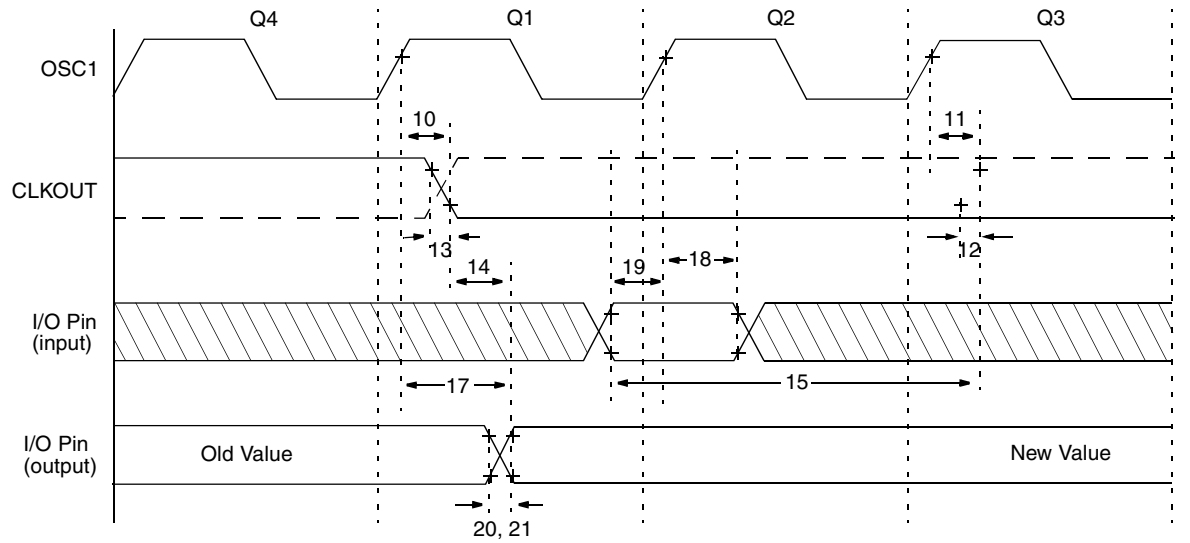
FIGURE 10-1: LOAD CONDITIONS - PIC16HV540



C_L = 50 pF for all pins except OSC2

15 pF for OSC2 in XT, HS or LP options when external clock is used to drive OSC1

FIGURE 10-3: CLKOUT AND I/O TIMING - PIC16HV540



Note: All tests must be done with specified capacitive loads of 50 pF on I/O pins and CLKOUT.

TABLE 10-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16HV540

AC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)				
Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5.0	15**	ns
13	TckF	CLKOUT fall time(2)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at VREG = 5V, VDD = 9V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 8 x TOSC.

3: See Figure 10-1 for loading conditions.

TABLE 10-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16HV540

AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)						
Parameter No.	Sym	Characteristic	Min.	Typ.(1)	Max.	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	2	—	—	µs	VDD = 15V, VREG = 5V
31	Twdt	Watchdog Timer Time-out Period	9.0*	18*	40*	ms	VDD = 15V, VREG = 5V
32	TDRT	Device Reset Timer Period	9.0* 0.55*	18* 1.1*	30* 2.5*	ms	VDD = 15V, VREG = 5V, RC mode
34	TioZ	I/O Hi-impedance from $\overline{MCLR}$ Low	—	—	100*	ns	
—	Tpc	Pin Change Pulse Width	2	—	—	µs	
35	TBOD	Brown-out Detect Pulse Width	—	2	—	µs	VREG ≤ BVDD

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at VREG = 5V, VDD = 15V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 10-6: TIMER0 CLOCK TIMINGS - PIC16HV540

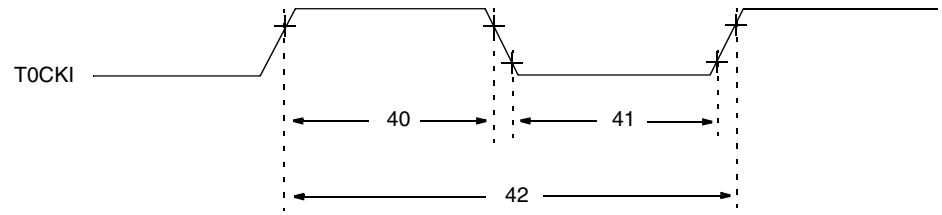


TABLE 10-4: TIMER0 CLOCK REQUIREMENTS - PIC16HV540

AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)						
Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{TCY + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 3.8V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 11-10: MAXIMUM IPD vs. VDD, WATCHDOG TIMER DISABLED (VIO = 3V)

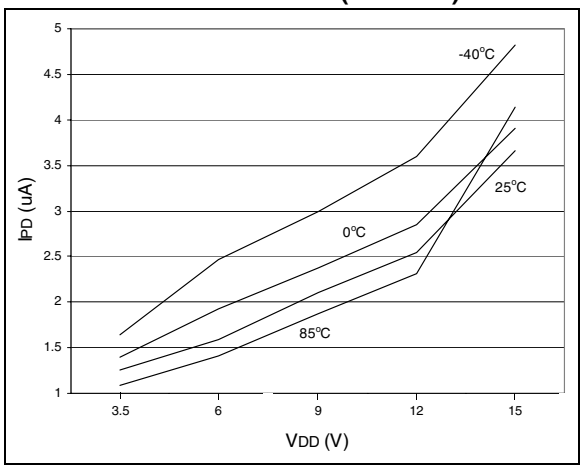


FIGURE 11-11: TYPICAL IPD vs. VDD, WATCHDOG TIMER ENABLED (VIO = 3V)

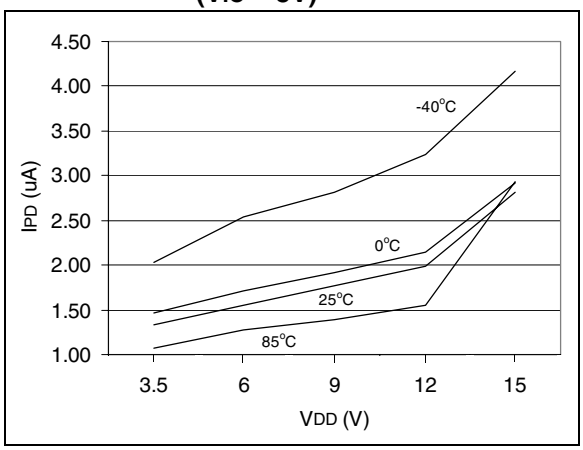


FIGURE 11-12: MAXIMUM IPD vs. VDD, WATCHDOG TIMER ENABLED (VIO = 3V)

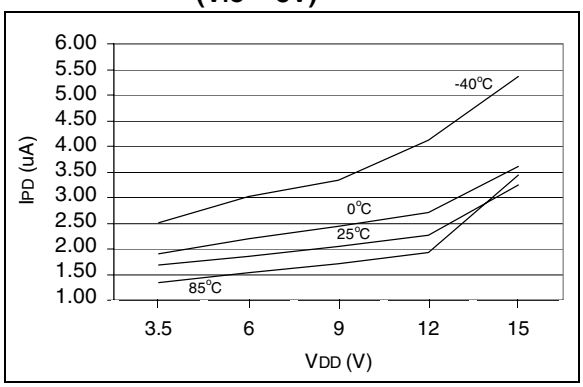


FIGURE 11-13: MAXIMUM IDD vs. FREQUENCY, WATCHDOG TIMER DISABLED, RC MODE (VDD = 15V, VIO = 5V, -40°C TO +85°C)

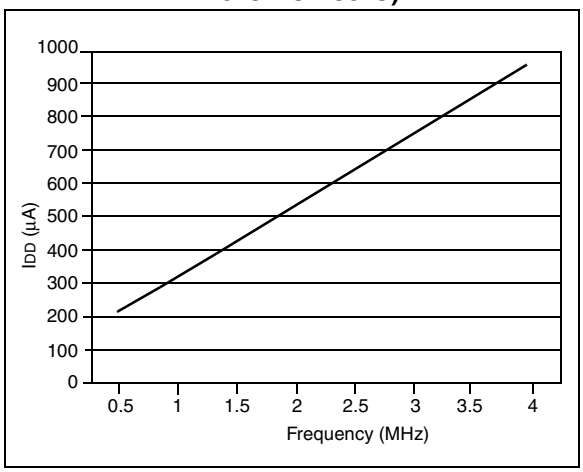
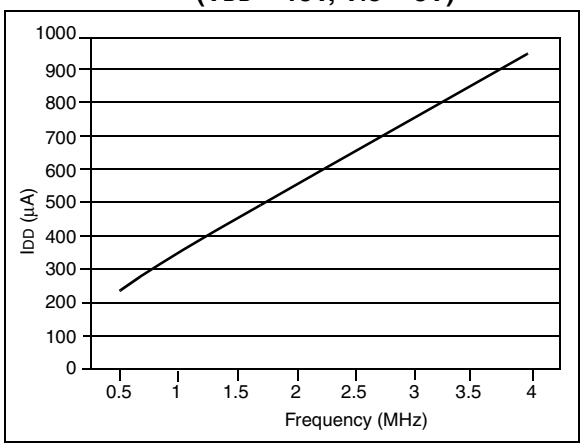


FIGURE 11-14: MAXIMUM IDD vs. FREQUENCY, WATCHDOG TIMER ENABLED, RC MODE (VDD = 15V, VIO = 5V)



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