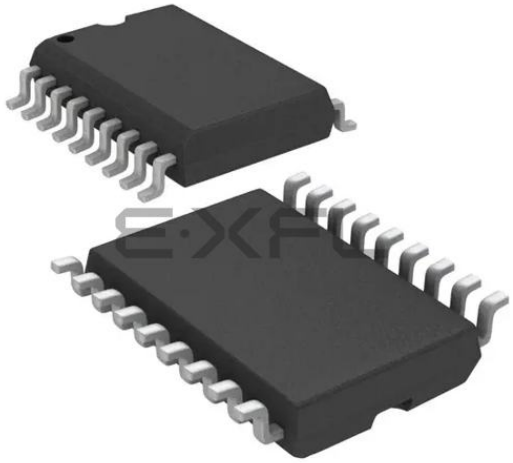

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 15V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16hv540t-20i-so

1.0 GENERAL DESCRIPTION

The PIC16HV540 from Microchip Technology is a low-cost, high-performance, 8-bit, fully-static, EPROM-based CMOS microcontroller. It is pin and software compatible with the PIC16C5X family of devices. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle except for program branches, which take two cycles. The PIC16HV540 delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly orthogonal resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy-to-use and easy-to-remember instruction set reduces development time significantly.

The PIC16HV540 is the first One-Time-Programmable (OTP) microcontroller with an on-chip 3 volt and 5 volt regulator. This eliminates the need for an external regulator in many applications powered from 9 Volt or 12 Volt batteries or unregulated 6 volt, 9 volt or 12 volt mains adapters. The PIC16HV540 is ideally suited for applications that require very low standby current at high voltages. These typically require expensive low current regulators.

The PIC16HV540 is equipped with special features that reduce system cost and power requirements. The Power-On Reset (POR) and Device Reset Timer (DRT) eliminate the need for external reset circuitry. There are four oscillator configurations to choose from, including the power-saving LP (Low Power) oscillator, cost saving RC oscillator, and XT and HS for crystal oscillators. Power saving SLEEP mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The UV erasable CERDIP packaged versions are ideal for code development, while the cost-effective OTP versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers, while benefiting from the OTP's flexibility.

The PIC16HV540 is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer, and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1 Applications

The PIC16HV540 fits in low-power battery applications such as CO and smoke detection, toys, games, security systems and automobile modules. The EPROM technology makes customizing of application programs (transmitter codes, receiver frequencies, etc.) extremely fast and convenient. The small footprint package, for through hole or surface mounting, make this microcontroller suitable for applications with space limitations. Low-cost, low-power, high-performance, ease of use and I/O flexibility make the PIC16HV540 very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, coprocessor applications).

1.2 Enhanced Features

1.2.1 REGULATED I/O PORTA INDEPENDENT OF CORE REGULATOR

PORTA I/O pads and OSC2 output are powered by the regulated internal voltage V_{IO}. A maximum of 10mA per output is allowed, or a total of 40mA. The core itself is powered from the independently regulated supply V_{REG}.

1.2.2 HIGH VOLTAGE I/O PORTB

All eight PORTB I/Os are high voltage I/O. The inputs will tolerate input voltages as high as the V_{DD} and outputs will swing from V_{SS} to the V_{DD}. The input threshold voltages vary with supply voltage. (See Electrical Characteristics.)

1.2.3 WAKE-UP ON PIN CHANGE ON PORTB [0:3]

Four of the PORTB inputs latch the status of the pin at the onset of sleep mode. A level change on the inputs resets the device, implementing wake up on pin change (via warm reset). The $\overline{\text{PCWUF}}$ bit in the status register is reset to indicate that a pin change caused the reset condition. Any pin change (glitch insensitive) of the opposite level of the initial value wakes up the device. This option can be enabled/disabled in OPTION2 register. (See OPTION2 Register, Register 4-3.)

1.2.4 WAKE-UP ON PIN CHANGE WITH A SLOWLY-RISING VOLTAGE ON PORTB [7]

PORTB [7] also implements wake up from sleep, however this input is specifically adapted so that a slowly **rising** voltage does not cause excessive power consumption. This input can be used with external RC circuits for long sleep periods without using the internal timer and prescaler. This option is also enabled/disabled in OPTION2 register. (The enable/disable bit is shared with the other 4 wake-up inputs.) The $\overline{\text{PCWUF}}$ bit in the status register is also shared with the other four wake-up inputs.

1.2.5 LOW-VOLTAGE (BROWN-OUT) DETECTION

A low voltage (Brown-out) detect circuit optionally resets the device at a voltage level higher than that at which the PICmicro® device stops operating. The nominal trip voltages are 3.1 volts (for 5 volt operation) and 2.2 volt (for 3 volt operation), respectively. The core remains in the reset state as long as this condition holds (as if a $\overline{\text{MCLR}}$ external reset was given). The Brown-out trip level is user selectable, with built-in interlocks. The Brown-out detector is disabled at power-up and is activated by clearing the appropriate bit ($\overline{\text{BODEN}}$) in OPTION2 register.

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16HV540 can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16HV540 uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12-bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (200ns @ 20MHz) except for program branches.

The PIC16HV540 address 512 x 12 of program memory. All program memory is internal.

The PIC16HV540 can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC16HV540 has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16HV540 simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16HV540 device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the `SUBWF` and `ADDWF` instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1.

TABLE 3-1: PINOUT DESCRIPTION - PIC16HV540

Name	DIP, SOIC No.	SSOP No.	I/O/P Type	Input Levels	Description	
RA0	17	19	I/O	TTL	Independently regulated Bi-directional I/O port — VIO	
RA1	18	20	I/O	TTL		
RA2	1	1	I/O	TTL		
RA3	2	2	I/O	TTL		
RB0	6	7	I/O	TTL	High-voltage Bi-directional I/O port. Sourced from VDD.	Wake-up on pin change
RB1	7	8	I/O	TTL		
RB2	8	9	I/O	TTL		
RB3	9	10	I/O	TTL		
RB4	10	11	I/O	TTL		
RB5	11	12	I/O	TTL		
RB6	12	13	I/O	TTL		
RB7	13	14	I/O	TTL		Wake-up on SLOW rising pin change.
T0CKI	3	3	I	ST	Clock input to Timer 0. Must be tied to VSS or VDD, if not in use, to reduce current consumption.	
$\overline{MCLR}$/VPP	4	4	I	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device. Voltage on the $\overline{MCLR}$/VPP pin must not exceed VDD(1) to avoid unintended entering of programming mode.	
OSC1/CLKIN	16	18	I	ST	Oscillator crystal input/external clock source input.	
OSC2/CLKOUT	15	17	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2/CLKOUT output is connected to TMR0, bit 0. Frequencies of CLKIN/8 to CLKIN/1024 can be generated on this pin.	
VDD	14	15,16	P	—	Positive supply.	
VSS	5	5,6	P	—	Ground reference.	

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input.

Note 1: VDD during programming mode can not exceed parameter PD1 called out in the PIC16C5X Programming Specification (Literature number DS30190).

TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{MCLR}$ and WDT Reset	Value on Wake-up on Pin Change	Value on Brown-Out Reset
N/A	TRIS	I/O control registers (TRISA, TRISB)								1111 1111	1111 1111	1111 1111	1111 1111
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT prescaler								--11 1111	--11 1111	--11 1111	--11 1111
N/A	OPTION2	Contains control bits to configure pin changes, software enabled WDT, regulation and brown-out								--11 1111	--uu uuuu	--uu uuuu	--xx xxxx
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu	uuuu uuuu	xxxx xxxx
01h	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu	uuuu uuuu	xxxx xxxx
02h(1)	PCL	Low order 8 bits of PC								1111 1111	1111 1111	1111 1111	1111 1111
03h	STATUS	$\overline{PCWUF}$	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	1001 1xxx	100q quuu	000u uuuu	x00x xxxx
04h	FSR	Indirect data memory address pointer								111x xxxx	111u uuuu	111u uuuu	111x xxxx
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu	---- uuuu	---- xxxx
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu	uuuu uuuu	xxxx xxxx

Legend: Shaded boxes = unimplemented or unused, – = unimplemented, read as '0' (if applicable)
x = unknown, u = unchanged, q = value depends on condition.

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 4.6 of the PIC16HV540 data sheet (DS40197B) for an explanation of how to access these bits.

4.6 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

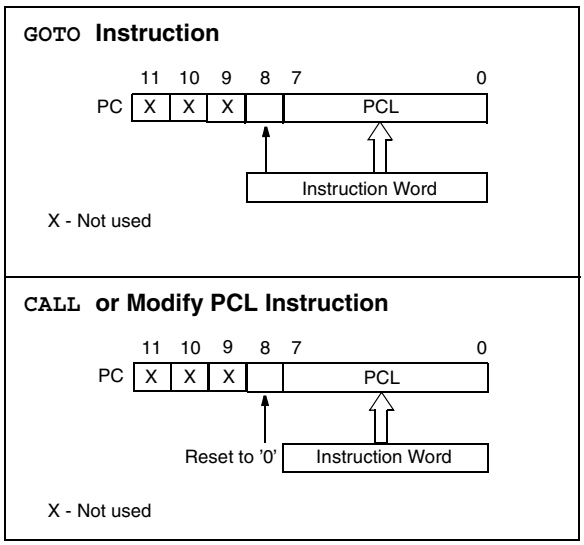
For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. (Figure 4-3).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-3).

Instructions where the PCL is the destination, or Modify PCL instructions, include MOVWF PC, ADDWF PC, and BSF PC, 5. .

Note:	Because PC<8> is cleared in the CALL instruction, or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-3: LOADING OF PC BRANCH INSTRUCTIONS - PIC16HV540



4.6.1 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page i.e., the reset vector.

The STATUS register page preselect bits are cleared upon a RESET, which means that page 0 is preselected.

Therefore, upon a RESET, a GOTO instruction at the reset vector location will automatically cause the program to jump to page 0.

4.7 Stack

PIC16HV540 device has a 12-bit wide L.I.F.O. (last in, first out) hardware 4 level stack.

A CALL instruction will *push* the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than four sequential CALL's are executed, only the most recent four return addresses are stored.

A RETLW instruction will *pop* the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than four sequential RETLW's are executed, the stack will be filled with the address previously stored in level 4. Note that the W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

Upon any reset, the contents of the stack remain unchanged, however the program counter (PCL) will also be reset to 0.

Note 1:	There are no STATUS bits to indicate stack overflows or stack underflow conditions.
Note 2:	There are no instructions mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL and RETLW instructions.

NOTES:

5.0 I/O PORTS

As with any other register, the I/O registers can be written and read under program control. However, read instructions (e.g., `MOVF PORTB,W`) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB) are all set.

5.1 PORTA

PORTA is a 4-bit I/O register. Only the low order 4 bits are used (RA3:RA0). Bits 7-4 are unimplemented and read as '0's. The inputs will tolerate input voltages as high as V_{IO} and outputs will swing from V_{SS} to V_{IO}. The internal voltage regulator V_{IO} powers PORTA I/O pads. The internal regulator output, V_{IO}, is switchable between 3Vdc and 5Vdc, via the (RL) bit in the OPTION2 register.

5.2 PORTB

PORTB is an 8-bit I/O register (PORTB<7:0>). All 8 PORTB I/Os are high voltage I/O. The inputs will tolerate input voltages as high as V_{DD} and outputs will swing from V_{SS} to V_{DD}. In addition, 5 of the PORTB pins can be configured for the wake-up on change feature. Pins RB0, RB1, RB2 and RB3 latch the state of the pin at the onset of sleep mode. (No "dummy" read of the PORTB pins is required prior to executing the `SLEEP` instruction.) A level change on the input resets the device, implementing wake-up on pin change. The $\overline{\text{PCWUF}}$ bit in the status register is cleared to indicate that a pin change caused the reset. This feature can be enabled/disabled in the OPTION2 register.

PORTB pin RB7 also exhibits this wake-up on pin high feature but is specially adapted for a slow-rising input signal. This special feature prevents excessive power consumption when desiring long sleep periods without using the watchdog timer and prescaler. $\overline{\text{PCWUF}}$ bit in the status register is cleared to indicate that a pin change caused the reset. This feature can be enabled/disabled in the OPTION2 register.

Only pins configured as inputs can cause this wake-up on pin change to occur.

To prevent false wake-up on pin change events on pins RB<0:3>, the pin state must be driven to a logic 1 or logic 0 and not left floating during the "`SLEEP`" state. For pin RB7, the pin state must be driven to logic 0 and allowed to ramp to a logic 1 for correct operation.

5.3 TRIS Registers

The output driver control registers are loaded with the contents of the W register by executing the `TRIS f` instruction. A '1' from a TRIS register bit puts the corresponding output driver in a hi-impedance mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

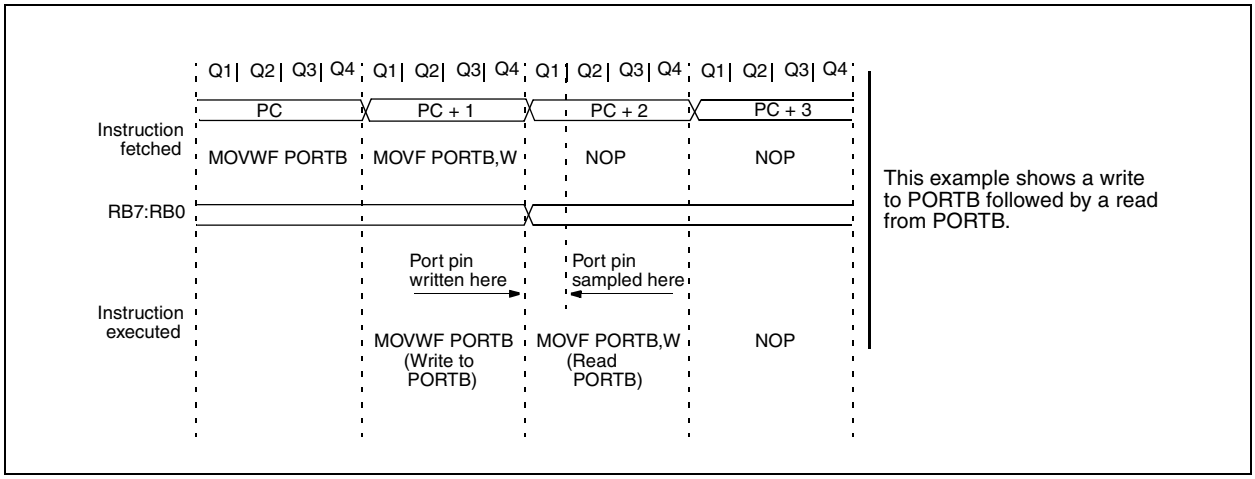
Note:	A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low.

The TRIS registers are "write-only" and are set (output drivers disabled) upon RESET.

5.4 I/O Interfacing

The equivalent circuit for the PORTA and PORTB I/O pins are shown in Figure 5-1 through Figure 5-4. All ports may be used for both input and output operation. For input operations, these ports are non-latching. Any input must be present until read by an input instruction (e.g., `MOVF PORTB, W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

FIGURE 5-5: SUCCESSIVE I/O OPERATION



6.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT) (WDT postscaler not implemented on PIC16C52), respectively (Section 6.1.2). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x`, etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

6.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on the fly” during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

```
1. CLRWDT                ;Clear WDT
2. CLRF     TMR0         ;Clear TMR0 & Prescaler
3. MOVLW    '00xx1111'b  ;These 3 lines (5, 6, 7)
4. OPTION                ; are required only if
                         ; desired
5. CLRWDT                ;PS<2:0> are 000 or 001
6. MOVLW    '00xx1xxx'b  ;Set Postscaler to
7. OPTION                ; desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A `CLRWDT` instruction should be executed before switching the prescaler.

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                   ;Clear WDT and
                         ;prescaler
MOVLW   'xxxx0xxx'       ;Select TMR0, new
                         ;prescale value and
                         ;clock source
OPTION
```

6.3 Programmable Clock Generator

When the PIC16HV540 is programmed to operate in the RC oscillator mode, the CLKOUT pin is connected to the compliment state of TMR0<0>. Use of the prescaler rate select bits PSA:PS0 in the OPTION register will provide for frequencies of CLKIN/8 to CLKIN/1024 on the CLKOUT pin.

EXAMPLE 6-3:

Fosc	PRESCALER SETTING/CLKOUT FREQUENCY	
	CLKIN/1024	CLKIN/8
1Mhz	976 Hz	125 kHz
2Mhz	1953 Hz	250 kHz
3Mhz	2930 Hz	375 kHz
4Mhz	3906 Hz	500 kHz

In addition to this mode of operation, TMR0<0> can be toggled via the bcf and bsf bit type instructions. For this mode, the T0CS bit in the OPTION register must be set to 1. This setting configures TMR0 to increment on the T0CKI pin. To set the CLKOUT pin high, a bcf TMR0,0 instruction is used and to set the CLKOUT pin low, the bsf TMR0,0 instruction is used. The T0CKI pin should be pulled high or low to prevent false state changes on the CLKOUT pin.

7.11 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note:	Microchip does not recommend code protecting windowed devices.

7.12 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

Note:	Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code.

BSF **Bit Set f**

Syntax: [*label*] BSF f,b

Operands: 0 ≤ f ≤ 31
0 ≤ b ≤ 7

Operation: 1 → (f<b>)

Status Affected: None

Encoding:

0101	bbbf	ffff

Description: Bit 'b' in register 'f' is set.

Words: 1

Cycles: 1

Example:
```
BSF     FLAG_REG,   7
```
Before Instruction
FLAG_REG = 0x0A
After Instruction
FLAG_REG = 0x8A

BTFSC **Bit Test f, Skip if Clear**

Syntax: [*label*] BTFSC f,b

Operands: 0 ≤ f ≤ 31
0 ≤ b ≤ 7

Operation: skip if (f<b>) = 0

Status Affected: None

Encoding:

0110	bbbf	ffff

Description: If bit 'b' in register 'f' is 0 then the next instruction is skipped.
If bit 'b' is 0 then the next instruction fetched during the current instruction execution is discarded, and an NOP is executed instead, making this a 2 cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address (HERE)
After Instruction
if FLAG<1> = 0,
PC = address (TRUE);
if FLAG<1> = 1,
PC = address (FALSE)

BTFSS **Bit Test f, Skip if Set**

Syntax: [*label*] BTFSS f,b

Operands: 0 ≤ f ≤ 31
0 ≤ b < 7

Operation: skip if (f<b>) = 1

Status Affected: None

Encoding:

0111	bbbf	ffff

Description: If bit 'b' in register 'f' is '1' then the next instruction is skipped.
If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and an NOP is executed instead, making this a 2 cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    BTFSS   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address (HERE)
After Instruction
If FLAG<1> = 0,
PC = address (FALSE);
if FLAG<1> = 1,
PC = address (TRUE)

COMF **Complement f**

Syntax: [*label*] COMF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(\bar{f}) \rightarrow (dest)$

Status Affected: Z

Encoding:

0010	01df	ffff

Description: The contents of register 'f' are complemented. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
COMF    REG1,0
```
Before Instruction
REG1 = 0x13

After Instruction
REG1 = 0x13
W = 0xEC

DECF **Decrement f**

Syntax: [*label*] DECF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(f) - 1 \rightarrow (dest)$

Status Affected: Z

Encoding:

0000	11df	ffff

Description: Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
DECF    CNT,    1
```
Before Instruction
CNT = 0x01
Z = 0

After Instruction
CNT = 0x00
Z = 1

DECFSZ **Decrement f, Skip if 0**

Syntax: [*label*] DECFSZ f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(f) - 1 \rightarrow d$; skip if result = 0

Status Affected: None

Encoding:

0010	11df	ffff

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

If the result is 0, the next instruction, which is already fetched, is discarded and an NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE      DECFSZ    CNT, 1
          GOTO      LOOP
CONTINUE  •
          •
          •
```
Before Instruction
PC = address (HERE)

After Instruction
CNT = CNT - 1;
if CNT = 0,
PC = address (CONTINUE);
if CNT ≠ 0,
PC = address (HERE+1)

GOTO **Unconditional Branch**

Syntax: [*label*] GOTO k

Operands: $0 \le k \le 511$

Operation: $k \rightarrow PC<8:0>$;
$STATUS<6:5> \rightarrow PC<10:9>$

Status Affected: None

Encoding:

101k	kkkk	kkkk

Description: GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two cycle instruction.

Words: 1

Cycles: 2

Example:
```
GOTO THERE
```
After Instruction
PC = address (THERE)

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f<3:0>) → (dest<7:4>);
(f<7:4>) → (dest<3:0>)

Status Affected: None

Encoding:

0011	10df	ffff

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Example
```
SWAPF   REG1,  0
```
Before Instruction
REG1 = 0xA5
After Instruction
REG1 = 0xA5
W = 0X5A

TRIS **Load TRIS Register**

Syntax: [*label*] TRIS f

Operands: f = 5, 6 or 7

Operation: (W) → TRIS register f

Status Affected: None

Encoding:

0000	0000	0fff

Description: TRIS register 'f' (f = 5, 6, or 7*) is loaded with the contents of the W register

Words: 1

Cycles: 1

Example
```
TRIS    PORTA
```
Before Instruction
W = 0XA5
After Instruction
TRISA = 0XA5

*A TRIS 7 operation will update the OPTION2 SFR.

XORLW **Exclusive OR literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Encoding:

1111	kkkk	kkkk

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example
```
XORLW           0xAF
```
Before Instruction
W = 0xB5
After Instruction
W = 0x1A

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (dest)

Status Affected: Z

Encoding:

0001	10df	ffff

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example
```
XORWF  REG,1
```
Before Instruction
REG = 0xAF
W = 0xB5
After Instruction
REG = 0x1A
W = 0xB5

9.0 DEVELOPMENT SUPPORT

The PICmicro® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM Assembler
  - MPLAB-C17 and MPLAB-C18 C Compilers
  - MPLINK/MPLIB Linker/Librarian
- Simulators
  - MPLAB-SIM Software Simulator
- Emulators
  - MPLAB-ICE Real-Time In-Circuit Emulator
  - PICMASTER®/PICMASTER-CE In-Circuit Emulator
  - ICEPIC™
- In-Circuit Debugger
  - MPLAB-ICD for PIC16F877
- Device Programmers
  - PRO MATE® II Universal Programmer
  - PICSTART® Plus Entry-Level Prototype Programmer
- Low-Cost Demonstration Boards
  - SIMICE
  - PICDEM-1
  - PICDEM-2
  - PICDEM-3
  - PICDEM-17
  - SEEVAL®
  - KEELOQ®

9.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a Windows®-based application which contains:

- Multiple functionality
  - editor
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
- A full featured editor
- A project manager
- Customizable tool bar and key mapping
- A status bar
- On-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PICmicro tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - object code

The ability to use MPLAB with Microchip's simulator, MPLAB-SIM, allows a consistent platform and the ability to easily switch from the cost-effective simulator to the full featured emulator with minimal retraining.

9.2 MPASM Assembler

MPASM is a full featured universal macro assembler for all PICmicro MCU's. It can produce absolute code directly in the form of HEX files for device programmers, or it can generate relocatable objects for MPLINK.

MPASM has a command line interface and a Windows shell and can be used as a standalone application on a Windows 3.x or greater system. MPASM generates relocatable object files, Intel standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file which contains source lines and generated machine code, and a COD file for MPLAB debugging.

MPASM features include:

- MPASM and MPLINK are integrated into MPLAB projects.
- MPASM allows user defined macros to be created for streamlined assembly.
- MPASM allows conditional assembly for multi purpose source files.
- MPASM directives allow complete control over the assembly process.

9.3 MPLAB-C17 and MPLAB-C18 C Compilers

The MPLAB-C17 and MPLAB-C18 Code Development Systems are complete ANSI 'C' compilers and integrated development environments for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

9.4 MPLINK/MPLIB Linker/Librarian

MPLINK is a relocatable linker for MPASM and MPLAB-C17 and MPLAB-C18. It can link relocatable objects from assembly or C source files along with pre-compiled libraries using directives from a linker script.

MPLIB is a librarian for pre-compiled code to be used with MPLINK. When a routine from a library is called from another source file, only the modules that contains that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. MPLIB manages the creation and modification of library files.

MPLINK features include:

- MPLINK works with MPASM and MPLAB-C17 and MPLAB-C18.
- MPLINK allows all memory areas to be defined as sections to provide link-time flexibility.

MPLIB features include:

- MPLIB makes linking easier because single libraries can be included instead of many smaller files.
- MPLIB helps keep code maintainable by grouping related modules together.
- MPLIB commands allow libraries to be created and modules to be added, listed, replaced, deleted, or extracted.

9.5 MPLAB-SIM Software Simulator

The MPLAB-SIM Software Simulator allows code development in a PC host environment by simulating the PICmicro series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file or user-defined key press to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C17 and MPLAB-C18 and MPASM. The Software Simulator offers the flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

9.6 MPLAB-ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB-ICE Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers (MCUs). Software control of MPLAB-ICE is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, “make” and download, and source debugging from a single environment.

Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB-ICE allows expansion to support new PICmicro microcontrollers.

The MPLAB-ICE Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft® Windows 3.x/95/98 environment were chosen to best make these features available to you, the end user.

MPLAB-ICE 2000 is a full-featured emulator system with enhanced trace, trigger, and data monitoring features. Both systems use the same processor modules and will operate across the full operating speed range of the PICmicro MCU.

9.7 PICMASTER/PICMASTER CE

The PICMASTER system from Microchip Technology is a full-featured, professional quality emulator system. This flexible in-circuit emulator provides a high-quality, universal platform for emulating Microchip 8-bit PICmicro microcontrollers (MCUs). PICMASTER systems are sold worldwide, with a CE compliant model available for European Union (EU) countries.

9.8 ICEPIC

ICEPIC is a low-cost in-circuit emulation solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X, and PIC16CXXX families of 8-bit one-time-programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules or daughter boards. The emulator is capable of emulating without target application circuitry being present.

9.9 MPLAB-ICD In-Circuit Debugger

Microchip’s In-Circuit Debugger, MPLAB-ICD, is a powerful, low-cost run-time development tool. This tool is based on the flash PIC16F877 and can be used to develop for this and other PICmicro microcontrollers from the PIC16CXXX family. MPLAB-ICD utilizes the In-Circuit Debugging capability built into the PIC16F87X. This feature, along with Microchip’s In-Circuit Serial Programming protocol, offers cost-effective in-circuit flash programming and debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time. The MPLAB-ICD is also a programmer for the flash PIC16F87X family.

10.1 DC Characteristics: PIC16HV540-04, 20 (Commercial) PIC16HV540-04I, 20I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym.**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
Supply Voltage	VDD	3.5 4.5		15 15	V V	LP, XT and RC modes HS mode
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See section on Power-on Reset for details.
VDD rise rate to ensure Power-on Reset	SVDD	0.05 VDD			V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) HS option XT and RC(4) options LP option	IDD	 — — —	 5 1.8 300	 20 3.3 500	 mA mA µA	 FOSC = 20 MHz, VDD = 15V, VREG = 5V FOSC = 4 MHz, VDD = 15V, VREG = 5V FOSC = 32 kHz, VDD = 15V, VREG = 5V, WDT disabled
Power-down Current(5)(6)	IPD	 — — — —	 4.5 0.25 1.8 1.4	 20 14 10 5	 µA µA µA µA	 VDD = 15V, VREG = 5V sleep timer enable, BOD disabled VDD = 15V, VREG = 3V sleep timer enable, BOD disabled VDD = 15V, VREG = 5V sleep timer disabled, BOD disabled VDD = 15V, VREG = 3V sleep timer disabled, BOD disabled
Brown-out Current		—	0.5	—	µA	VDD = 15V, VREG = 5V, BOD enabled
Brown-out Detector Threshold	BVDD	2.7 1.8	3.1 2.2	4.2 2.8	V V	VDD = 15V, VREG = 5V* (7) VDD = 15V, VREG = 3V* (7)
Regulation Voltage	VIO	2 4	3 5	4.5 6	V V	VDD = 15V, VREG = 3V, Unloaded outputs, SLEEP VDD = 15V, VREG = 5V, Unloaded outputs, SLEEP

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

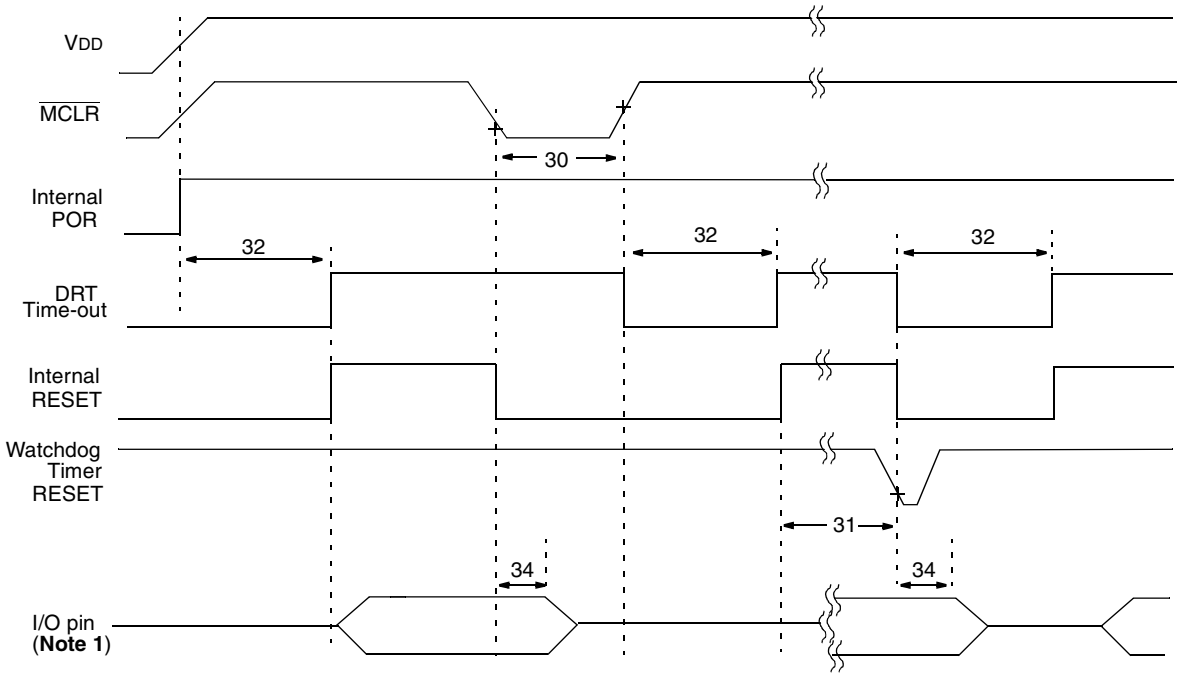
4: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

6: The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection, if the SLEEP mode is exited or during initial power-up.

7: See Section 7.6.1 for additional information.

FIGURE 10-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16HV540



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

FIGURE 10-5: BROWN-OUT DETECT TIMING

TABLE 10-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16HV540

AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)						
Parameter No.	Sym	Characteristic	Min.	Typ.(1)	Max.	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	2	—	—	µs	VDD = 15V, VREG = 5V
31	Twdt	Watchdog Timer Time-out Period	9.0*	18*	40*	ms	VDD = 15V, VREG = 5V
32	TDRT	Device Reset Timer Period	9.0* 0.55*	18* 1.1*	30* 2.5*	ms	VDD = 15V, VREG = 5V, RC mode
34	TioZ	I/O Hi-impedance from $\overline{MCLR}$ Low	—	—	100*	ns	
—	Tpc	Pin Change Pulse Width	2	—	—	µs	
35	TBOD	Brown-out Detect Pulse Width	—	2	—	µs	VREG ≤ BVDD

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at VREG = 5V, VDD = 15V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 10-6: TIMER0 CLOCK TIMINGS - PIC16HV540

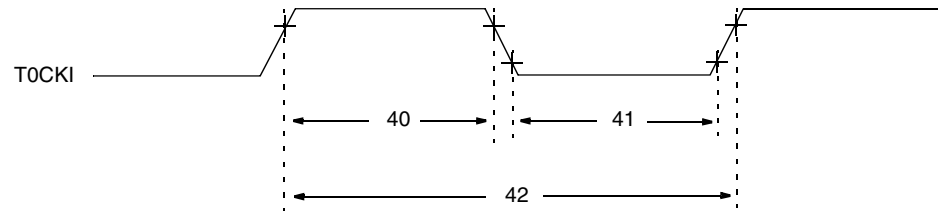


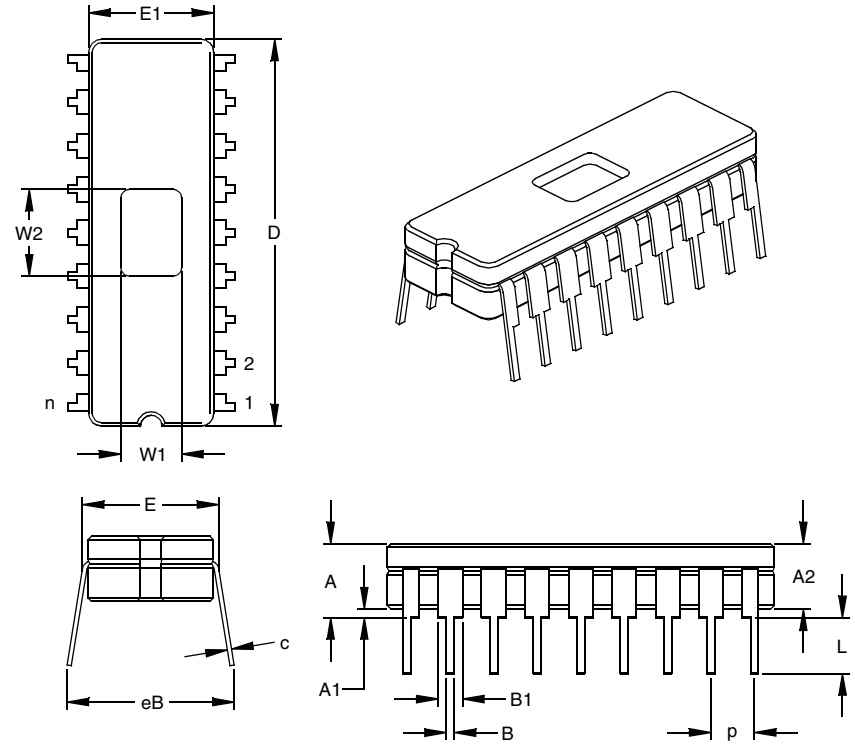
TABLE 10-4: TIMER0 CLOCK REQUIREMENTS - PIC16HV540

AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)						
Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{TCY + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 3.8V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

12.3 18-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)

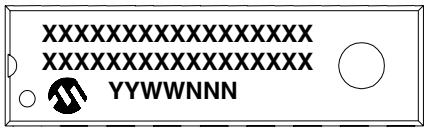


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.170	.183	.195	4.32	4.64	4.95
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.023	.030	0.38	0.57	0.76
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Ceramic Pkg. Width	E1	.285	.290	.295	7.24	7.37	7.49
Overall Length	D	.880	.900	.920	22.35	22.86	23.37
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81
Lead Thickness	c	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.055	.060	1.27	1.40	1.52
Lower Lead Width	B	.016	.019	.021	0.41	0.47	0.53
Overall Row Spacing §	eB	.345	.385	.425	8.76	9.78	10.80
Window Width	W1	.130	.140	.150	3.30	3.56	3.81
Window Length	W2	.190	.200	.210	4.83	5.08	5.33

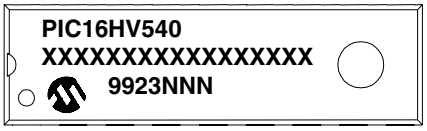
* Controlling Parameter
§ Significant Characteristic
JEDEC Equivalent: MO-036
Drawing No. C04-010

12.5 Package Marking Information

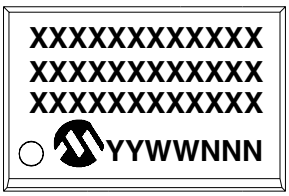
18-Lead PDIP



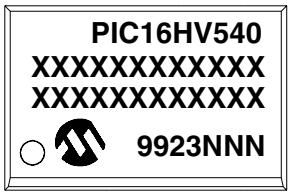
Example



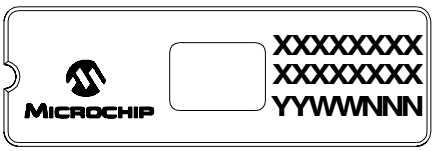
18-Lead SOIC



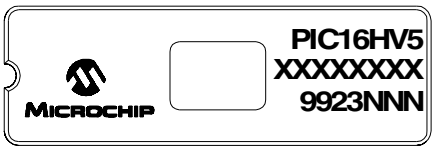
Example



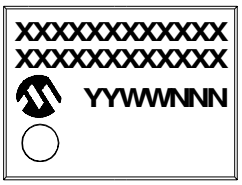
18-Lead CERDIP Windowed



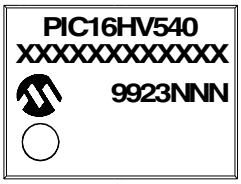
Example



20-Lead SSOP



Example



Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.