Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 15V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16hv540t-20i-ss

2.0 PIC16HV540 DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC16HV540 Product Identification System at the back of this data sheet to specify the correct part number.

For the PIC16HV540 family of devices, there is one device type, as indicated in the device number:

1. **HV**, as in PIC16HV540. These devices have EPROM program memory and operate over the standard voltage range of 3.5 to 15 volts.

2.1 UV Erasable Devices

The UV erasable versions, offered in CERDIP packages, are optimal for prototype development and pilot programs.

UV erasable devices can be programmed for any of the four oscillator configurations. Microchip's PICSTART® and PRO MATE® programmers both support programming of the PIC16HV540. Third party programmers also are available; refer to Literature Number DS00104 for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. (Please contact your Microchip Technology sales office for more details.)

2.4 Serialized Quick-Turnaround-Production (SQTP) Devices

Microchip offers the unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry code, password or ID number. (Please contact your Microchip Technology sales office for more details.)

4.0 MEMORY ORGANIZATION

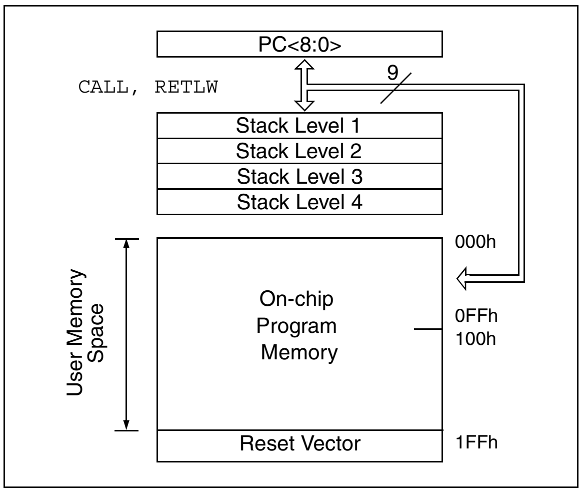
PIC16HV540 memory is organized into program memory and data memory. For devices with more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using one or two STATUS register bits. For devices with a data memory register file of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Selection Register (FSR).

4.1 Program Memory Organization

The PIC16HV540 has a 9-bit Program Counter (PC) capable of addressing a 512 x 12 program memory space (Figure 4-1). Accessing a location above the physically implemented address will cause a wrap-around.

The reset vector for the PIC16HV540 is at 1FFh. A NOP at the reset vector location will cause a restart at location 000h.

FIGURE 4-1: PIC16HV540 PROGRAM MEMORY MAP AND STACK



4.2 Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: special function registers and general purpose registers.

The special function registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports), and the File Select Register (FSR). In addition, special purpose registers are used to control the I/O port configuration and prescaler options.

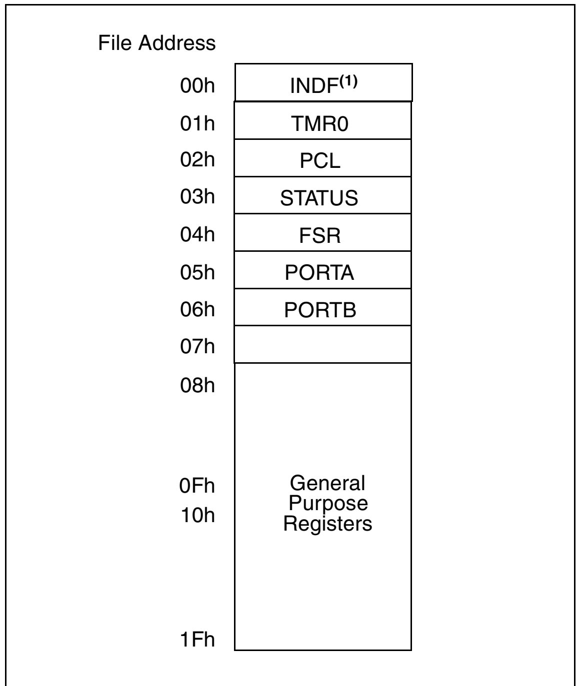
The general purpose registers are used for data and control information under command of the instructions.

For the PIC16HV540, the register file is composed of 10 special function registers and 25 general purpose registers (Figure 4-2).

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is accessed either directly or indirectly through the file select register FSR (Section 4.8).

FIGURE 4-2: PIC16HV540 REGISTER FILE MAP



Note 1: Not a physical register.

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The special registers can be classified into two sets. The special function registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

4.6 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

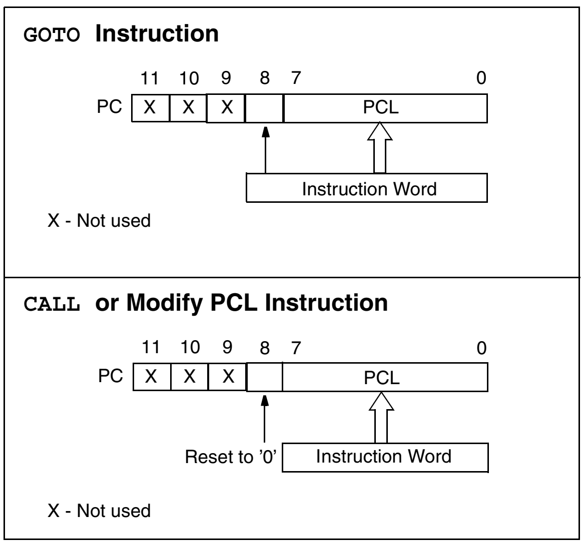
For a `GOTO` instruction, bits 8:0 of the PC are provided by the `GOTO` instruction word. (Figure 4-3).

For a `CALL` instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-3).

Instructions where the PCL is the destination, or Modify PCL instructions, include `MOVWF PC`, `ADDWF PC`, and `BSF PC, 5.` .

Note:	Because PC<8> is cleared in the `CALL` instruction, or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-3: LOADING OF PC BRANCH INSTRUCTIONS - PIC16HV540



4.6.1 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page i.e., the reset vector.

The STATUS register page preselect bits are cleared upon a RESET, which means that page 0 is preselected.

Therefore, upon a RESET, a `GOTO` instruction at the reset vector location will automatically cause the program to jump to page 0.

4.7 Stack

PIC16HV540 device has a 12-bit wide L.I.F.O. (last in, first out) hardware 4 level stack.

A `CALL` instruction will *push* the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than four sequential `CALL`'s are executed, only the most recent four return addresses are stored.

A `RETLW` instruction will *pop* the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than four sequential `RETLW`'s are executed, the stack will be filled with the address previously stored in level 4. Note that the W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

Upon any reset, the contents of the stack remain unchanged, however the program counter (PCL) will also be reset to 0.

Note 1:	There are no STATUS bits to indicate stack overflows or stack underflow conditions.
Note 2:	There are no instructions mnemonics called PUSH or POP. These are actions that occur from the execution of the `CALL` and `RETLW` instructions.

 Preliminary

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{\text{MCLR}}$ and WDT Reset	Value on Wake-up on Pin Change	Value on Brown-Out Reset
N/A	TRIS	I/O control registers (TRISA, TRISB)								1111 1111	1111 1111	1111 1111	1111 1111
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu	---- uuuu	---- xxxx
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu	uuuu uuuu	xxxx xxxx
03h	STATUS	$\overline{\text{PCWUF}}$	PA1	PA0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	100x xxxx	100q quuu	000u uuuu	x00x xxxx
N/A	OPTION2	—	—	$\overline{\text{PCWU}}$	$\overline{\text{SWDTEN}}$	RL	SL	BODL	$\overline{\text{BODEN}}$	--11 1111	--uu uuuu	--uu uuuu	--xx xxxx

Legend: Shaded boxes = unimplemented, read as '0', —= unimplemented, read as '0', x = unknown, u = unchanged.

5.5 I/O Programming Considerations

5.5.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The `BCF` and `BSF` instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a `BSF` operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., `BCF`, `BSF`, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

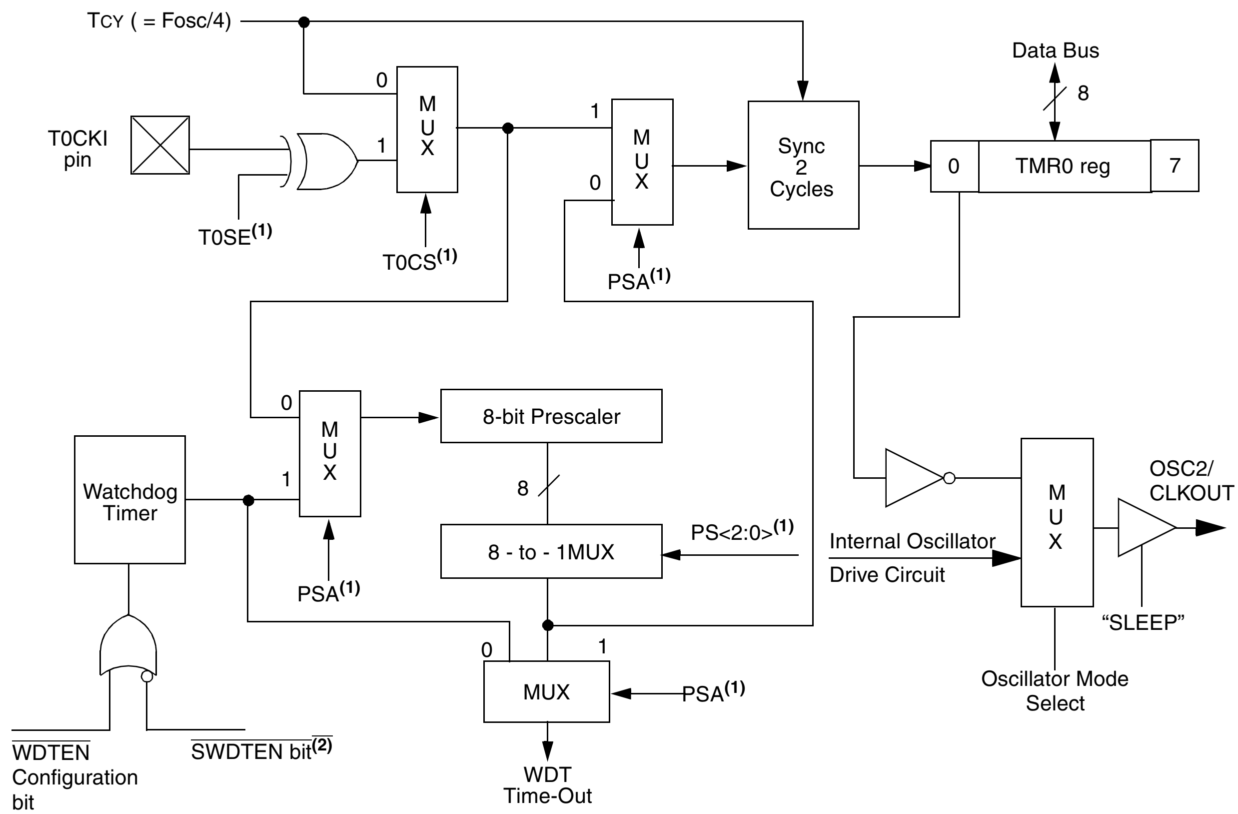
```
;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                    PORT latch  PORT pins
;                     ----------  ----------
  BCF   PORTB, 7   ;01pp pppp   11pp pppp
  BCF   PORTB, 6   ;10pp pppp   11pp pppp
  MOVLW 03Fh       ;
  TRIS  PORTB      ;10pp pppp   10pp pppp
;
;Note that the user may have expected the pin
;values to be 00pp pppp. The 2nd BCF caused
;RB7 to be latched as the pin value (High).
```

5.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-5). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a `NOP` or another instruction not accessing this I/O port.

NOTES:

FIGURE 6-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note 1: T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

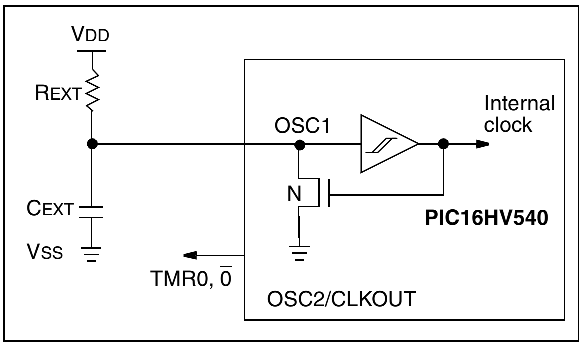
2: $\overline{\text{SWDTEN}}$ is a bit in the OPTION2 register.

The Electrical Specifications sections show RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

Also, see the Electrical Specifications sections for variation of oscillator frequency due to V_{DD} for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and V_{DD} values.

When used in RC mode, the CLKOUT pin can be used as a programmable clock output. The output is connected to TMR0, bit 0, and by setting the prescaler rate select bits, clock out frequencies of CLKIN/8 to CLKIN/1024 can be generated.

FIGURE 7-5: RC OSCILLATOR MODE



Note:	If you change from this device to another device, please verify oscillator characteristics in your application.

7.3 Reset

PIC16HV540 devices may be reset in one of the following ways:

- Power-On Reset (POR)
- $\overline{MCLR}$ reset (normal operation)
- $\overline{MCLR}$ wake-up reset (from SLEEP)
- WDT reset (normal operation)
- WDT wake-up reset (from SLEEP)
- Wake-up from SLEEP on Pin Change
- Brown-out Detect

Table 7-3 shows these reset conditions for the PCL and STATUS registers.

Some registers are not affected in any reset condition. Their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a “reset state” on Power-On Reset (POR), $\overline{MCLR}$ or WDT Reset. A $\overline{MCLR}$, WDT Wake-up from SLEEP or Wake-up from SLEEP on Pin Change also results in a device RESET, and not a continuation of operation before SLEEP.

The $\overline{TO}$ and $\overline{PD}$ bits (STATUS <4:3>) and $\overline{PCWUF}$ (STATUS<7>) are set or cleared depending on the different reset conditions (Section 7.9). These bits may be used to determine the nature of the reset.

Table 7-4 lists a full description of reset states of all registers. Figure 7-6 shows a simplified block diagram of the on-chip reset circuit.

7.9 Time-out Sequence and Power-down Status Bits ($\overline{TO}$/$\overline{PD}$/$\overline{PCWUF}$)

The $\overline{TO}$, $\overline{PD}$ and $\overline{PCWUF}$ bits in the STATUS register can be tested to determine if a RESET condition has been caused by a power-up condition, a $\overline{MCLR}$, Watchdog Timer (WDT) Reset, WDT Wake-up Reset, or Wake-up from SLEEP on Pin Change.

TABLE 7-7: $\overline{TO}$/$\overline{PD}$/$\overline{PCWUF}$ STATUS AFTER RESET

$\overline{PCWUF}$	$\overline{TO}$	$\overline{PD}$	RESET was caused by
1	1	1	Power-up (POR)
u	u	u	$\overline{MCLR}$ Reset (normal operation)(1)
u	1	0	$\overline{MCLR}$ Wake-up Reset (from SLEEP)
u	0	1	WDT Reset (normal operation)
u	0	0	WDT Wake-up Reset (from SLEEP)
0	u	u	Wake-up from SLEEP on Pin Change
x	x	x	Brown-out Reset

Legend: u = unchanged, x = unknown

Note 1: The $\overline{TO}$ and $\overline{PD}$ and $\overline{PCWUF}$ bits maintain their status (u) until a reset occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{TO}$ and $\overline{PD}$ and $\overline{PCWUF}$ status bits.

These STATUS bits are only affected by events listed in Table 7-8.

TABLE 7-8: EVENTS AFFECTING $\overline{TO}$/$\overline{PD}$ STATUS BITS

Event	$\overline{PCWUF}$	$\overline{TO}$	$\overline{PD}$	Remarks
Power-up	1	1	1	
WDT Time-out	u	0	u	No effect on $\overline{PD}$
`SLEEP` instruction	1	1	0	
`CLRWDT` instruction	u	1	1	
Wake-up from SLEEP on Pin Change	0	u	u	

Legend: u = unchanged

Note: A WDT time-out will occur regardless of the status of the $\overline{TO}$ bit. A `SLEEP` instruction will be executed, regardless of the status of the $\overline{PD}$ bit. Table 7-7 reflects the status of $\overline{TO}$ and $\overline{PD}$ after the corresponding event.

Table 7-3 lists the reset conditions for the special function registers, while Table 7-4 lists the reset conditions for all the registers.

7.10 Power-down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

7.10.1 SLEEP

The Power-down mode is entered by executing a `SLEEP` instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (STATUS<4>) is set, the $\overline{PD}$ bit (STATUS<3>) is cleared, the $\overline{PCWUF}$ bit (STATUS<7>) is set and the oscillator driver is turned off. The I/O ports maintain the status they had before the `SLEEP` instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the $\overline{MCLR}$/V_{PP} pin low.

For lowest current consumption while powered down, the T0CKI input should be at V_{DD} or V_{SS} and the $\overline{MCLR}$/V_{PP} pin must be at a logic high level (V_{IH} $\overline{MCLR}$).

7.10.2 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

1. An external reset input on $\overline{MCLR}$/V_{PP} pin.
2. A Watchdog Timer Time-out Reset (if WDT was enabled).
3. A change on input pins PORTB:<0-3,7> when Wake-up on Pin Change is enabled.
4. Brown-out Reset.

These events cause a device RESET. The $\overline{TO}$ and $\overline{PD}$ and $\overline{PCWUF}$ bits can be used to determine the cause of device RESET. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked.

The $\overline{PCWUF}$ bit indicates a change in state while in SLEEP at pins PORTB:<0-3,7> (since the SLEEP state was entered).

The WDT is cleared when the device wakes from SLEEP, regardless of the wake-up source.

CALL — Subroutine Call

Syntax:	[*label*] CALL k
Operands:	0 ≤ k ≤ 255
Operation:	(PC) + 1→ Top of Stack; k → PC<7:0>; (STATUS<6:5>) → PC<10:9>; 0 → PC<8>
Status Affected:	None
Encoding:	`1001` `kkkk` `kkkk`
Description:	Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. `CALL` is a two cycle instruction.
Words:	1
Cycles:	2
Example:	`HERE CALL THERE`

Before Instruction
PC = address `(HERE)`

After Instruction
PC = address `(THERE)`
TOS = address `(HERE + 1)`

CLRF — Clear f

Syntax:	[*label*] CLRF f
Operands:	0 ≤ f ≤ 31
Operation:	00h → (f); 1 → Z
Status Affected:	Z
Encoding:	`0000` `011f` `ffff`
Description:	The contents of register 'f' are cleared and the Z bit is set.
Words:	1
Cycles:	1
Example:	`CLRF FLAG_REG`

Before Instruction
FLAG_REG = 0x5A

After Instruction
FLAG_REG = 0x00
Z = 1

CLRW — Clear W

Syntax:	[*label*] CLRW
Operands:	None
Operation:	00h → (W); 1 → Z
Status Affected:	Z
Encoding:	`0000` `0100` `0000`
Description:	The W register is cleared. Zero bit (Z) is set.
Words:	1
Cycles:	1
Example:	`CLRW`

Before Instruction
W = 0x5A

After Instruction
W = 0x00
Z = 1

CLRWDT — Clear Watchdog Timer

Syntax:	[*label*] CLRWDT
Operands:	None
Operation:	00h → WDT; 0 → WDT prescaler (if assigned); 1 → $\overline{TO}$; 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Encoding:	`0000` `0000` `0100`
Description:	The `CLRWDT` instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits $\overline{TO}$ and $\overline{PD}$ are set.
Words:	1
Cycles:	1
Example:	`CLRWDT`

Before Instruction
WDT counter = ?

After Instruction
WDT counter = 0x00
WDT prescale = 0
$\overline{TO}$ = 1
$\overline{PD}$ = 1

MOVF — Move f

Syntax:	[*label*] MOVF f,d
Operands:	0 ≤ f ≤ 31 d ∈ [0,1]
Operation:	(f) → (dest)
Status Affected:	Z
Encoding:	`0010` `00df` `ffff`
Description:	The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.
Words:	1
Cycles:	1
Example:	`MOVF FSR, 0`

After Instruction
W = value in FSR register

MOVLW — Move Literal to W

Syntax:	[*label*] MOVLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W)
Status Affected:	None
Encoding:	`1100` `kkkk` `kkkk`
Description:	The eight bit literal 'k' is loaded into the W register. The don't cares will assemble as 0s.
Words:	1
Cycles:	1
Example:	`MOVLW 0x5A`

After Instruction
W = 0x5A

MOVWF — Move W to f

Syntax:	[*label*] MOVWF f
Operands:	0 ≤ f ≤ 31
Operation:	(W) → (f)
Status Affected:	None
Encoding:	`0000` `001f` `ffff`
Description:	Move data from the W register to register 'f'.
Words:	1
Cycles:	1
Example:	`MOVWF TEMP_REG`

Before Instruction
TEMP_REG = 0xFF
W = 0x4F

After Instruction
TEMP_REG = 0x4F
W = 0x4F

NOP — No Operation

Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Encoding:	`0000` `0000` `0000`
Description:	No operation.
Words:	1
Cycles:	1
Example:	`NOP`

OPTION **Load OPTION Register**

Syntax: [*label*] OPTION

Operands: None

Operation: (W) → OPTION

Status Affected: None

Encoding:

0000	0000	0010

Description: The content of the W register is loaded into the OPTION register.

Words: 1

Cycles: 1

Example

```
OPTIO
  N
```

Before Instruction
W = 0x07

After Instruction
OPTION = 0x07

RETLW **Return with Literal in W**

Syntax: [*label*] RETLW k

Operands: $0 \le k \le 255$

Operation: k → (W);
TOS → PC

Status Affected: None

Encoding:

1000	kkkk	kkkk

Description: The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

Words: 1

Cycles: 2

Example:

```
        CALL TABLE ;W contains
                   ;table offset
                   ;value.
        •          ;W now has table
        •          ;value.
        •
TABLE   ADDWF PC   ;W = offset
        RETLW k1   ;Begin table
        RETLW k2   ;
        •
        •
        •
        RETLW kn   ; End of table
```

Before Instruction
W = 0x07

After Instruction
W = value of k8

RLF **Rotate Left f through Carry**

Syntax: [*label*] RLF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

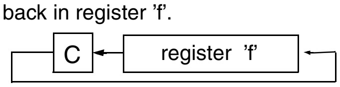
Operation: See description below

Status Affected: C

Encoding:

0011	01df	ffff

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example: `RLF REG1,0`

Before Instruction
REG1 = 1110 0110
C = 0

After Instruction
REG1 = 1110 0110
W = 1100 1100
C = 1

RRF **Rotate Right f through Carry**

Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

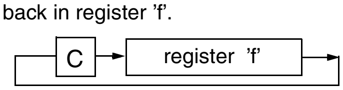
Operation: See description below

Status Affected: C

Encoding:

0011	00df	ffff

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.



Words: 1

Cycles: 1

Example: `RRF REG1,0`

Before Instruction
REG1 = 1110 0110
C = 0

After Instruction
REG1 = 1110 0110
W = 0111 0011
C = 0

SLEEP **Enter SLEEP Mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT;
0 → WDT prescaler;
1 → $\overline{TO}$;
0 → $\overline{PD}$
1→ $\overline{PCWUF}$

Status Affected: $\overline{TO}$, $\overline{PD}$, $\overline{PCWUF}$

Encoding:

0000	0000	0011

Description: Time-out status bit ($\overline{TO}$) is set. The power down status bit ($\overline{PD}$) is cleared. The WDT and its prescaler are cleared.

The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.

Words: 1

Cycles: 1

Example: `SLEEP`

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \leq f \leq 31$
$d \in [0,1]$

Operation: (f) – (W) → (dest)

Status Affected: C, DC, Z

Encoding:

0000	10df	ffff

Description: Subtract (2’s complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example 1: `SUBWF REG1, 1`

Before Instruction
REG1 = 3
W = 2
C = ?

After Instruction
REG1 = 1
W = 2
C = 1 ; result is positive

Example 2:

Before Instruction
REG1 = 2
W = 2
C = ?

After Instruction
REG1 = 0
W = 2
C = 1 ; result is zero

Example 3:

Before Instruction
REG1 = 1
W = 2
C = ?

After Instruction
REG1 = FF
W = 2
C = 0 ; result is negative

10.0 ELECTRICAL CHARACTERISTICS - PIC16HV540

Absolute Maximum Ratings†

Ambient temperature under bias .... –20°C to +85°C
Storage temperature .... –65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} .... 0 to +16V
Voltage on $\overline{MCLR}$ with respect to V_{SS} .... 0 to +14V
Voltage on all other pins with respect to V_{SS} .... –0.6V to (V_{DD} + 0.6V)
Total power dissipation(1) .... 800 mW
Max. current out of V_{SS} pin .... 150 mA
Max. current into V_{DD} pin .... 100 mA
Max. current into an input pin (T0CKI only) .... ±500 μA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) .... ±20 mA
Max. output current sunk by any I/O pin .... 25 mA
Max. output current sourced by any I/O pin .... 10 mA
Max. output current sourced by a single I/O port A or B .... 40 mA
Max. output current sourced by a single I/O port A or B .... 50 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

10.1 DC Characteristics: PIC16HV540-04, 20 (Commercial) PIC16HV540-04I, 20I (Industrial)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)					
Characteristic	**Sym.**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
Supply Voltage	V_{DD}	3.5 4.5	 —	15 15	V V	LP, XT and RC modes HS mode
RAM Data Retention Voltage(2)	V_{DR}	—	1.5*	—	V	Device in SLEEP mode
V_{DD} start voltage to ensure Power-on Reset	V_{POR}	—	V_{SS}	—	V	See section on Power-on Reset for details.
V_{DD} rise rate to ensure Power-on Reset	S_{VDD}	0.05 V_{DD}			V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) HS option XT and RC(4) options LP option	I_{DD}	 — — —	 5 1.8 300	 20 3.3 500	 mA mA µA	 F_{OSC} = 20 MHz, V_{DD} = 15V, V_{REG} = 5V F_{OSC} = 4 MHz, V_{DD} = 15V, V_{REG} = 5V F_{OSC} = 32 kHz, V_{DD} = 15V, V_{REG} = 5V, WDT disabled
Power-down Current(5)(6)	I_{PD}	 — — — —	 4.5 0.25 1.8 1.4	 20 14 10 5	 µA µA µA µA	 V_{DD} = 15V, V_{REG} = 5V sleep timer enable, BOD disabled V_{DD} = 15V, V_{REG} = 3V sleep timer enable, BOD disabled V_{DD} = 15V, V_{REG} = 5V sleep timer disabled, BOD disabled V_{DD} = 15V, V_{REG} = 3V sleep timer disabled, BOD disabled
Brown-out Current		—	0.5	—	µA	V_{DD} = 15V, V_{REG} = 5V, BOD enabled
Brown-out Detector Threshold	B_{VDD}	2.7 1.8	3.1 2.2	4.2 2.8	V V	V_{DD} = 15V, V_{REG} = 5V* (7) V_{DD} = 15V, V_{REG} = 3V* (7)
Regulation Voltage	V_{IO}	2 4	3 5	4.5 6	V V	V_{DD} = 15V, V_{REG} = 3V, Unloaded outputs, SLEEP V_{DD} = 15V, V_{REG} = 5V, Unloaded outputs, SLEEP

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
a) The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{ss}, T0CKI = V_{DD}, $\overline{MCLR}$ = V_{DD}; WDT enabled/disabled as specified.
b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through R_{EXT}. The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} and V_{SS}.

6: The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection, if the SLEEP mode is exited or during initial power-up.

7: See Section 7.6.1 for additional information.

12.5 Package Marking Information

Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

NOTES:

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