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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	27
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21331cdfp-v2

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/33C Group.

Table 1.1 Specifications for R8C/33C Group (1)

Item	Function	Specification

CPU	Central processing unit	R8C CPU core
		• Number of fundamental instructions: 89
		• Minimum instruction execution time:
		   50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)
		   200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V)
		• Multiplier: 16 bits × 16 bits → 32 bits
		• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits
		• Operation mode: Single-chip mode (address space: 1 Mbyte)

Memory	ROM, RAM, Data flash	Refer to **Table 1.3 Product List for R8C/33C Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• Input-only: 1 pin • CMOS I/O ports: 27, selectable pull-up resistor • High current drive ports: 27

Clock	Clock generation circuits	4 circuits: XIN clock oscillation circuit,
		        XCIN clock oscillation circuit (32 kHz),
		        High-speed on-chip oscillator (with frequency adjustment function),
		        Low-speed on-chip oscillator
		• Oscillation stop detection: XIN clock oscillation stop detection function
		• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16
		• Low power consumption modes:
		   Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode

		Real-time clock (timer RE)
Interrupts		• Number of interrupt vectors: 69 • External Interrupt: 7 ($\overline{\text{INT}}$ × 3, Key input × 4) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 23 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RE	8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode

1.2   Product List

Table 1.3 lists Product List for R8C/33C Group, and Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/33C Group.

Table 1.3   Product List for R8C/33C Group   **Current of Aug 2010**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21331CNFP	4 Kbytes	1 Kbyte × 4	512 bytes	PLQP0032GB-A	N version
R5F21332CNFP	8 Kbytes	1 Kbyte × 4	1 Kbyte	PLQP0032GB-A	
R5F21334CNFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0032GB-A	
R5F21335CNFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0032GB-A	
R5F21336CNFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0032GB-A	
R5F21331CDFP	4 Kbytes	1 Kbyte × 4	512 bytes	PLQP0032GB-A	D version
R5F21332CDFP	8 Kbytes	1 Kbyte × 4	1 Kbyte	PLQP0032GB-A	
R5F21334CDFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0032GB-A	
R5F21335CDFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0032GB-A	
R5F21336CDFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0032GB-A	

Part No.   R 5 F 21 33 6 C N FP

Package type:
    FP: PLQP0032GB-A (0.8 mm pin-pitch, 7 mm square body)

Classification
    N: Operating ambient temperature -20°C to 85°C
    D: Operating ambient temperature -40°C to 85°C

ROM capacity
    1: 4 KB
    2: 8 KB
    4: 16 KB
    5: 24 KB
    6: 32 KB

R8C/33C Group

R8C/3x Series

Memory type
    F: Flash memory

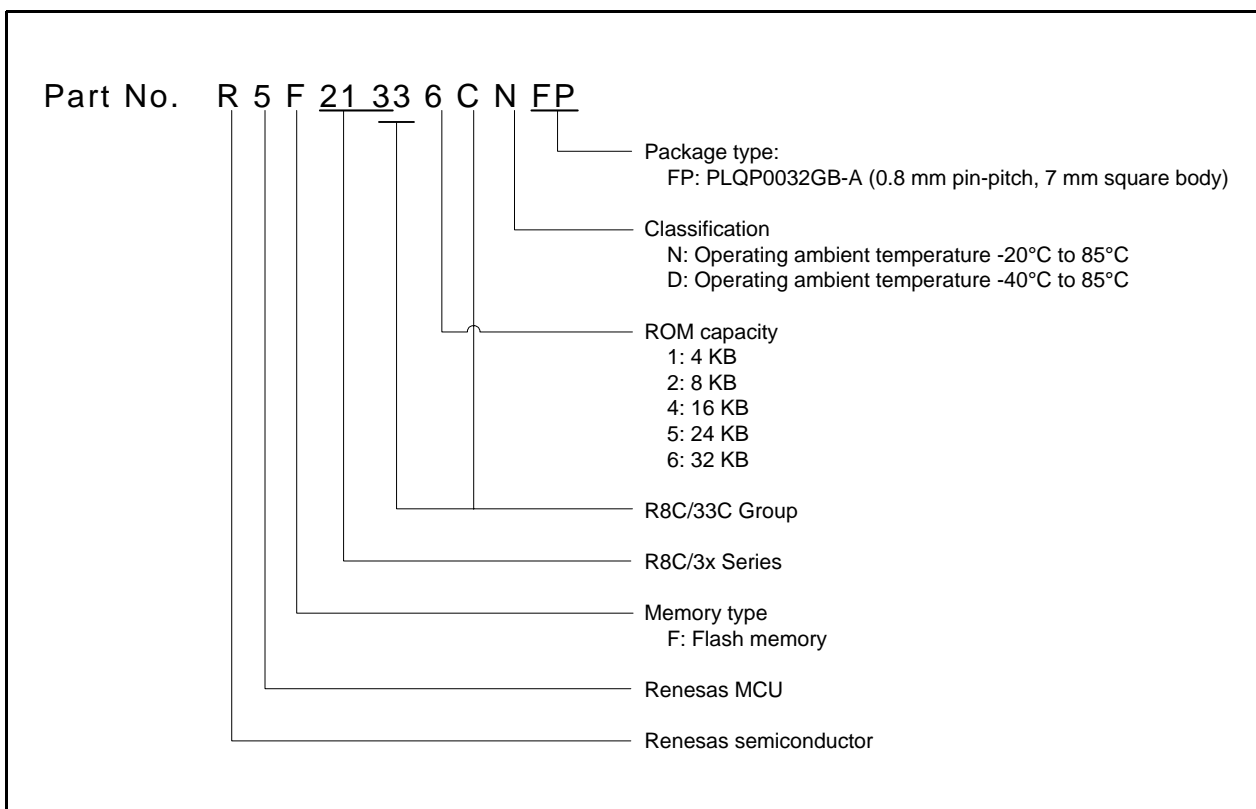Renesas MCU

Renesas semiconductor

Figure 1.1   Part Number, Memory Size, and Package of R8C/33C Group

1.3   Block Diagram
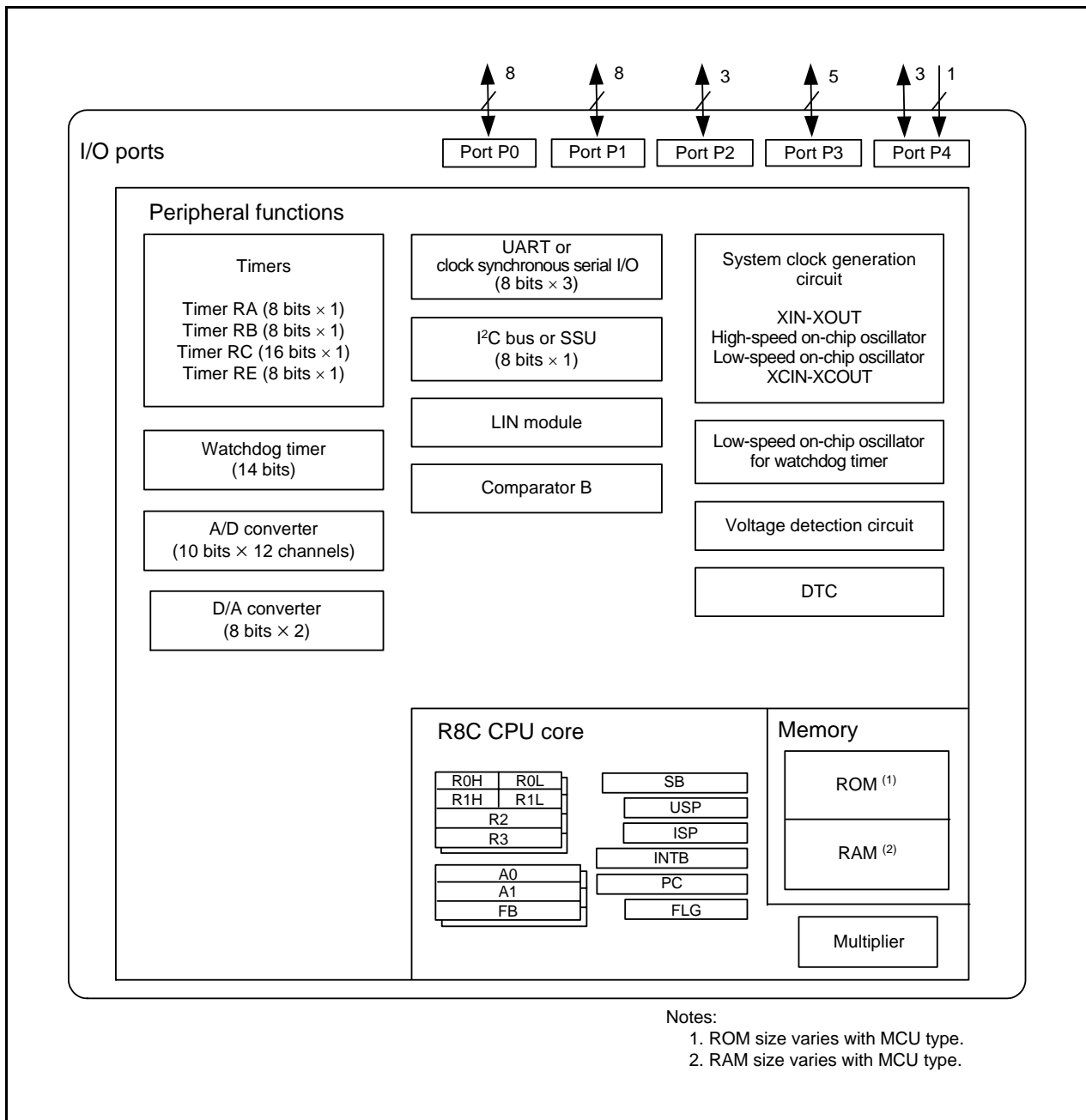
Figure 1.2 shows a Block Diagram.

Figure 1.2   Block Diagram

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Table 1.4 outline the Pin Name Information by Pin Number.
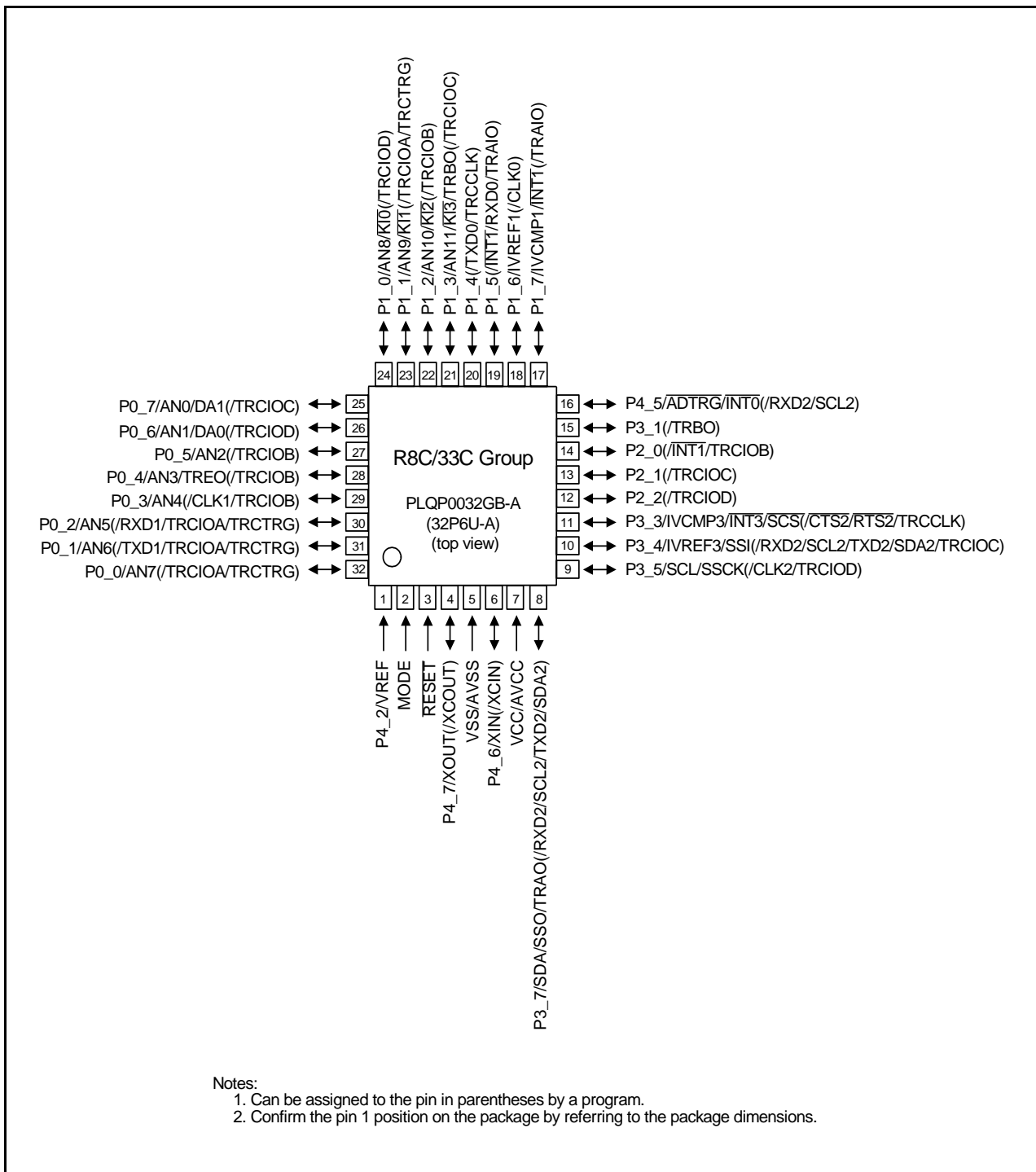

Figure 1.3   Pin Assignment (Top View)

Table 1.4 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I²C bus	A/D Converter, D/A Converter, Comparator B
1		P4_2						VREF
2	MODE							
3	$\overline{\text{RESET}}$							
4	XOUT(/XCOUT)	P4_7						
5	VSS/AVSS							
6	XIN(/XCIN)	P4_6						
7	VCC/AVCC							
8		P3_7		TRAO	(RXD2/SCL2/ TXD2/SDA2)	SSO	SDA	
9		P3_5		(TRCIOD)	(CLK2)	SSCK	SCL	
10		P3_4		(TRCIOC)	(RXD2/SCL2/ TXD2/SDA2)	SSI		IVREF3
11		P3_3	$\overline{\text{INT3}}$	(TRCCLK)	($\overline{\text{CTS2}}/\overline{\text{RTS2}}$)	$\overline{\text{SCS}}$		IVCMP3
12		P2_2		(TRCIOD)				
13		P2_1		(TRCIOC)				
14		P2_0	($\overline{\text{INT1}}$)	(TRCIOB)				
15		P3_1		(TRBO)				
16		P4_5	$\overline{\text{INT0}}$		(RXD2/SCL2)			$\overline{\text{ADTRG}}$
17		P1_7	$\overline{\text{INT1}}$	(TRAIO)				IVCMP1
18		P1_6			(CLK0)			IVREF1
19		P1_5	($\overline{\text{INT1}}$)	(TRAIO)	(RXD0)			
20		P1_4		(TRCCLK)	(TXD0)			
21		P1_3	$\overline{\text{KI3}}$	TRBO (/TRCIOC)				AN11
22		P1_2	$\overline{\text{KI2}}$	(TRCIOB)				AN10
23		P1_1	$\overline{\text{KI1}}$	(TRCIOA/ TRCTRG)				AN9
24		P1_0	$\overline{\text{KI0}}$	(TRCIOD)				AN8
25		P0_7		(TRCIOC)				AN0/DA1
26		P0_6		(TRCIOD)				AN1/DA0
27		P0_5		(TRCIOB)				AN2
28		P0_4		TREO (/TRCIOB)				AN3
29		P0_3		(TRCIOB)	(CLK1)			AN4
30		P0_2		(TRCIOA/ TRCTRG)	(RXD1)			AN5
31		P0_1		(TRCIOA/ TRCTRG)	(TXD1)			AN6
32		P0_0		(TRCIOA/ TRCTRG)				AN7

Note:
1. Can be assigned to the pin in parentheses by a program.

2.   Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.
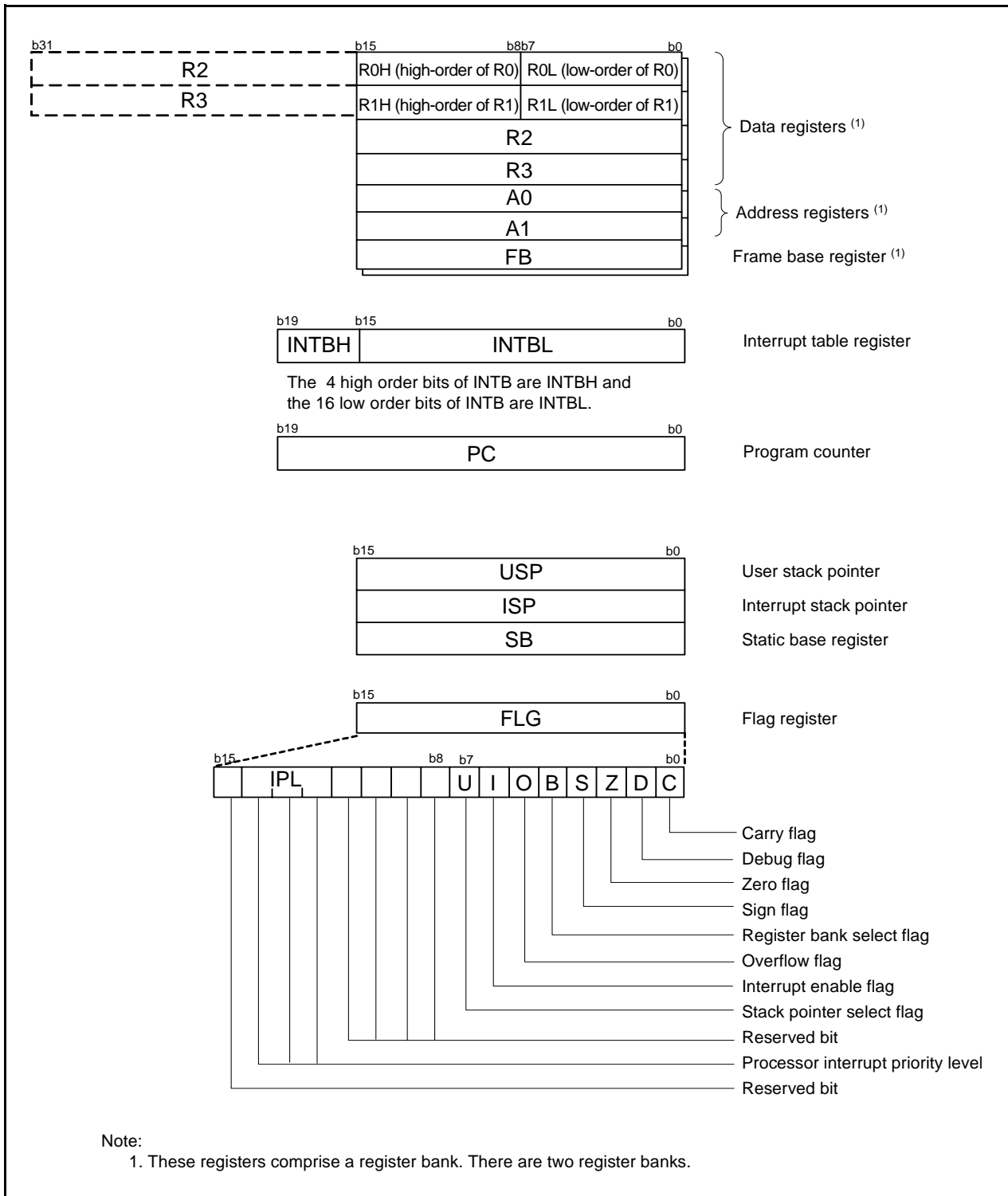

Figure 2.1   CPU Registers

4.   Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers and Table 4.13 lists the ID Code Areas and Option Function Select Area.

Table 4.1   SFR Information (1) [1]

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXXb [2]
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b [3]
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When Shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When Shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h [4] 00100000b [5]
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b [4] 1100X011b [5]
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined
Notes:
1.   The blank areas are reserved and cannot be accessed by users.
2.   The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, Software reset, or watchdog timer reset does not affect this bit.
3.   The CSPROINI bit in the OFS register is set to 0.
4.   The LVDAS bit in the OFS register is set to 1.
5.   The LVDAS bit in the OFS register is set to 0.

Table 4.2   SFR Information (2) [1]

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register [2]	SSUIC / IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:
1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.3   SFR Information (3) [1]

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch			
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.6 **SFR Information (6)** [1]

Address	Register	Symbol	After Reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h	UART1 Transmit/Receive Mode Register	U1MR	00h
0161h	UART1 Bit Rate Register	U1BRG	XXh
0162h	UART1 Transmit Buffer Register	U1TB	XXh
0163h			XXh
0164h	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
0165h	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
0166h	UART1 Receive Buffer Register	U1RB	XXh
0167h			XXh
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.11   SFR Information (11) [1]

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined
Note:
  1.   The blank areas are reserved and cannot be accessed by users.

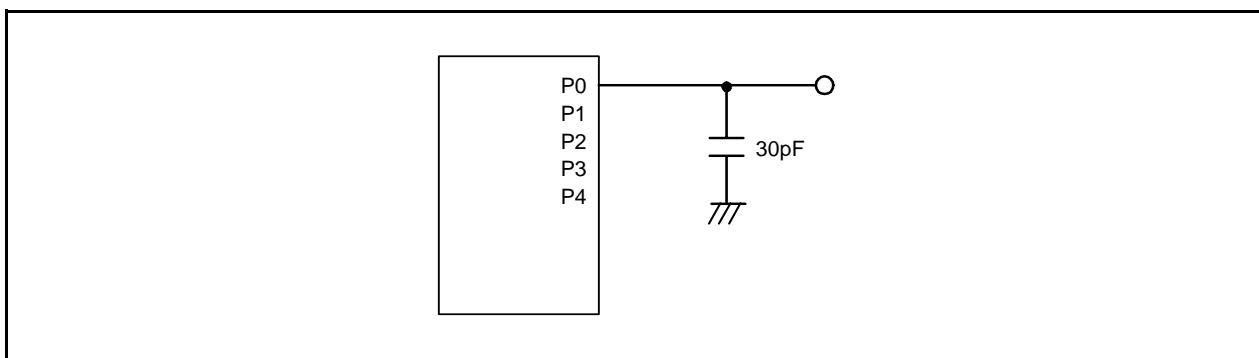**Figure 5.1   Ports P0 to P4 Timing Measurement Circuit**

Table 5.3   A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		Vref = AVcc		–	–	10	Bit
–	Absolute accuracy	10-bit mode	Vref = AVcc = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	–		±3	LSB
			Vref = AVcc = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±5	LSB
			Vref = AVcc = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±5	LSB
			Vref = AVcc = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±5	LSB
		8-bit mode	Vref = AVcc = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
			Vref = AVcc = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
			Vref = AVcc = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
			Vref = AVcc = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
ϕAD	A/D conversion clock		$4.0 \leq$ Vref = AVcc ≤ 5.5 V [2]		2	–	20	MHz
			$3.2 \leq$ Vref = AVcc ≤ 5.5 V [2]		2	–	16	MHz
			$2.7 \leq$ Vref = AVcc ≤ 5.5 V [2]		2	–	10	MHz
			$2.2 \leq$ Vref = AVcc ≤ 5.5 V [2]		2	–	5	MHz
–	Tolerance level impedance				–	3	–	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	–	–	μs
		8-bit mode	Vref = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	–	–	μs
tSAMP	Sampling time		ϕAD = 20 MHz		0.8	–	–	μs
IVref	Vref current		Vcc = 5 V, XIN = f1 = ϕAD = 20 MHz		–	45	–	μA
Vref	Reference voltage				2.2	–	AVcc	V
VIA	Analog input voltage [3]				0	–	Vref	V
OCVREF	On-chip reference voltage		2 MHz $\leq \phi$AD $\leq$ 4 MHz		1.19	1.34	1.49	V

Notes:
1. Vcc/AVcc = Vref = 2.2 to 5.5 V, Vss = 0 V and Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.6   Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance [2]		1,000 [3]	–	–	times
–	Byte program time		–	80	500	μs
–	Block erase time		–	0.3	–	s
t$_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	5+CPU clock × 3 cycles	ms
–	Interval from erase start/restart until following suspend request		0	–	–	μs
–	Time from suspend until erase restart		–	–	30+CPU clock × 1 cycle	μs
t$_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30+CPU clock × 1 cycle	μs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time [7]	Ambient temperature = 55°C	20	–	–	year

Notes:
1. V_{CC} = 2.7 to 5.5 V and T$_{opr}$ = 0 to 60°C, unless otherwise specified.
2.   Definition of programming/erasure endurance
     The programming and erasure endurance is defined on a per-block basis.
     If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
     However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3.   Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4.   In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5.   If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6.   Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7.   The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.10   Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard Min.	Standard Typ.	Standard Max.	Unit
Vdet2	Voltage detection level Vdet2_0	At the falling of Vcc	3.70	4.00	4.30	V
−	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		−	0.10	−	V
−	Voltage detection 2 circuit response time [2]	At the falling of Vcc from 5 V to (Vdet2_0 − 0.1) V	−	20	150	μs
−	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	−	1.7	−	μA
td(E-A)	Waiting time until voltage detection circuit operation starts [3]		−	−	100	μs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.11   Power-on Reset Circuit [2]

Symbol	Parameter	Condition	Standard Min.	Standard Typ.	Standard Max.	Unit
trth	External power Vcc rise gradient	[1]	0	−	50,000	mV/msec

Notes:
1. The measurement condition is T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

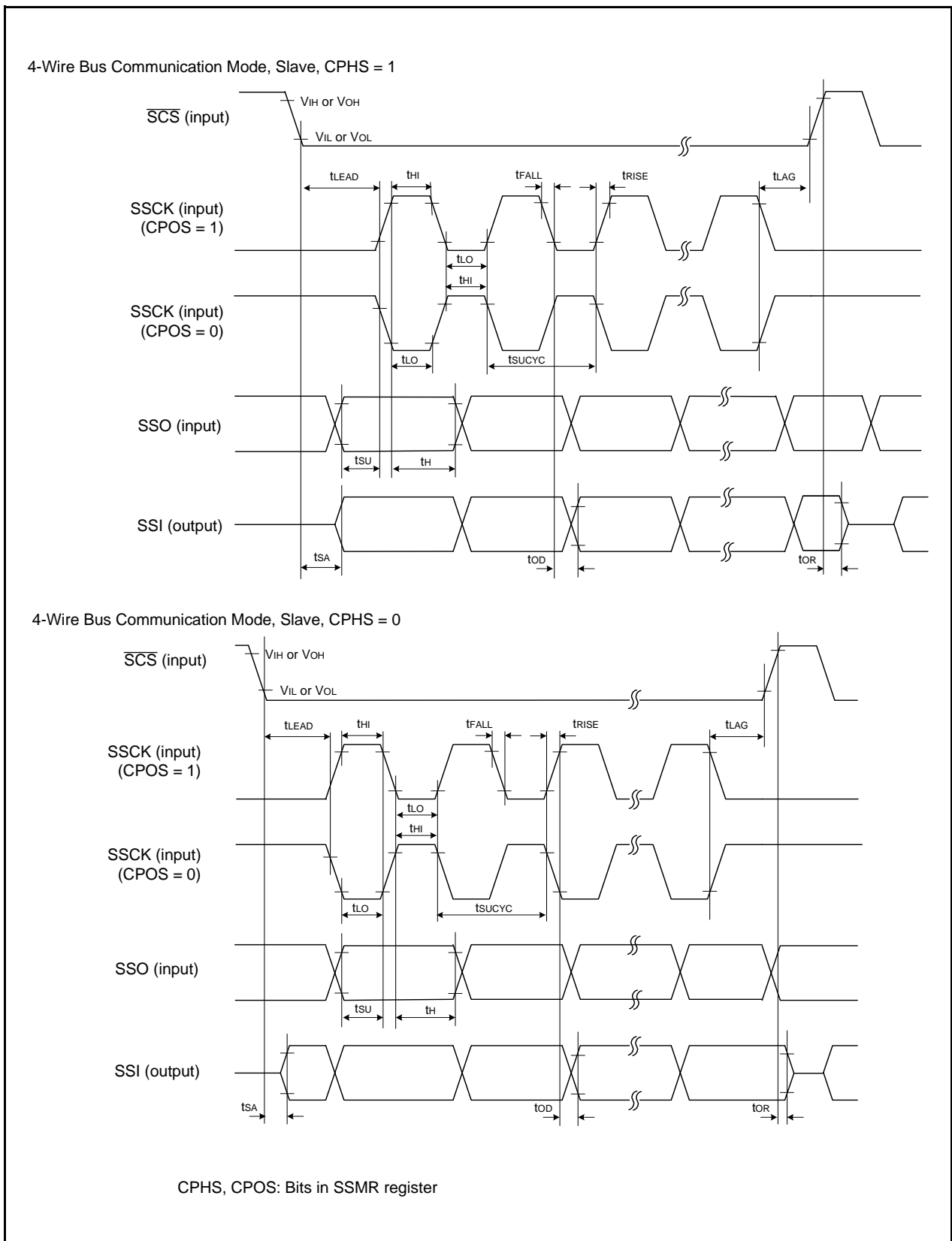**Figure 5.3   Power-on Reset Circuit Electrical Characteristics**

Figure 5.5   I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

Table 5.27   Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{W(CKH)}$	CLKi input "H" width	150	–	ns
$t_{W(CKL)}$	CLKi Input "L" width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 to 2

Figure 5.14   Serial Interface Timing Diagram when VCC = 3 V

Table 5.28   External Interrupt INTi (i = 0, 1, 3) Input, Key Input Interrupt KIi (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	INTi input "H" width, KIi input "H" width	380 [1]	–	ns
$t_{W(INL)}$	INTi input "L" width, KIi input "L" width	380 [2]	–	ns

Notes:
1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
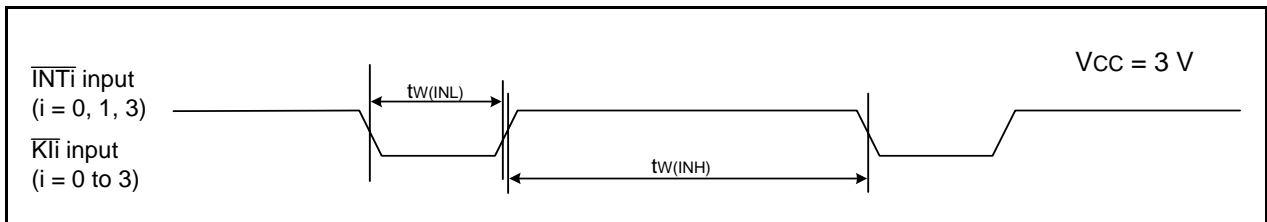

Figure 5.15   Input Timing Diagram for External Interrupt INTi and Key Input Interrupt KIi when Vcc = 3 V

Table 5.29   Electrical Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]

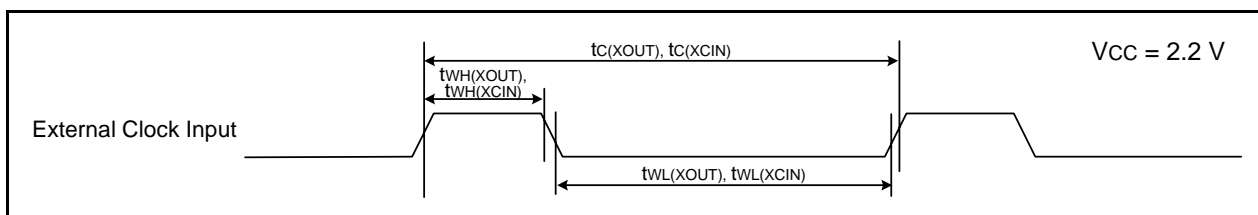| Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output "H" voltage	Other than XOUT	Drive capacity High	IOH = −2 mA	Vcc − 0.5	–	Vcc	V
			Drive capacity Low	IOH = −1 mA	Vcc − 0.5	–	Vcc	V
		XOUT		IOH = −200 µA	1.0	–	Vcc	V
VOL	Output "L" voltage	Other than XOUT	Drive capacity High	IOL = 2 mA	–	–	0.5	V
			Drive capacity Low	IOL = 1 mA	–	–	0.5	V
		XOUT		IOL = 200 µA	–	–	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.05	0.20	–	V
		RESET			0.05	0.2	–	V
IIH	Input "H" current		VI = 2.2 V, Vcc = 2.2 V		–	–	4.0	µA
IIL	Input "L" current		VI = 0 V, Vcc = 2.2 V		–	–	−4.0	µA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 2.2 V		70	140	300	kΩ
RfXIN	Feedback resistance	XIN			–	0.3	–	MΩ
RfXCIN	Feedback resistance	XCIN			–	8	–	MΩ
VRAM	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. 1.8 V ≤ Vcc < 2.7 V and Topr = −20 to 85°C (N version) / −40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

Table 5.30   Electrical Characteristics (6) [1.8 V ≤ Vcc < 2.7 V]
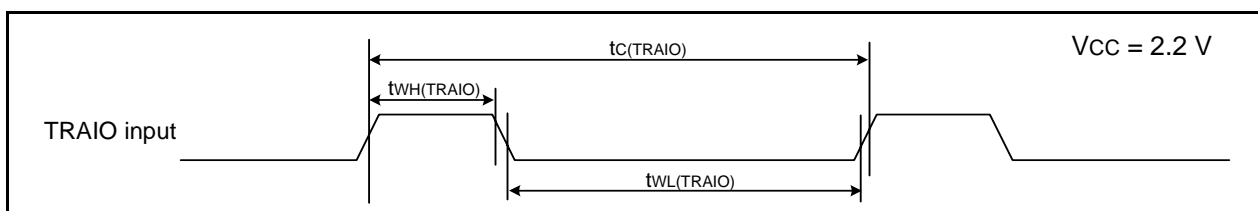**(Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)**

Symbol	Parameter	Condition			Standard			Unit
					Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 1.8 to 2.7 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode		XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	−	2.2	−	mA
				XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	0.8	−	mA
		High-speed on-chip oscillator mode		XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	−	2.5	10	mA
				XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	1.7	−	mA
				XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	−	1	−	mA
		Low-speed on-chip oscillator mode		XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	−	90	300	μA
		Low-speed clock mode		XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	−	80	350	μA
				XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	−	40	−	μA
		Wait mode		XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	−	15	90	μA
				XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	−	4	80	μA
				XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	−	3.5	−	μA
		Stop mode		XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	−	2.0	5	μA
				XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	−	5.0	−	μA

Timing requirements
(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C)

Table 5.31   External Clock Input (XOUT, XCIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(XOUT)}$	XOUT input cycle time	200	–	ns
$t_{WH(XOUT)}$	XOUT input "H" width	90	–	ns
$t_{WL(XOUT)}$	XOUT input "L" width	90	–	ns
$t_{C(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input "H" width	7	–	μs
$t_{WL(XCIN)}$	XCIN input "L" width	7	–	μs

Figure 5.16   External Clock Input Timing Diagram when Vcc = 2.2 V

Table 5.32   TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TRAIO)}$	TRAIO input cycle time	500	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	200	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	200	–	ns

Figure 5.17   TRAIO Input Timing Diagram when Vcc = 2.2 V