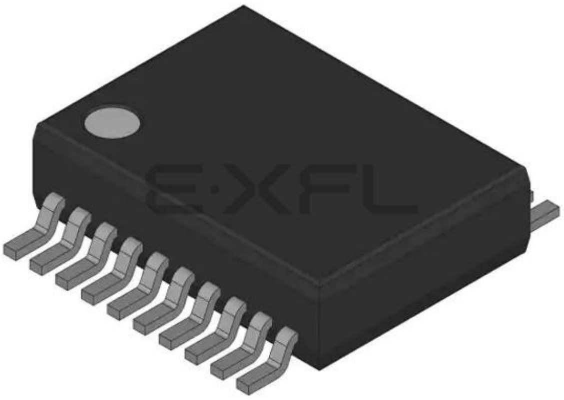
# Renesas Electronics America Inc - R5F21332CNFP#V2 Datasheet



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## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | I²C, LINbus, SIO, SSU, UART/USART |
| Peripherals | POR, PWM, Voltage Detect, WDT |
| Number of I/O | 27 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 12x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21332cnfp-v2 |

### 1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/33C Group.

**Table 1.1 Specifications for R8C/33C Group (1)**

| Item | Function | Specification |
|---|---|---|
| CPU | Central processing unit | R8C CPU core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)<br>200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operation mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM, Data flash | Refer to **Table 1.3 Product List for R8C/33C Group**. |
| Power Supply Voltage Detection | Voltage detection circuit | • Power-on reset<br>• Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable) |
| I/O Ports | Programmable I/O ports | • Input-only: 1 pin<br>• CMOS I/O ports: 27, selectable pull-up resistor<br>• High current drive ports: 27 |
| Clock | Clock generation circuits | 4 circuits: XIN clock oscillation circuit,<br>XCIN clock oscillation circuit (32 kHz),<br>High-speed on-chip oscillator (with frequency adjustment function),<br>Low-speed on-chip oscillator<br>• Oscillation stop detection: XIN clock oscillation stop detection function<br>• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16<br>• Low power consumption modes:<br>Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode |
| | | Real-time clock (timer RE) |
| Interrupts | | • Number of interrupt vectors: 69<br>• External Interrupt: 7 ($\overline{\text{INT}}$ × 3, Key input × 4)<br>• Priority levels: 7 levels |
| Watchdog Timer | | • 14 bits × 1 (with prescaler)<br>• Reset start selectable<br>• Low-speed on-chip oscillator for watchdog timer selectable |
| DTC (Data Transfer Controller) | | • 1 channel<br>• Activation sources: 23<br>• Transfer modes: 2 (normal mode, repeat mode) |
| Timer | Timer RA | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits × 1 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RE | 8 bits × 1<br>Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode |

## 1.2 Product List

Table 1.3 lists Product List for R8C/33C Group, and Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/33C Group.

**Table 1.3 Product List for R8C/33C Group** **Current of Aug 2010**

| Part No. | ROM Capacity | | RAM Capacity | Package Type | Remarks |
|---|---|---|---|---|---|
| | Program ROM | Data flash | | | |
| R5F21331CNFP | 4 Kbytes | 1 Kbyte × 4 | 512 bytes | PLQP0032GB-A | N version |
| R5F21332CNFP | 8 Kbytes | 1 Kbyte × 4 | 1 Kbyte | PLQP0032GB-A | |
| R5F21334CNFP | 16 Kbytes | 1 Kbyte × 4 | 1.5 Kbytes | PLQP0032GB-A | |
| R5F21335CNFP | 24 Kbytes | 1 Kbyte × 4 | 2 Kbytes | PLQP0032GB-A | |
| R5F21336CNFP | 32 Kbytes | 1 Kbyte × 4 | 2.5 Kbytes | PLQP0032GB-A | |
| R5F21331CDFP | 4 Kbytes | 1 Kbyte × 4 | 512 bytes | PLQP0032GB-A | D version |
| R5F21332CDFP | 8 Kbytes | 1 Kbyte × 4 | 1 Kbyte | PLQP0032GB-A | |
| R5F21334CDFP | 16 Kbytes | 1 Kbyte × 4 | 1.5 Kbytes | PLQP0032GB-A | |
| R5F21335CDFP | 24 Kbytes | 1 Kbyte × 4 | 2 Kbytes | PLQP0032GB-A | |
| R5F21336CDFP | 32 Kbytes | 1 Kbyte × 4 | 2.5 Kbytes | PLQP0032GB-A | |

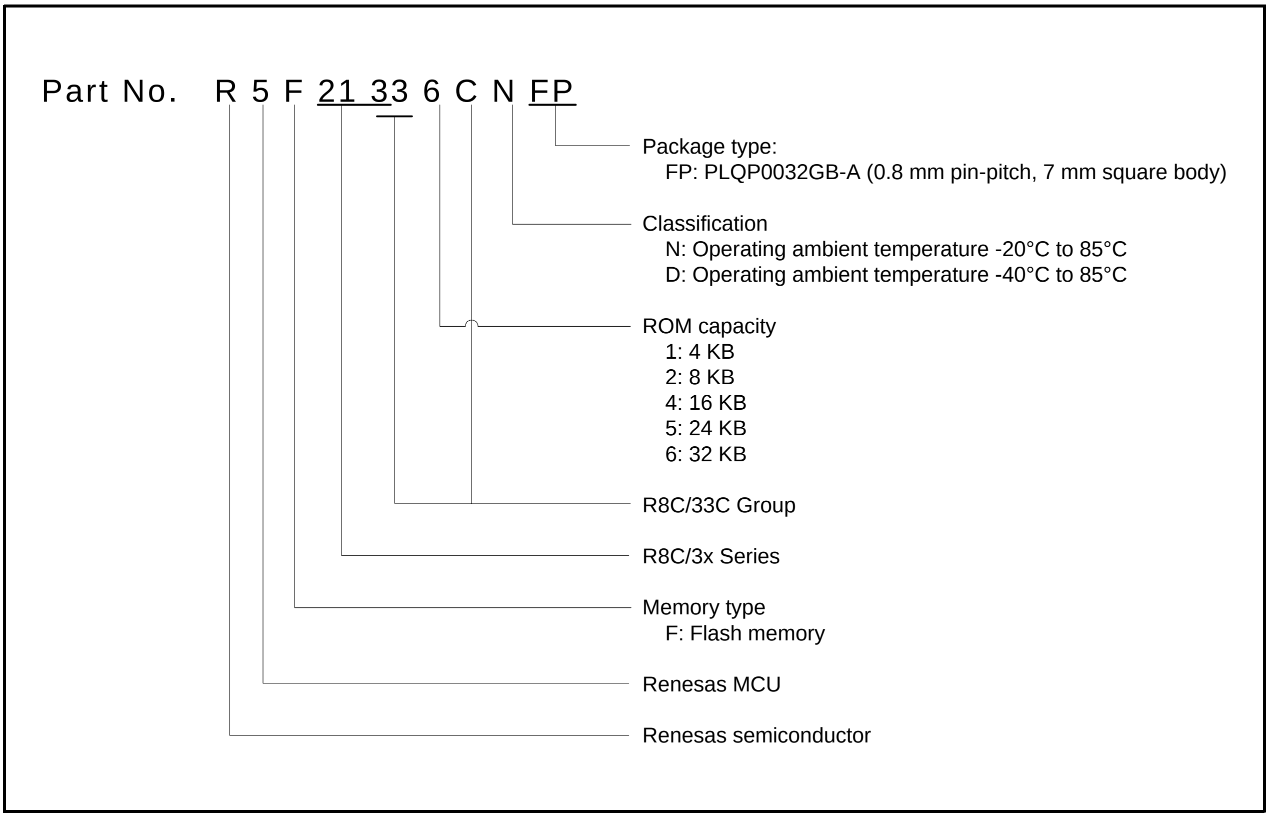
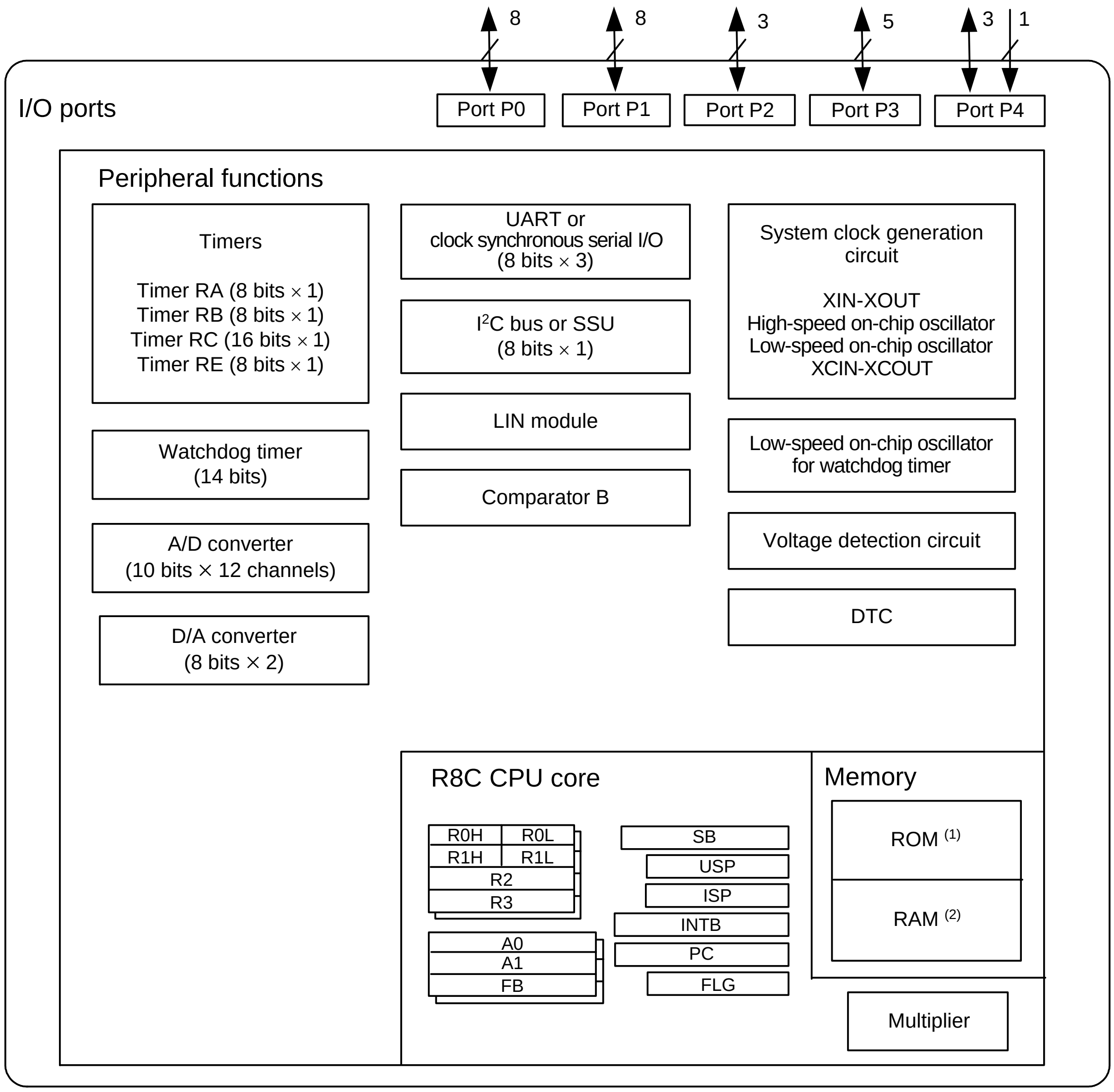


**Figure 1.1 Part Number, Memory Size, and Package of R8C/33C Group**

## 1.3 Block Diagram

Figure 1.2 shows a Block Diagram.

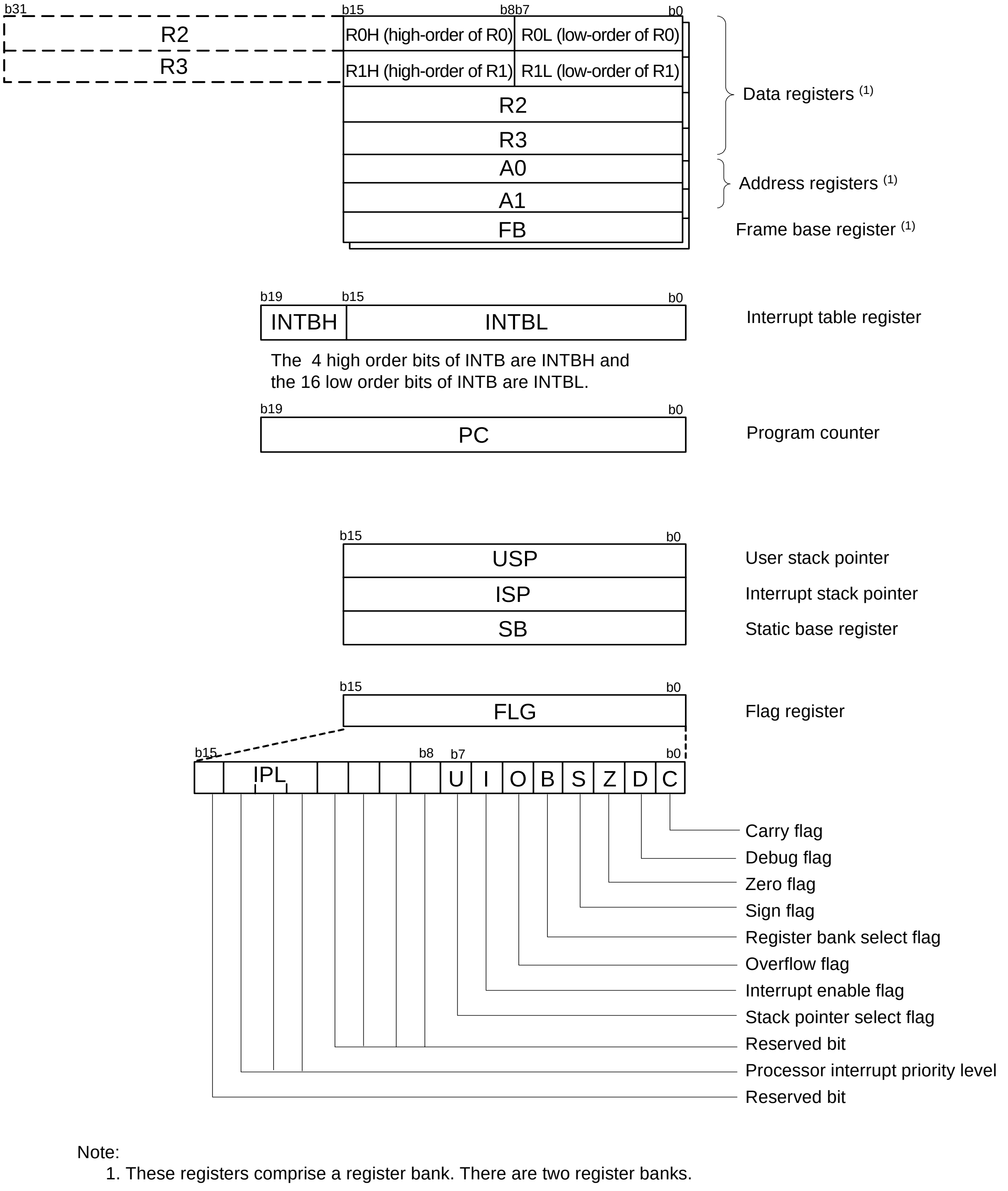


Notes:
1. ROM size varies with MCU type.
2. RAM size varies with MCU type.

**Figure 1.2 Block Diagram**

# 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



Note:
1. These registers comprise a register bank. There are two register banks.

**Figure 2.1 CPU Registers**

## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

## Table 4.8 SFR Information (8) (1)

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 01C0h | Address Match Interrupt Register 0 | RMAD0 | XXh |
| 01C1h | | | XXh |
| 01C2h | | | 0000XXXXb |
| 01C3h | Address Match Interrupt Enable Register 0 | AIER0 | 00h |
| 01C4h | Address Match Interrupt Register 1 | RMAD1 | XXh |
| 01C5h | | | XXh |
| 01C6h | | | 0000XXXXb |
| 01C7h | Address Match Interrupt Enable Register 1 | AIER1 | 00h |
| 01C8h | | | |
| 01C9h | | | |
| 01CAh | | | |
| 01CBh | | | |
| 01CCh | | | |
| 01CDh | | | |
| 01CEh | | | |
| 01CFh | | | |
| 01D0h | | | |
| 01D1h | | | |
| 01D2h | | | |
| 01D3h | | | |
| 01D4h | | | |
| 01D5h | | | |
| 01D6h | | | |
| 01D7h | | | |
| 01D8h | | | |
| 01D9h | | | |
| 01DAh | | | |
| 01DBh | | | |
| 01DCh | | | |
| 01DDh | | | |
| 01DEh | | | |
| 01DFh | | | |
| 01E0h | Pull-Up Control Register 0 | PUR0 | 00h |
| 01E1h | Pull-Up Control Register 1 | PUR1 | 00h |
| 01E2h | | | |
| 01E3h | | | |
| 01E4h | | | |
| 01E5h | | | |
| 01E6h | | | |
| 01E7h | | | |
| 01E8h | | | |
| 01E9h | | | |
| 01EAh | | | |
| 01EBh | | | |
| 01ECh | | | |
| 01EDh | | | |
| 01EEh | | | |
| 01EFh | | | |
| 01F0h | Port P1 Drive Capacity Control Register | P1DRR | 00h |
| 01F1h | Port P2 Drive Capacity Control Register | P2DRR | 00h |
| 01F2h | Drive Capacity Control Register 0 | DRR0 | 00h |
| 01F3h | Drive Capacity Control Register 1 | DRR1 | 00h |
| 01F4h | | | |
| 01F5h | Input Threshold Control Register 0 | VLT0 | 00h |
| 01F6h | Input Threshold Control Register 1 | VLT1 | 00h |
| 01F7h | | | |
| 01F8h | Comparator B Control Register 0 | INTCMP | 00h |
| 01F9h | | | |
| 01FAh | External Input Enable Register 0 | INTEN | 00h |
| 01FBh | | | |
| 01FCh | INT Input Filter Select Register 0 | INTF | 00h |
| 01FDh | | | |
| 01FEh | Key Input Enable Register 0 | KIEN | 00h |
| 01FFh | | | |

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

### Table 4.9 SFR Information (9) (1)

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 2C00h | DTC Transfer Vector Area | | XXh |
| 2C01h | DTC Transfer Vector Area | | XXh |
| 2C02h | DTC Transfer Vector Area | | XXh |
| 2C03h | DTC Transfer Vector Area | | XXh |
| 2C04h | DTC Transfer Vector Area | | XXh |
| 2C05h | DTC Transfer Vector Area | | XXh |
| 2C06h | DTC Transfer Vector Area | | XXh |
| 2C07h | DTC Transfer Vector Area | | XXh |
| 2C08h | DTC Transfer Vector Area | | XXh |
| 2C09h | DTC Transfer Vector Area | | XXh |
| 2C0Ah | DTC Transfer Vector Area | | XXh |
| : | DTC Transfer Vector Area | | XXh |
| : | DTC Transfer Vector Area | | XXh |
| 2C3Ah | DTC Transfer Vector Area | | XXh |
| 2C3Bh | DTC Transfer Vector Area | | XXh |
| 2C3Ch | DTC Transfer Vector Area | | XXh |
| 2C3Dh | DTC Transfer Vector Area | | XXh |
| 2C3Eh | DTC Transfer Vector Area | | XXh |
| 2C3Fh | DTC Transfer Vector Area | | XXh |
| 2C40h | DTC Control Data 0 | DTCD0 | XXh |
| 2C41h | | | XXh |
| 2C42h | | | XXh |
| 2C43h | | | XXh |
| 2C44h | | | XXh |
| 2C45h | | | XXh |
| 2C46h | | | XXh |
| 2C47h | | | XXh |
| 2C48h | DTC Control Data 1 | DTCD1 | XXh |
| 2C49h | | | XXh |
| 2C4Ah | | | XXh |
| 2C4Bh | | | XXh |
| 2C4Ch | | | XXh |
| 2C4Dh | | | XXh |
| 2C4Eh | | | XXh |
| 2C4Fh | | | XXh |
| 2C50h | DTC Control Data 2 | DTCD2 | XXh |
| 2C51h | | | XXh |
| 2C52h | | | XXh |
| 2C53h | | | XXh |
| 2C54h | | | XXh |
| 2C55h | | | XXh |
| 2C56h | | | XXh |
| 2C57h | | | XXh |
| 2C58h | DTC Control Data 3 | DTCD3 | XXh |
| 2C59h | | | XXh |
| 2C5Ah | | | XXh |
| 2C5Bh | | | XXh |
| 2C5Ch | | | XXh |
| 2C5Dh | | | XXh |
| 2C5Eh | | | XXh |
| 2C5Fh | | | XXh |
| 2C60h | DTC Control Data 4 | DTCD4 | XXh |
| 2C61h | | | XXh |
| 2C62h | | | XXh |
| 2C63h | | | XXh |
| 2C64h | | | XXh |
| 2C65h | | | XXh |
| 2C66h | | | XXh |
| 2C67h | | | XXh |
| 2C68h | DTC Control Data 5 | DTCD5 | XXh |
| 2C69h | | | XXh |
| 2C6Ah | | | XXh |
| 2C6Bh | | | XXh |
| 2C6Ch | | | XXh |
| 2C6Dh | | | XXh |
| 2C6Eh | | | XXh |
| 2C6Fh | | | XXh |

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

**Table 4.11 SFR Information (11) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 2CB0h | DTC Control Data 14 | DTCD14 | XXh |
| 2CB1h | | | XXh |
| 2CB2h | | | XXh |
| 2CB3h | | | XXh |
| 2CB4h | | | XXh |
| 2CB5h | | | XXh |
| 2CB6h | | | XXh |
| 2CB7h | | | XXh |
| 2CB8h | DTC Control Data 15 | DTCD15 | XXh |
| 2CB9h | | | XXh |
| 2CBAh | | | XXh |
| 2CBBh | | | XXh |
| 2CBCh | | | XXh |
| 2CBDh | | | XXh |
| 2CBEh | | | XXh |
| 2CBFh | | | XXh |
| 2CC0h | DTC Control Data 16 | DTCD16 | XXh |
| 2CC1h | | | XXh |
| 2CC2h | | | XXh |
| 2CC3h | | | XXh |
| 2CC4h | | | XXh |
| 2CC5h | | | XXh |
| 2CC6h | | | XXh |
| 2CC7h | | | XXh |
| 2CC8h | DTC Control Data 17 | DTCD17 | XXh |
| 2CC9h | | | XXh |
| 2CCAh | | | XXh |
| 2CCBh | | | XXh |
| 2CCCh | | | XXh |
| 2CCDh | | | XXh |
| 2CCEh | | | XXh |
| 2CCFh | | | XXh |
| 2CD0h | DTC Control Data 18 | DTCD18 | XXh |
| 2CD1h | | | XXh |
| 2CD2h | | | XXh |
| 2CD3h | | | XXh |
| 2CD4h | | | XXh |
| 2CD5h | | | XXh |
| 2CD6h | | | XXh |
| 2CD7h | | | XXh |
| 2CD8h | DTC Control Data 19 | DTCD19 | XXh |
| 2CD9h | | | XXh |
| 2CDAh | | | XXh |
| 2CDBh | | | XXh |
| 2CDCh | | | XXh |
| 2CDDh | | | XXh |
| 2CDEh | | | XXh |
| 2CDFh | | | XXh |
| 2CE0h | DTC Control Data 20 | DTCD20 | XXh |
| 2CE1h | | | XXh |
| 2CE2h | | | XXh |
| 2CE3h | | | XXh |
| 2CE4h | | | XXh |
| 2CE5h | | | XXh |
| 2CE6h | | | XXh |
| 2CE7h | | | XXh |
| 2CE8h | DTC Control Data 21 | DTCD21 | XXh |
| 2CE9h | | | XXh |
| 2CEAh | | | XXh |
| 2CEBh | | | XXh |
| 2CECh | | | XXh |
| 2CEDh | | | XXh |
| 2CEEh | | | XXh |
| 2CEFh | | | XXh |

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

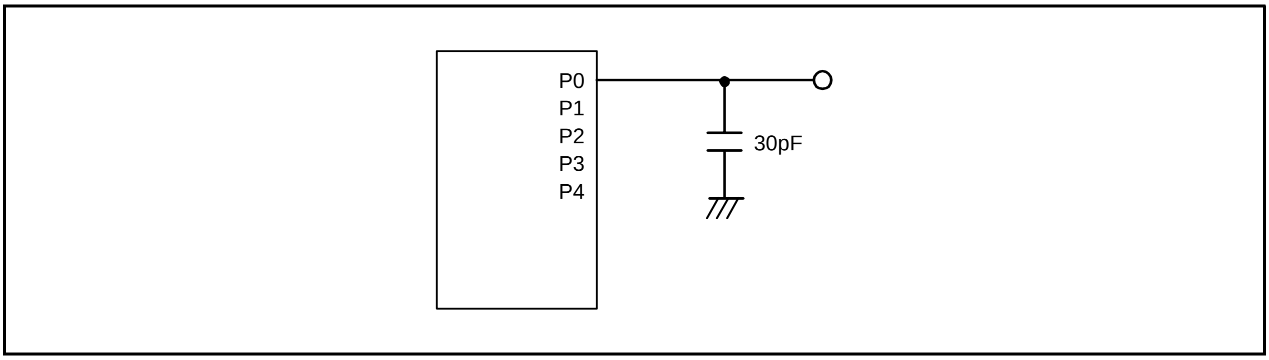


**Figure 5.1** Ports P0 to P4 Timing Measurement Circuit

### Table 5.4 D/A Converter Characteristics

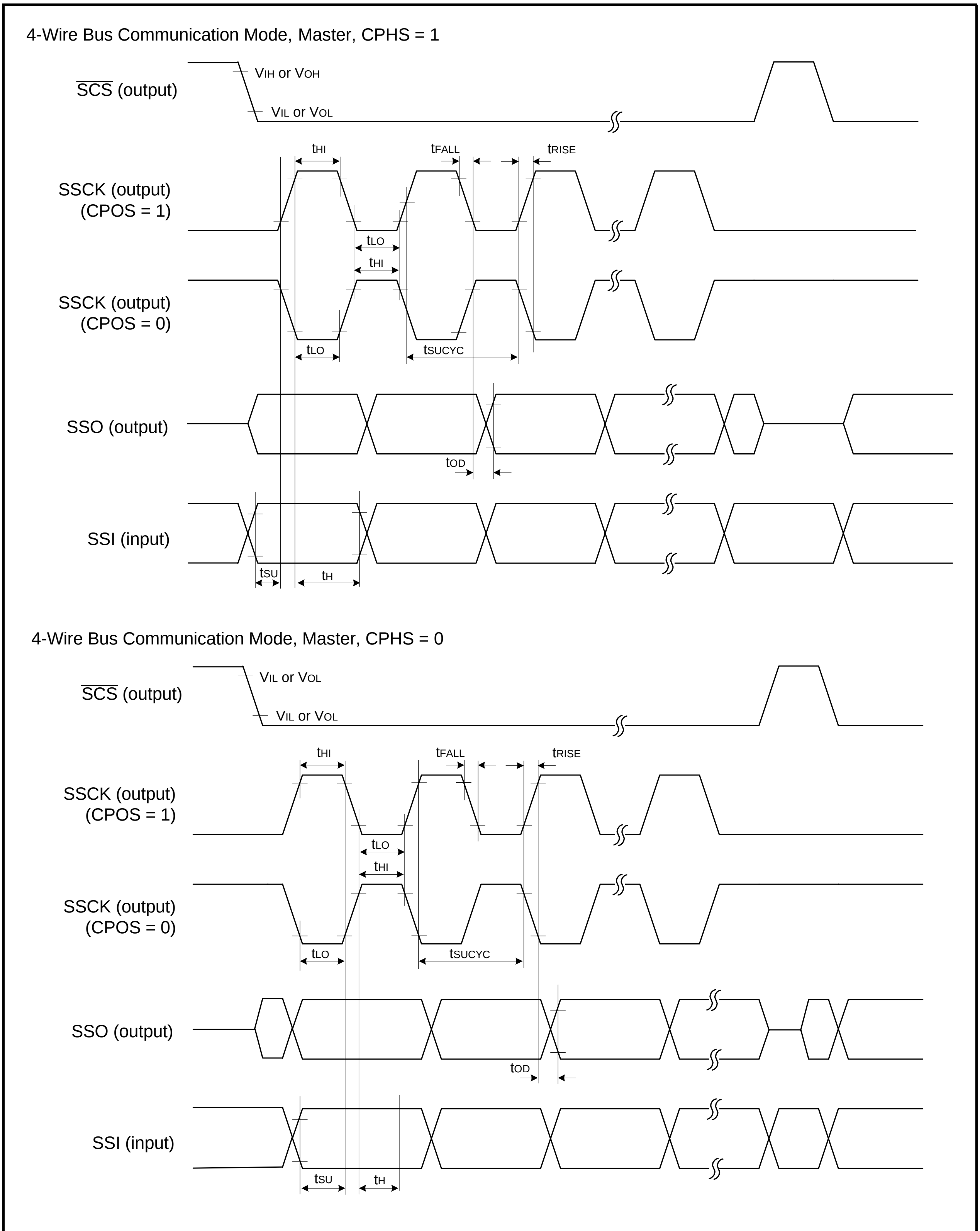
| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | – | – | 8 | Bit |
| – | Absolute accuracy | | – | – | 2.5 | LSB |
| $t_{su}$ | Setup time | | – | – | 3 | µs |
| $R_O$ | Output resistor | | – | 6 | – | kΩ |
| $I_{Vref}$ | Reference power input current | (Note 2) | – | – | 1.5 | mA |

Notes:
1. $V_{CC}/AV_{CC} = V_{ref}$ = 2.7 to 5.5 V and $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. This applies when one D/A converter is used and the value of the DAi register (i = 0 or 1) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included.

### Table 5.5 Comparator B Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Vref | IVREF1, IVREF3 input reference voltage | | 0 | – | $V_{CC} - 1.4$ | V |
| $V_I$ | IVCMP1, IVCMP3 input voltage | | –0.3 | – | $V_{CC} + 0.3$ | V |
| – | Offset | | – | 5 | 100 | mV |
| $t_d$ | Comparator output delay time (2) | $V_I$ = Vref ± 100 mV | – | 0.1 | – | µs |
| $I_{CMP}$ | Comparator operating current | $V_{CC}$ = 5.0 V | – | 17.5 | – | µA |

Notes:
1. $V_{CC}$ = 2.7 to 5.5 V, $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. When the digital filter is disabled.



CPHS, CPOS: Bits in SSMR register

**Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)**

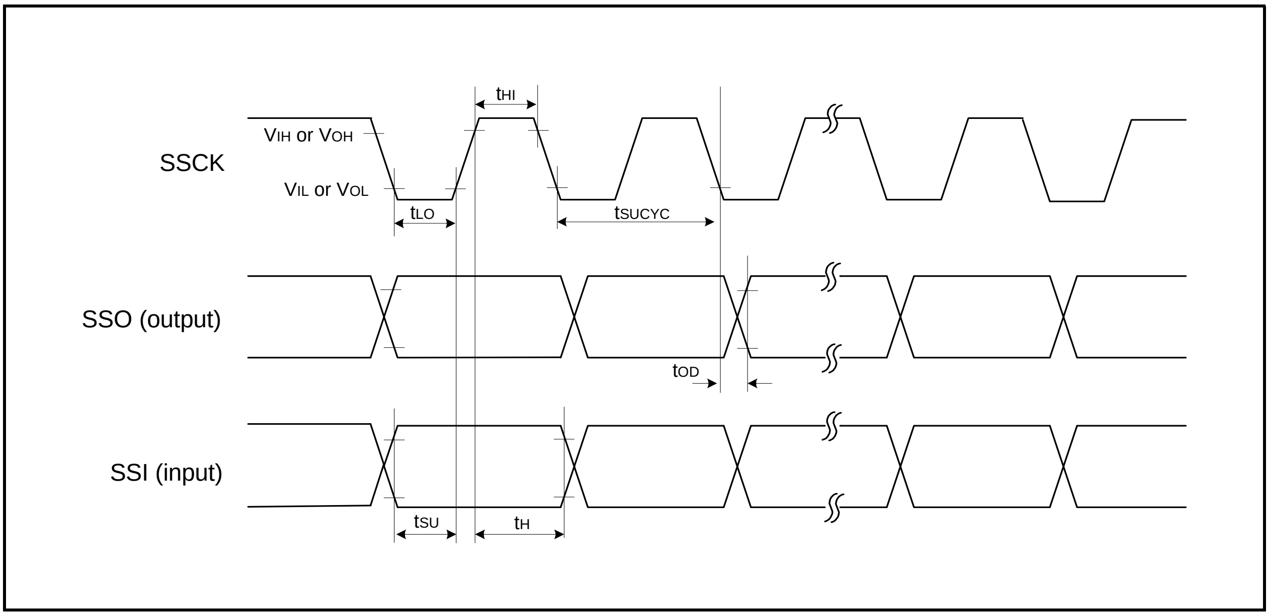


**Figure 5.6** I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

### Table 5.17 Electrical Characteristics (1) [$4.2 \text{ V} \le V_{CC} \le 5.5 \text{ V}$]

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | Other than XOUT | Drive capacity High $V_{CC}$ = 5 V | $I_{OH}$ = –20 mA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | | Drive capacity Low $V_{CC}$ = 5 V | $I_{OH}$ = –5 mA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | XOUT | $V_{CC}$ = 5 V | $I_{OH}$ = –200 µA | 1.0 | – | $V_{CC}$ | V |
| $V_{OL}$ | Output “L” voltage | Other than XOUT | Drive capacity High $V_{CC}$ = 5 V | $I_{OL}$ = 20 mA | – | – | 2.0 | V |
| | | | Drive capacity Low $V_{CC}$ = 5 V | $I_{OL}$ = 5 mA | – | – | 2.0 | V |
| | | XOUT | $V_{CC}$ = 5 V | $I_{OL}$ = 200 µA | – | – | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$, $\overline{\text{KI0}}$, $\overline{\text{KI1}}$, $\overline{\text{KI2}}$, $\overline{\text{KI3}}$, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, $\overline{\text{TRCTRG}}$, TRCCLK, $\overline{\text{ADTRG}}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO | | | 0.1 | 1.2 | – | V |
| | | $\overline{\text{RESET}}$ | | | 0.1 | 1.2 | – | V |
| $I_{IH}$ | Input “H” current | | VI = 5 V, $V_{CC}$ = 5.0 V | | – | – | 5.0 | µA |
| $I_{IL}$ | Input “L” current | | VI = 0 V, $V_{CC}$ = 5.0 V | | – | – | –5.0 | µA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V, $V_{CC}$ = 5.0 V | | 25 | 50 | 100 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 0.3 | – | MΩ |
| $R_{fXCIN}$ | Feedback resistance | XCIN | | | – | 8 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

Note:

1. $4.2 \text{ V} \le V_{CC} \le 5.5 \text{ V}$ and $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

## Timing Requirements
## (Unless Otherwise Specified: $V_{CC}$ = 5 V, $V_{SS}$ = 0 V at Topr = 25°C)

### Table 5.19 External Clock Input (XOUT, XCIN)

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XOUT)}$ | XOUT input cycle time | 50 | – | ns |
| $t_{WH(XOUT)}$ | XOUT input “H” width | 24 | – | ns |
| $t_{WL(XOUT)}$ | XOUT input “L” width | 24 | – | ns |
| $t_{c(XCIN)}$ | XCIN input cycle time | 14 | – | µs |
| $t_{WH(XCIN)}$ | XCIN input “H” width | 7 | – | µs |
| $t_{WL(XCIN)}$ | XCIN input “L” width | 7 | – | µs |

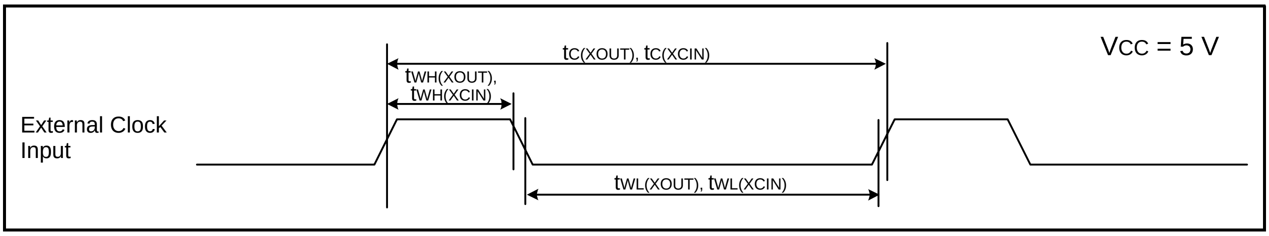


Figure 5.8 External Clock Input Timing Diagram when $V_{CC}$ = 5 V

### Table 5.20 TRAIO Input

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 100 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width | 40 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width | 40 | – | ns |

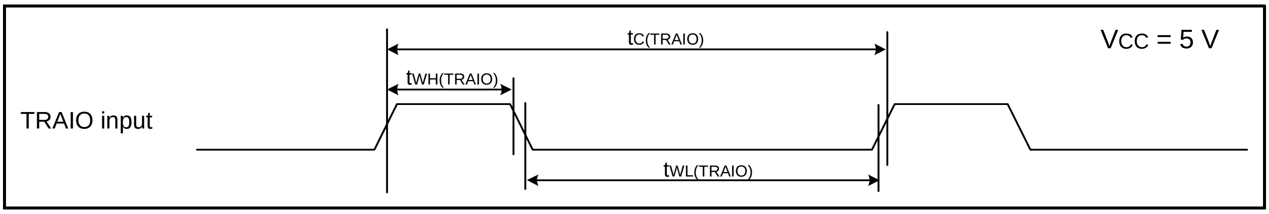


Figure 5.9 TRAIO Input Timing Diagram when $V_{CC}$ = 5 V

### Table 5.23 Electrical Characteristics (3) [2.7 V ≤ Vcc < 4.2 V]

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output "H" voltage | Other than XOUT | Drive capacity High | $I_{OH}$ = –5 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | | Drive capacity Low | $I_{OH}$ = –1 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | XOUT | | $I_{OH}$ = –200 µA | 1.0 | – | $V_{CC}$ | V |
| $V_{OL}$ | Output "L" voltage | Other than XOUT | Drive capacity High | $I_{OL}$ = 5 mA | – | – | 0.5 | V |
| | | | Drive capacity Low | $I_{OL}$ = 1 mA | – | – | 0.5 | V |
| | | XOUT | | $I_{OL}$ = 200 µA | – | – | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$, $\overline{\text{KI0}}$, $\overline{\text{KI1}}$, $\overline{\text{KI2}}$, $\overline{\text{KI3}}$, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, $\overline{\text{ADTRG}}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO | $V_{CC}$ = 3.0 V | | 0.1 | 0.4 | – | V |
| | | $\overline{\text{RESET}}$ | $V_{CC}$ = 3.0 V | | 0.1 | 0.5 | – | V |
| $I_{IH}$ | Input "H" current | | VI = 3 V, $V_{CC}$ = 3.0 V | | – | – | 4.0 | µA |
| $I_{IL}$ | Input "L" current | | VI = 0 V, $V_{CC}$ = 3.0 V | | – | – | –4.0 | µA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V, $V_{CC}$ = 3.0 V | | 42 | 84 | 168 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 0.3 | – | MΩ |
| $R_{fXCIN}$ | Feedback resistance | XCIN | | | – | 8 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

Note:

1. 2.7 V ≤ $V_{CC}$ < 4.2 V and $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

**Table 5.24 Electrical Characteristics (4) [$2.7\ V \leq V_{CC} < 3.3\ V$]**
**($T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $I_{CC}$ | Power supply current ($V_{CC}$ = 2.7 to 3.3 V)<br>Single-chip mode, output pins are open, other pins are $V_{SS}$ | High-speed clock mode | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 3.5 | 10 | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1.5 | 7.5 | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 7.0 | 15 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 3.0 | – | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 4.0 | – | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1.5 | – | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 4 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-16<br>MSTIIC = MSTTRD = MSTTRC = 1 | – | 1 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR27 = 1, VCA20 = 0 | – | 90 | 390 | µA |
| | | Low-speed clock mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>FMR27 = 1, VCA20 = 0 | – | 80 | 400 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>Program operation on RAM<br>Flash memory off, FMSTP = 1, VCA20 = 0 | – | 40 | – | µA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1 | – | 15 | 90 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1 | – | 4 | 80 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (peripheral clock off)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1 | – | 3.5 | – | µA |
| | | Stop mode | XIN clock off, $T_{opr}$ = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 2.0 | 5.0 | µA |
| | | | XIN clock off, $T_{opr}$ = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 5.0 | – | µA |

## Timing requirements
## (Unless Otherwise Specified: $V_{CC}$ = 3 V, $V_{SS}$ = 0 V at Topr = 25°C)

**Table 5.25 External Clock Input (XOUT, XCIN)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XOUT)}$ | XOUT input cycle time | 50 | – | ns |
| $t_{WH(XOUT)}$ | XOUT input “H” width | 24 | – | ns |
| $t_{WL(XOUT)}$ | XOUT input “L” width | 24 | – | ns |
| $t_{c(XCIN)}$ | XCIN input cycle time | 14 | – | µs |
| $t_{WH(XCIN)}$ | XCIN input “H” width | 7 | – | µs |
| $t_{WL(XCIN)}$ | XCIN input “L” width | 7 | – | µs |

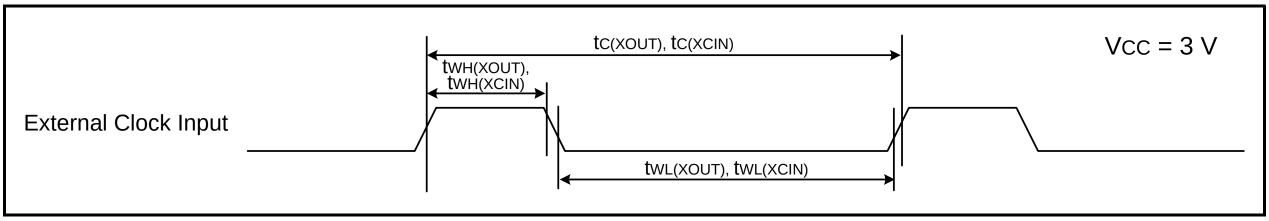


**Figure 5.12 External Clock Input Timing Diagram when $V_{CC}$ = 3 V**

**Table 5.26 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 300 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width | 120 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width | 120 | – | ns |

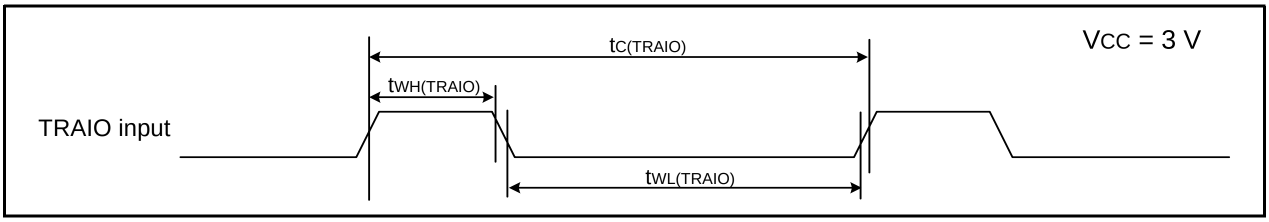


**Figure 5.13 TRAIO Input Timing Diagram when $V_{CC}$ = 3 V**

**Table 5.30 Electrical Characteristics (6) [1.8 V ≤ Vcc < 2.7 V]**
**($T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $I_{CC}$ | Power supply current ($V_{CC}$ = 1.8 to 2.7 V)<br>Single-chip mode, output pins are open, other pins are $V_{SS}$ | High-speed clock mode | XIN = 5 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 2.2 | – | mA |
| | | | XIN = 5 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 0.8 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 5 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 2.5 | 10 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 5 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1.7 | – | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 4 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-16<br>MSTIIC = MSTTRD = MSTTRC = 1 | – | 1 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR27 = 1, VCA20 = 0 | – | 90 | 300 | µA |
| | | Low-speed clock mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>FMR27 = 1, VCA20 = 0 | – | 80 | 350 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>Program operation on RAM<br>Flash memory off, FMSTP = 1, VCA20 = 0 | – | 40 | – | µA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 15 | 90 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 4 | 80 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (peripheral clock off)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 3.5 | – | µA |
| | | Stop mode | XIN clock off, $T_{opr}$ = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 2.0 | 5 | µA |
| | | | XIN clock off, $T_{opr}$ = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 5.0 | – | µA |

### Table 5.33 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 800 | – | ns |
| $t_{W(CKH)}$ | CLKi input “H” width | 400 | – | ns |
| $t_{W(CKL)}$ | CLKi input “L” width | 400 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 200 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 150 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0 to 2

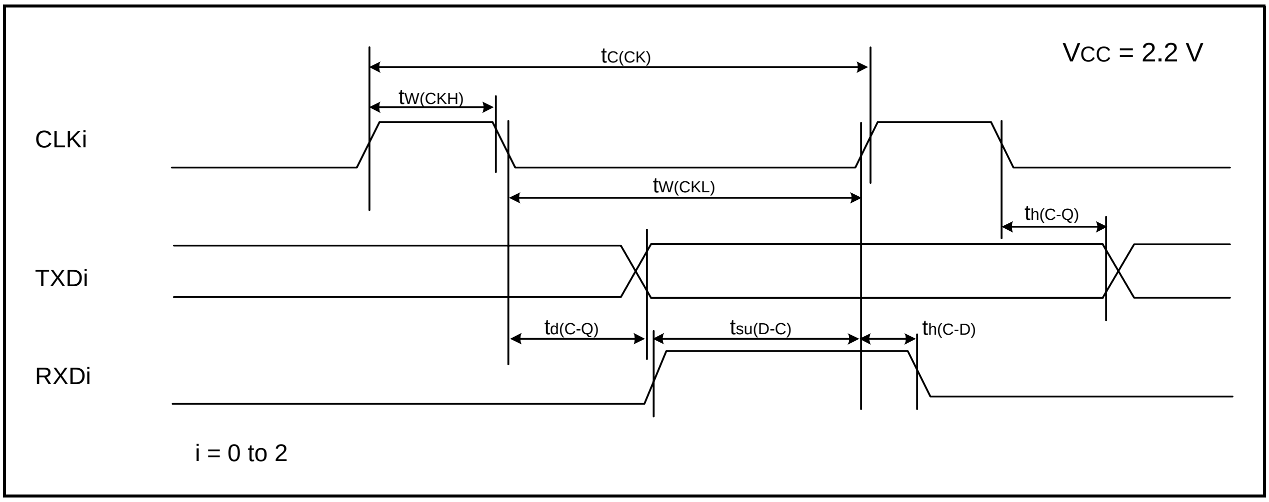


Figure 5.18 Serial Interface Timing Diagram when $V_{CC}$ = 2.2 V

### Table 5.34 External Interrupt $\overline{\text{INTi}}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{\text{KIi}}$ (i = 0 to 3)

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{W(INH)}$ | $\overline{\text{INTi}}$ input “H” width, $\overline{\text{KIi}}$ input “H” width | 1000 (1) | – | ns |
| $t_{W(INL)}$ | $\overline{\text{INTi}}$ input “L” width, $\overline{\text{KIi}}$ input “L” width | 1000 (2) | – | ns |

Notes:

1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

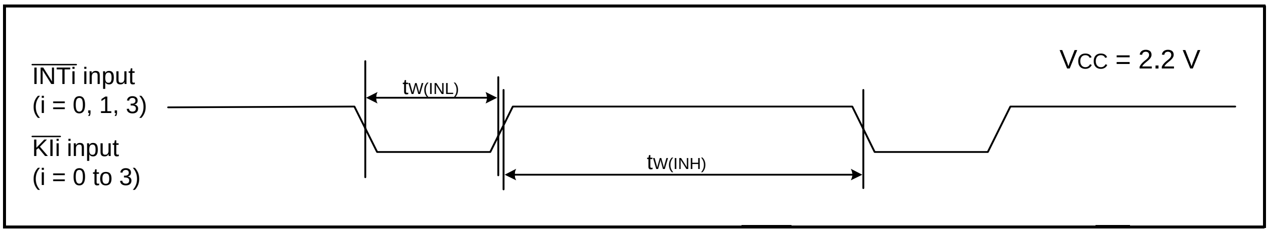


Figure 5.19 Input Timing Diagram for External Interrupt $\overline{\text{INTi}}$ and Key Input Interrupt $\overline{\text{KIi}}$ when Vcc = 2.2 V

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**Renesas Electronics America Inc.**
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

**Renesas Electronics Canada Limited**
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

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Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

**Renesas Electronics Europe GmbH**
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

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7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

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Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

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Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
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