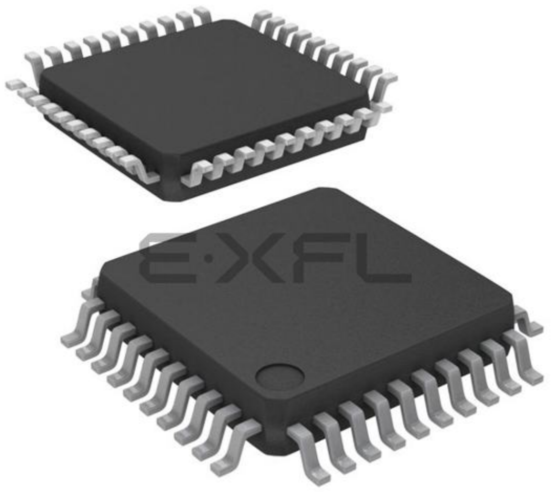

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	27
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21336cdfp-50

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/33C Group.

Table 1.1 Specifications for R8C/33C Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to **Table 1.3 Product List for R8C/33C Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• Input-only: 1 pin • CMOS I/O ports: 27, selectable pull-up resistor • High current drive ports: 27
Clock	Clock generation circuits	4 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit (32 kHz), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
		Real-time clock (timer RE)
Interrupts		• Number of interrupt vectors: 69 • External Interrupt: 7 ($\overline{INT}$ × 3, Key input × 4) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 23 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RE	8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode

1.2 Product List

Table 1.3 lists Product List for R8C/33C Group, and Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/33C Group.

Table 1.3 Product List for R8C/33C Group **Current of Aug 2010**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21331CNFP	4 Kbytes	1 Kbyte × 4	512 bytes	PLQP0032GB-A	N version
R5F21332CNFP	8 Kbytes	1 Kbyte × 4	1 Kbyte	PLQP0032GB-A	
R5F21334CNFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0032GB-A	
R5F21335CNFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0032GB-A	
R5F21336CNFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0032GB-A	
R5F21331CDFP	4 Kbytes	1 Kbyte × 4	512 bytes	PLQP0032GB-A	D version
R5F21332CDFP	8 Kbytes	1 Kbyte × 4	1 Kbyte	PLQP0032GB-A	
R5F21334CDFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0032GB-A	
R5F21335CDFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0032GB-A	
R5F21336CDFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0032GB-A	

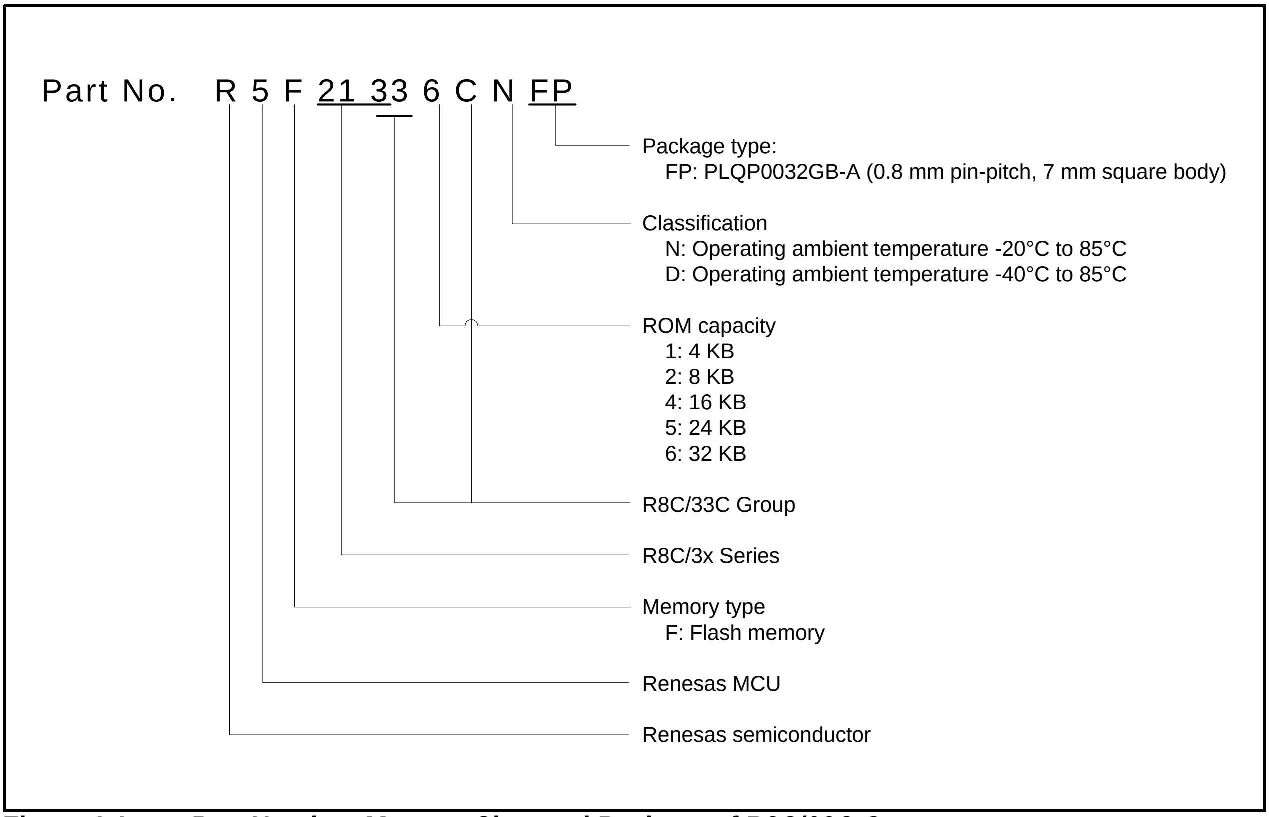
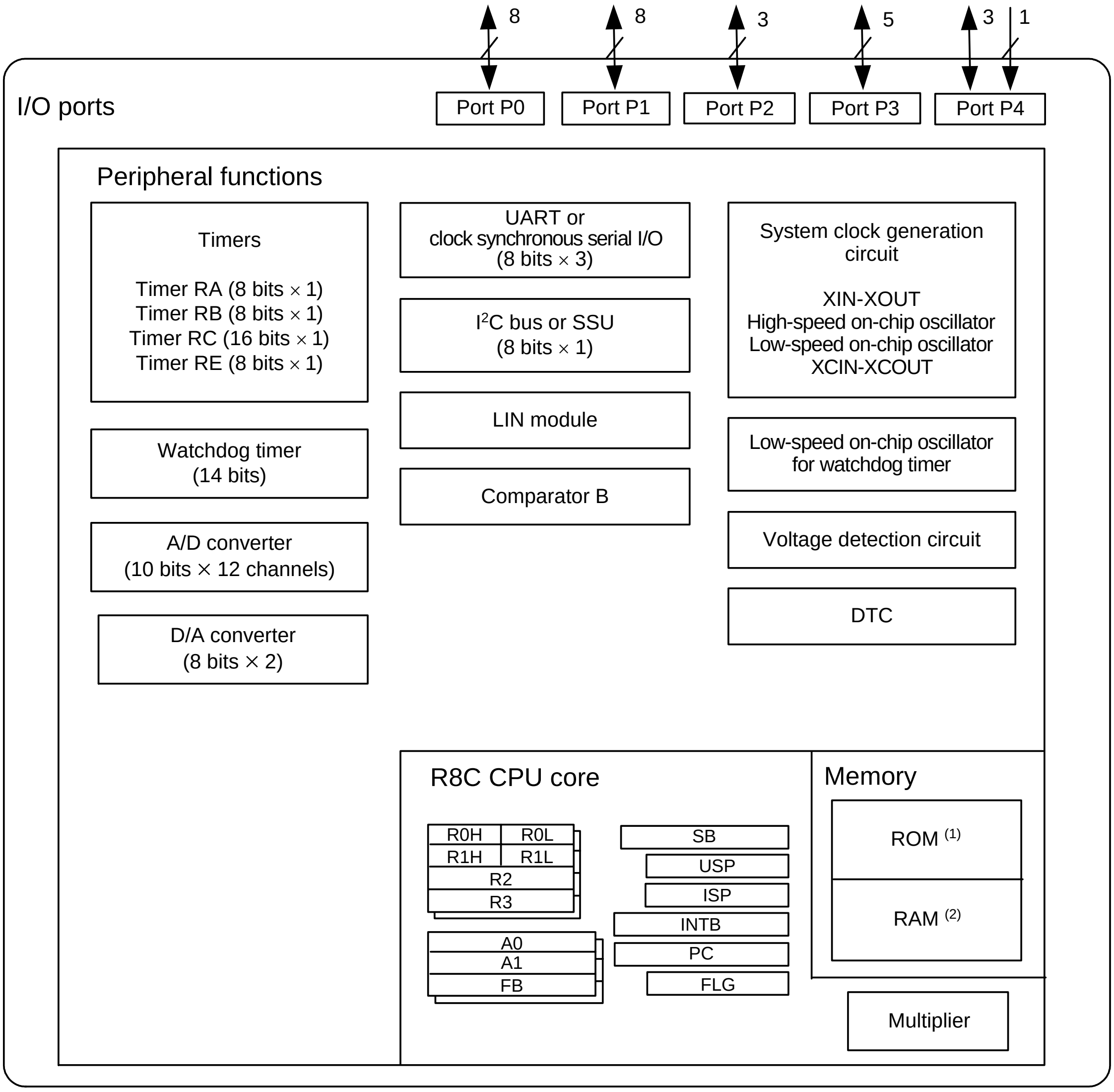


Figure 1.1 Part Number, Memory Size, and Package of R8C/33C Group

1.3 Block Diagram

Figure 1.2 shows a Block Diagram.



Notes:
1. ROM size varies with MCU type.
2. RAM size varies with MCU type.

Figure 1.2 Block Diagram

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A0 Register	DA0	00h
00D9h	D/A1 Register	DA1	00h
00DAh			
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h	UART1 Transmit/Receive Mode Register	U1MR	00h
0161h	UART1 Bit Rate Register	U1BRG	XXh
0162h	UART1 Transmit Buffer Register	U1TB	XXh
0163h			XXh
0164h	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
0165h	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
0166h	UART1 Receive Buffer Register	U1RB	XXh
0167h			XXh
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	After Reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACh			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		V_{ref} = AV_{CC}		–	–	10	Bit
–	Absolute accuracy	10-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±3	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±5	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±5	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±5	LSB
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
ϕAD	A/D conversion clock		$4.0 \leq V_{ref} = AV_{CC} \leq 5.5$ V (2)		2	–	20	MHz
			$3.2 \leq V_{ref} = AV_{CC} \leq 5.5$ V (2)		2	–	16	MHz
			$2.7 \leq V_{ref} = AV_{CC} \leq 5.5$ V (2)		2	–	10	MHz
			$2.2 \leq V_{ref} = AV_{CC} \leq 5.5$ V (2)		2	–	5	MHz
–	Tolerance level impedance				–	3	–	kΩ
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	–	–	µs
I_{Vref}	V_{ref} current		Vcc = 5 V, XIN = f1 = ϕAD = 20 MHz		–	45	–	µA
V_{ref}	Reference voltage				2.2	–	AV_{CC}	V
V_{IA}	Analog input voltage (3)				0	–	V_{ref}	V
OCVREF	On-chip reference voltage		$2 \text{ MHz} \leq \phi AD \leq 4$ MHz		1.19	1.34	1.49	V

Notes:
1. V_{CC}/AV_{CC} = V_{ref} = 2.2 to 5.5 V, V_{SS} = 0 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 D/A Converter Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution		–	–	8	Bit
–	Absolute accuracy		–	–	2.5	LSB
t_{su}	Setup time		–	–	3	µs
R_O	Output resistor		–	6	–	kΩ
I_{Vref}	Reference power input current	(Note 2)	–	–	1.5	mA

Notes:
1. $V_{CC}/AV_{CC} = V_{ref}$ = 2.7 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. This applies when one D/A converter is used and the value of the DAi register (i = 0 or 1) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included.

Table 5.5 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vref	IVREF1, IVREF3 input reference voltage		0	–	V_{CC} – 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		–0.3	–	V_{CC} + 0.3	V
–	Offset		–	5	100	mV
t_d	Comparator output delay time (2)	V_I = Vref ± 100 mV	–	0.1	–	µs
I_{CMP}	Comparator operating current	V_{CC} = 5.0 V	–	17.5	–	µA

Notes:
1. V_{CC} = 2.7 to 5.5 V, T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. When the digital filter is disabled.

Table 5.6 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (2)		1,000 (3)	–	–	times
–	Byte program time		–	80	500	µs
–	Block erase time		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	5+CPU clock × 3 cycles	ms
–	Interval from erase start/restart until following suspend request		0	–	–	µs
–	Time from suspend until erase restart		–	–	30+CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30+CPU clock × 1 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time (7)	Ambient temperature = 55°C	20	–	–	year

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.8 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (2)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (2)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (2)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (2)		3.55	3.80	4.05	V
–	Voltage detection 0 circuit response time (4)	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	–	6	150	µs
–	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V	–	1.5	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		–	–	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.9 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 (2)	At the falling of V_{CC}	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (2)	At the falling of V_{CC}	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (2)	At the falling of V_{CC}	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (2)	At the falling of V_{CC}	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (2)	At the falling of V_{CC}	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (2)	At the falling of V_{CC}	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (2)	At the falling of V_{CC}	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (2)	At the falling of V_{CC}	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (2)	At the falling of V_{CC}	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 (2)	At the falling of V_{CC}	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A (2)	At the falling of V_{CC}	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (2)	At the falling of V_{CC}	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C (2)	At the falling of V_{CC}	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (2)	At the falling of V_{CC}	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E (2)	At the falling of V_{CC}	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (2)	At the falling of V_{CC}	4.20	4.45	4.75	V
–	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	–	0.07	–	V
		Vdet1_6 to Vdet1_F selected	–	0.10	–	V
–	Voltage detection 1 circuit response time (3)	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	–	60	150	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	1.7	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (4)		–	–	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.12 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	High-speed on-chip oscillator frequency after reset	V_{CC} = 1.8 V to 5.5 V –20°C ≤ T_{opr} ≤ 85°C	38.4	40	41.6	MHz
		V_{CC} = 1.8 V to 5.5 V –40°C ≤ T_{opr} ≤ 85°C	38.0	40	42.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (2)	V_{CC} = 1.8 V to 5.5 V –20°C ≤ T_{opr} ≤ 85°C	35.389	36.864	38.338	MHz
		V_{CC} = 1.8 V to 5.5 V –40°C ≤ T_{opr} ≤ 85°C	35.020	36.864	38.707	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	V_{CC} = 1.8 V to 5.5 V –20°C ≤ T_{opr} ≤ 85°C	30.72	32	33.28	MHz
		V_{CC} = 1.8 V to 5.5 V –40°C ≤ T_{opr} ≤ 85°C	30.40	32	33.60	MHz
–	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25°C	–	0.5	3	ms
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	400	–	µA

Notes:
1. V_{CC} = 1.8 to 5.5 V, T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.13 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
f_{OCO-S}	Low-speed on-chip oscillator frequency		60	125	250	kHz
–	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25°C	–	30	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	2	–	µA

Note:
1. V_{CC} = 1.8 to 5.5 V, T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 5.14 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		–	–	2,000	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

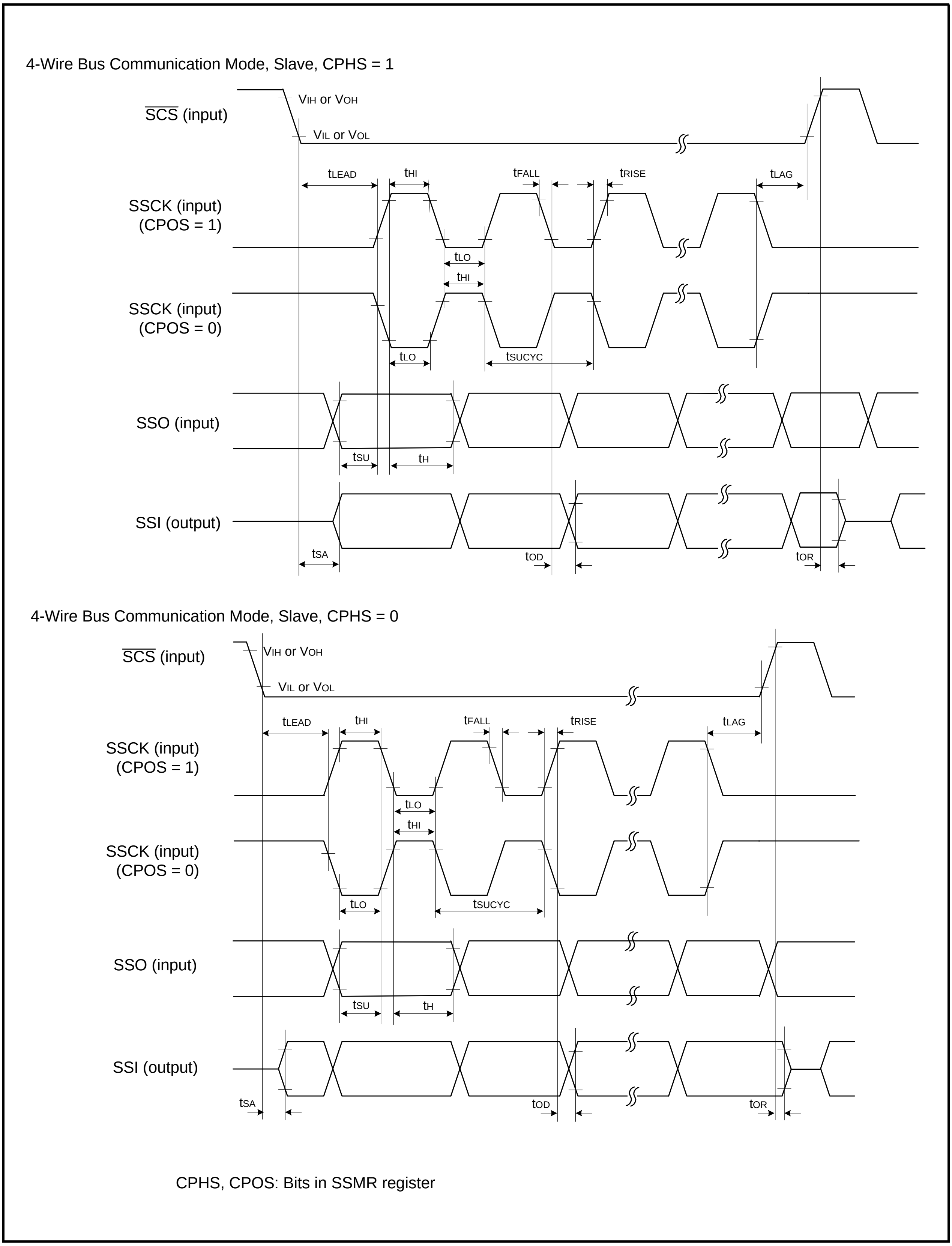


Figure 5.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

Table 5.17 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output "H" voltage	Other than XOUT	Drive capacity High V_{CC} = 5 V	I_{OH} = –20 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity Low V_{CC} = 5 V	I_{OH} = –5 mA	V_{CC} – 2.0	–	V_{CC}	V
		XOUT	V_{CC} = 5 V	I_{OH} = –200 μA	1.0	–	V_{CC}	V
V_{OL}	Output "L" voltage	Other than XOUT	Drive capacity High V_{CC} = 5 V	I_{OL} = 20 mA	–	–	2.0	V
			Drive capacity Low V_{CC} = 5 V	I_{OL} = 5 mA	–	–	2.0	V
		XOUT	V_{CC} = 5 V	I_{OL} = 200 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.1	1.2	–	V
		$\overline{RESET}$			0.1	1.2	–	V
I_{IH}	Input "H" current		VI = 5 V, V_{CC} = 5.0 V		–	–	5.0	μA
I_{IL}	Input "L" current		VI = 0 V, V_{CC} = 5.0 V		–	–	–5.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5.0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			–	0.3	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	8	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. 4.2 V ≤ V_{CC} ≤ 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.18 Electrical Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6.5	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.3	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.2	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	–	1	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	400	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	–	85	400	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	–	47	–	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	15	100	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	4	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	3.5	–	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	5.0	–	µA

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Table 5.23 Electrical Characteristics (3) [2.7 V ≤ Vcc < 4.2 V]

Symbol	Parameter		Condition		Standard Min.	Standard Typ.	Standard Max.	Unit
V_{OH}	Output "H" voltage	Other than XOUT	Drive capacity High	I_{OH} = –5 mA	V_{CC} – 0.5	–	V_{CC}	V
			Drive capacity Low	I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
		XOUT		I_{OH} = –200 μA	1.0	–	V_{CC}	V
V_{OL}	Output "L" voltage	Other than XOUT	Drive capacity High	I_{OL} = 5 mA	–	–	0.5	V
			Drive capacity Low	I_{OL} = 1 mA	–	–	0.5	V
		XOUT		I_{OL} = 200 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$, $\overline{\text{KI0}}$, $\overline{\text{KI1}}$, $\overline{\text{KI2}}$, $\overline{\text{KI3}}$, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, $\overline{\text{TRCTRG}}$, TRCCLK, $\overline{\text{ADTRG}}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO	V_{CC} = 3.0 V		0.1	0.4	–	V
		$\overline{\text{RESET}}$	V_{CC} = 3.0 V		0.1	0.5	–	V
I_{IH}	Input "H" current		VI = 3 V, V_{CC} = 3.0 V		–	–	4.0	μA
I_{IL}	Input "L" current		VI = 0 V, V_{CC} = 3.0 V		–	–	–4.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 3.0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			–	0.3	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	8	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. 2.7 V ≤ V_{CC} < 4.2 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.27 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{W(CKH)}$	CLKi input “H” width	150	–	ns
$t_{W(CKL)}$	CLKi Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 to 2

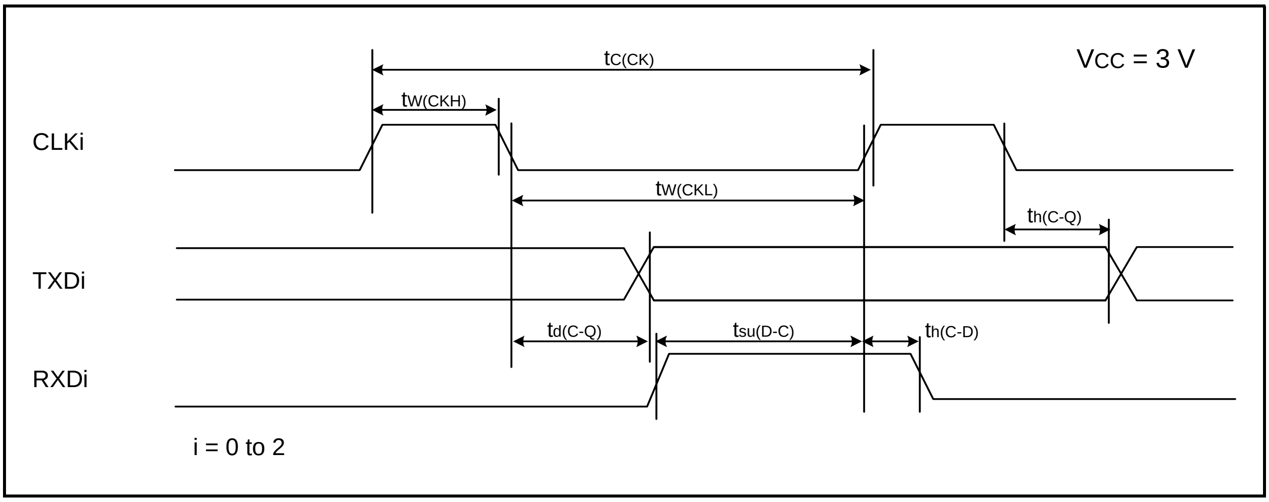

Figure 5.14 Serial Interface Timing Diagram when V_{CC} = 3 V

Table 5.28 External Interrupt $\overline{\text{INTi}}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{\text{KIi}}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{\text{INTi}}$ input “H” width, $\overline{\text{KIi}}$ input “H” width	380 (1)	–	ns
$t_{W(INL)}$	$\overline{\text{INTi}}$ input “L” width, $\overline{\text{KIi}}$ input “L” width	380 (2)	–	ns

Notes:
1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

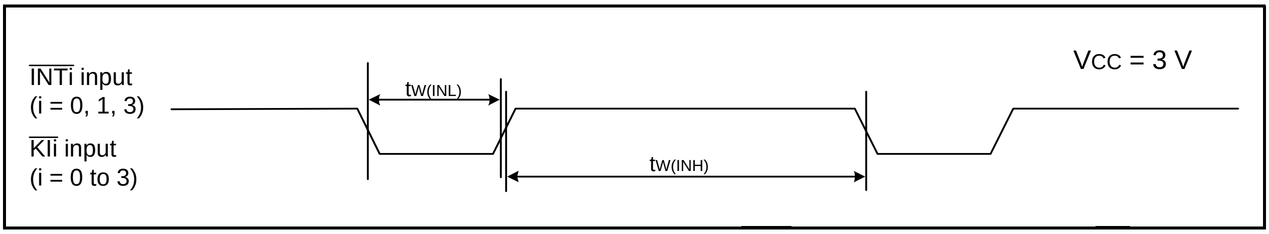

Figure 5.15 Input Timing Diagram for External Interrupt $\overline{\text{INTi}}$ and Key Input Interrupt $\overline{\text{KIi}}$ when Vcc = 3 V

Timing requirements
(Unless Otherwise Specified: VCC = 2.2 V, VSS = 0 V at Topr = 25°C)

Table 5.31 External Clock Input (XOUT, XCIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(XOUT)	XOUT input cycle time	200	–	ns
tWH(XOUT)	XOUT input "H" width	90	–	ns
tWL(XOUT)	XOUT input "L" width	90	–	ns
tc(XCIN)	XCIN input cycle time	14	–	µs
tWH(XCIN)	XCIN input "H" width	7	–	µs
tWL(XCIN)	XCIN input "L" width	7	–	µs

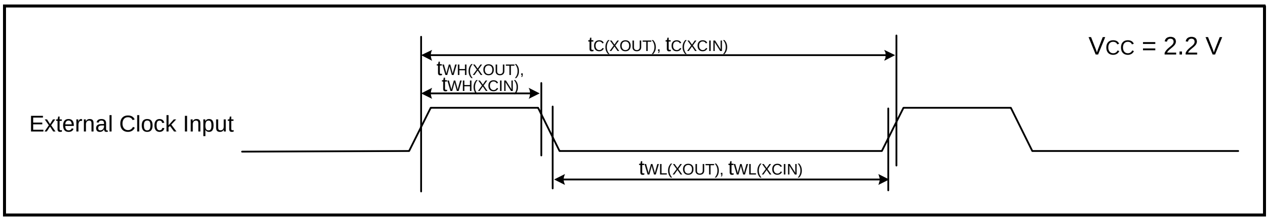

Figure 5.16 External Clock Input Timing Diagram when VCC = 2.2 V

Table 5.32 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TRAIO)	TRAIO input cycle time	500	–	ns
tWH(TRAIO)	TRAIO input "H" width	200	–	ns
tWL(TRAIO)	TRAIO input "L" width	200	–	ns

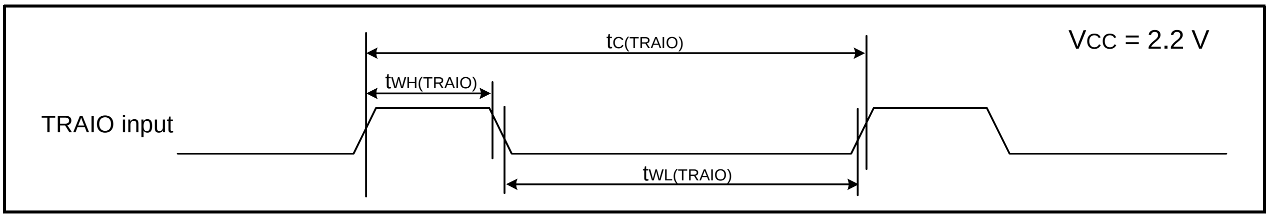

Figure 5.17 TRAIO Input Timing Diagram when VCC = 2.2 V

Table 5.33 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	–	ns
$t_{W(CKH)}$	CLKi input “H” width	400	–	ns
$t_{W(CKL)}$	CLKi input “L” width	400	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	150	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 to 2

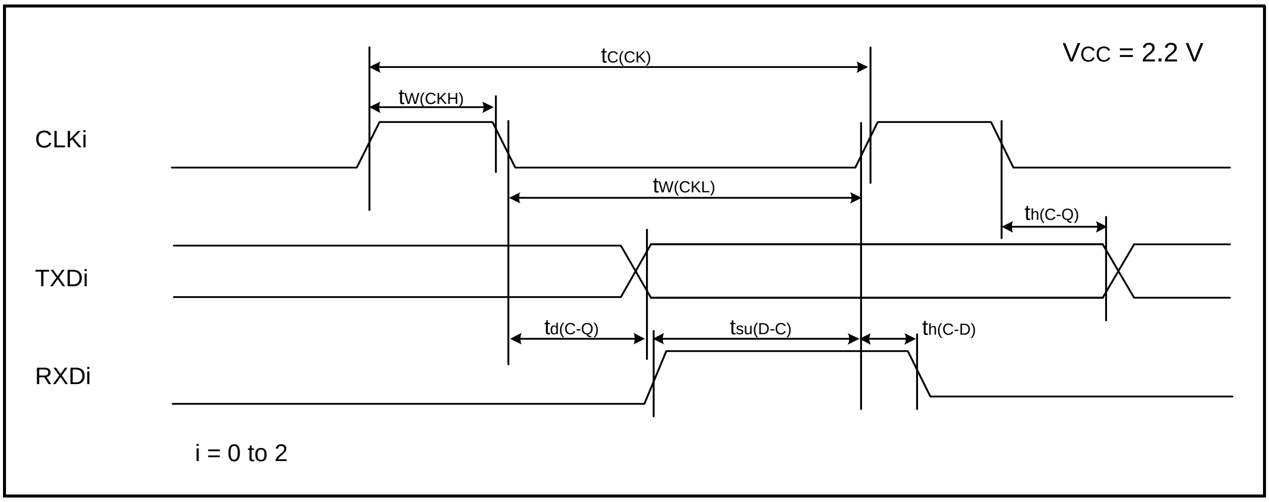

Figure 5.18 Serial Interface Timing Diagram when VCC = 2.2 V

Table 5.34 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	1000 (1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	1000 (2)	–	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

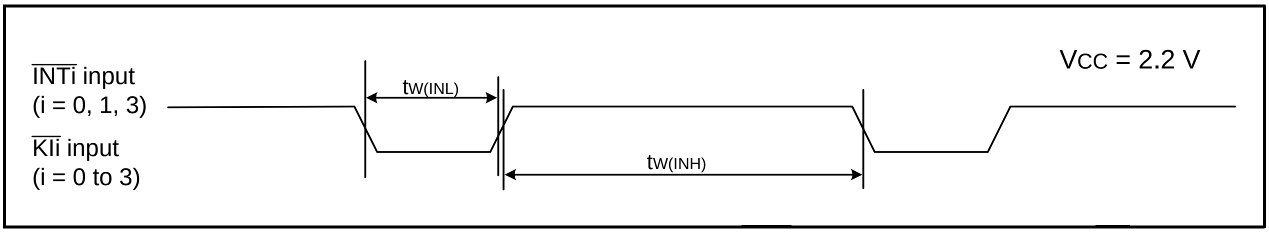

Figure 5.19 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 2.2 V

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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