Infineon Technologies - MB9AF155NAPMC-G-JNE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

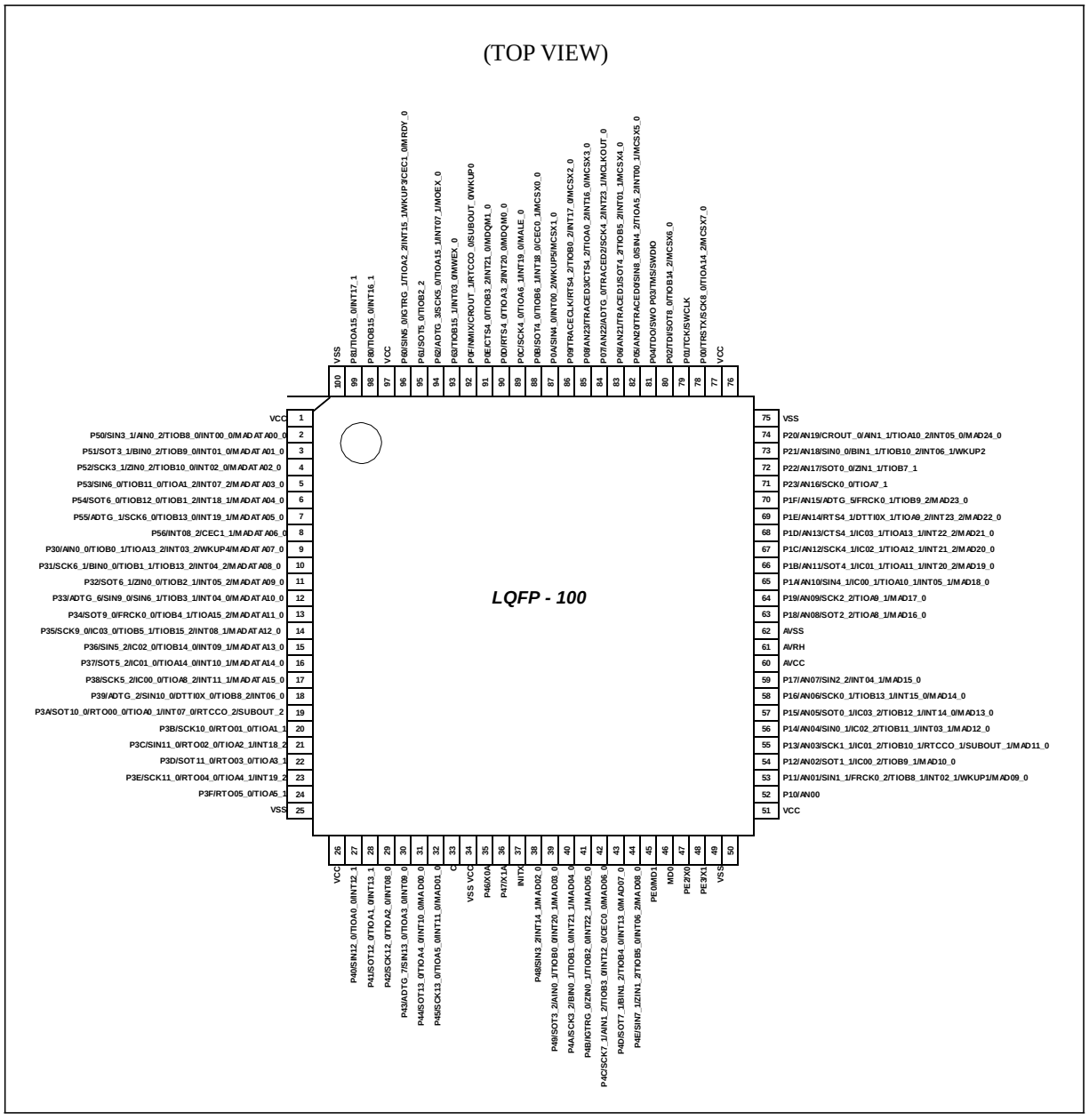
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, EBI/EMI, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	416KB (416K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9af155napmc-g-jne2

■ PRODUCT LINEUP

- Memory size

Product name		MB9AF154MA/NA/RA	MB9AF155MA/NA/RA	MB9AF156MA/NA/RA
On-chip Flash memory	Main area	256 Kbytes	384 Kbytes	512 Kbytes
	Work area	32 Kbytes	32 Kbytes	32 Kbytes
On-chip SRAM	SRAM0	16 Kbytes	24 Kbytes	32 Kbytes
	SRAM1	16 Kbytes	24 Kbytes	32 Kbytes
	Total	32 Kbytes	48 Kbytes	64 Kbytes

- FPT-100P-M23



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No					Pin Name	I/O circuit type	Pin state type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
18	-	-	-	-	P34 SOT9_0 (SDA9_0) FRCK0_0 TIOB4_1 TIOA15_2 MNALE_0	E	J
-	13	F1	-	-	P34 SOT9_0 (SDA9_0) FRCK0_0 TIOB4_1 TIOA15_2 MADATA11_0	E	J
19	-	-	-	-	P35 SCK9_0 (SCL9_0) IC03_0 TIOB5_1 TIOB15_2 INT08_1 MNCLE_0	E	K
-	14	F2	-	-	P35 SCK9_0 (SCL9_0) IC03_0 TIOB5_1 TIOB15_2 INT08_1 MADATA12_0	E	K
20	-	-	-	-	P36 SIN5_2 IC02_0 TIOB14_0 INT09_1 MNWEX_0	E	K
-	15	F3	-	-	P36 SIN5_2 IC02_0 TIOB14_0 INT09_1 MADATA13_0	E	K
-	-	-	-	F1	VSS	-	
-	-	-	-	F2	VSS	-	
-	-	-	-	F3	VSS	-	

Pin No					Pin Name	I/O circuit type	Pin state type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
63	53	J10	43	J10	P11 AN01 SIN1_1 FRCK0_2 TIOB8_1 INT02_1 WKUP1 MAD09_0	F	P
64	54	J8	44	J8	P12 AN02 SOT1_1 (SDA1_1) IC00_2 TIOB9_1 MAD10_0	F	L
-	-	K10	-	K10	VSS	-	
-	-	J9	-	J9	VSS	-	
65	55	H10	45	H10	P13 AN03 SCK1_1 (SCL1_1) IC01_2 TIOB10_1 RTCCO_1 SUBOUT_1 MAD11_0	F	L
66	56	H9	46	H9	P14 AN04 SIN0_1 IC02_2 TIOB11_1 INT03_1 MAD12_0	F	M
67	57	H7	47	G10	P15 AN05 SOT0_1 (SDA0_1) IC03_2 TIOB12_1 INT14_0 MAD13_0	F	M

Pin No					Pin Name	I/O circuit type	Pin state type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
77	67	E10	-	-	P1C AN12 SCK4_1 (SCL4_1) IC02_1 TIOA12_1 INT21_2 MAD20_0	F	M
78	68	F8	-	-	P1D AN13 CTS4_1 IC03_1 TIOA13_1 INT22_2 MAD21_0	F	M
79	69	E9	-	-	P1E AN14 RTS4_1 DTTI0X_1 TIOA9_2 INT23_2 MAD22_0	F	M
80	70	D11	-	-	P1F AN15 ADTG_5 FRCK0_1 TIOB9_2 MAD23_0	F	L
	-	-	-	-	SCK15_0 (SCL15_0)		
-	-	B10	-	B10	VSS	-	
-	-	C9	-	C9	VSS	-	
-	-	-	-	D11	VSS	-	
81	-	-	-	-	P28 ADTG_4 SOT15_0 (SDA15_0) RTO05_1 TIOB6_2	E	J
82	-	-	-	-	P27 SIN15_0 RTO04_1 TIOA6_2 INT02_2	E	K

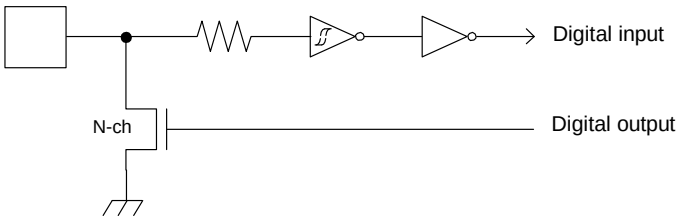
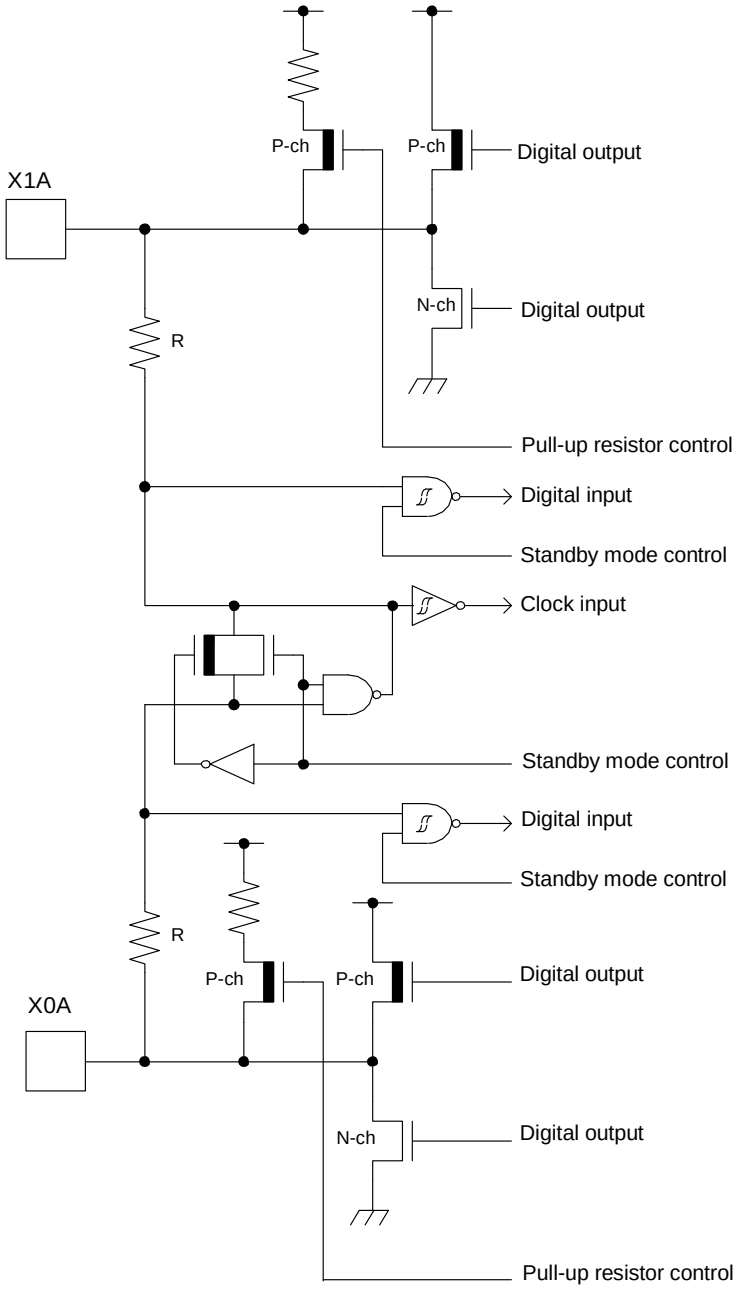
Pin No					Pin Name	I/O circuit type	Pin state type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
107	92	B5	72	A6	P0F NMIX CROUT_1 RTCCO_0 SUBOUT_0 WKUP0	E	H
108	-	-	-	-	P68 SCK3_0 (SCL3_0) TIOB7_2 INT12_2	E	K
109	-	-	-	-	P67 SOT3_0 (SDA3_0) TIOA7_2 INT22_0	E	K
110	-	-	-	-	P66 SIN3_0 TIOA12_2 INT11_2	E	K
111	-	-	-	-	P65 SCK5_1 (SCL5_1) TIOB7_0 TIOB12_2 INT23_0	E	K
112	-	-	-	-	P64 SOT5_1 (SDA5_1) TIOA7_0 INT10_2	E	K
113	93	D6	73	B5	P63 TIOB15_1 INT03_0 MWEX_0	E	K
	-	-	-	-	SIN5_1		
114	94	C5	74	C5	P62 ADTG_3 SCK5_0 (SCL5_0) TIOA15_1 INT07_1 MOEX_0	E	K

- List of pin functions

  The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin function	Pin name	Function description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
ADC	ADTG_0	A/D converter external trigger input pin	99	84	A7	66	A8
	ADTG_1		7	7	D3	7	D3
	ADTG_2		23	18	F4	13	G3
	ADTG_3		114	94	C5	74	C5
	ADTG_4		81	-	-	-	-
	ADTG_5		80	70	D11	-	-
	ADTG_6		17	12	E4	12	G2
	ADTG_7		35	30	J5	-	-
	ADTG_8		-	-	-	-	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	62	52	J11	42	J11
	AN01		63	53	J10	43	J10
	AN02		64	54	J8	44	J8
	AN03		65	55	H10	45	H10
	AN04		66	56	H9	46	H9
	AN05		67	57	H7	47	G10
	AN06		68	58	G10	48	G9
	AN07		69	59	G9	49	F10
	AN08		73	63	G8	53	F9
	AN09		74	64	F10	54	E11
	AN10		75	65	F9	55	E10
	AN11		76	66	E11	56	E9
	AN12		77	67	E10	-	-
	AN13		78	68	F8	-	-
	AN14		79	69	E9	-	-
	AN15		80	70	D11	-	-
	AN16		86	71	D10	57	D10
	AN17		87	72	E8	58	D9
	AN18		88	73	C11	59	C11
	AN19		89	74	C10	60	C10
	AN20		97	82	C8	-	-
	AN21		98	83	D9	-	-
	AN22		99	84	A7	66	A8
	AN23		100	85	B7	-	-

Pin function	Pin name	Function description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
GPIO	P00	General-purpose I/O port 0	92	77	A9	61	A10
	P01		93	78	B9	62	B9
	P02		94	79	B11	63	B11
	P03		95	80	A8	64	A9
	P04		96	81	B8	65	B8
	P05		97	82	C8	-	-
	P06		98	83	D9	-	-
	P07		99	84	A7	66	A8
	P08		100	85	B7	-	-
	P09		101	86	C7	-	-
	P0A		102	87	D7	67	C8
	P0B		103	88	A6	68	C7
	P0C		104	89	B6	69	B7
	P0D		105	90	C6	70	B6
	P0E		106	91	A5	71	C6
	P0F		107	92	B5	72	A6
	P10	General-purpose I/O port 1	62	52	J11	42	J11
	P11		63	53	J10	43	J10
	P12		64	54	J8	44	J8
	P13		65	55	H10	45	H10
	P14		66	56	H9	46	H9
	P15		67	57	H7	47	G10
	P16		68	58	G10	48	G9
	P17		69	59	G9	49	F10
	P18		73	63	G8	53	F9
	P19		74	64	F10	54	E11
	P1A		75	65	F9	55	E10
	P1B		76	66	E11	56	E9
	P1C		77	67	E10	-	-
	P1D		78	68	F8	-	-
	P1E		79	69	E9	-	-
	P1F		80	70	D11	-	-
	P20	General-purpose I/O port 2	89	74	C10	60	C10
	P21		88	73	C11	59	C11
	P22		87	72	E8	58	D9
	P23		86	71	D10	57	D10
	P24		85	-	-	-	-
	P25		84	-	-	-	-
	P26		83	-	-	-	-
	P27		82	-	-	-	-
	P28		81	-	-	-	-

Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 5MΩ • With standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 33kΩ • I_{OH}= -4mA, I_{OL}= 4mA

■ HANDLING PRECAUTIONS

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Spansion semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- **Absolute Maximum Ratings**

  Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- **Recommended Operating Conditions**

  Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

  Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

  No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- **Processing and Protection of Pins**

  These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

  (1) Preventing Over-Voltage and Over-Current Conditions

  Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

  (2) Protection of Output Pins

  Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
  Therefore, avoid this type of connection.

  (3) Handling of Unused Input Pins

  Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- **Latch-up**

  Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

  CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

  (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

  (2) Be sure that abnormal current flows do not occur during the power-on sequence.

- Observance of Safety Regulations and Standards

  Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- Fail-Safe Design

  Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- Precautions Related to Usage of Devices

  Spansion semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

  CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Spansion's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- Lead Insertion Type

  Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

  Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Spansion recommended mounting conditions.

  If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- Surface Mount Type

  Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

  You must use appropriate mounting techniques. Spansion Inc. recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Spansion ranking of recommended conditions.

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	TIMER mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
F	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
G	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z/ Internal input fixed at "0"	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ or Input enable	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state	Maintain previous state/When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*2, Hi-Z/ Internal input fixed at "0"	Maintain previous state/When oscillation stops*2, Hi-Z/ Internal input fixed at "0"	Maintain previous state/When oscillation stops*2, Hi-Z/ Internal input fixed at "0"
H	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	TIMER mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
Q	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected							GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									
R	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									
S	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected							GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									

*1: Oscillation is stopped at Sub timer mode, Low-speed CR timer mode, RTC mode, STOP mode, Deep standby RTC mode, and Deep standby STOP mode.

*2: Oscillation is stopped at STOP mode and Deep standby STOP mode.

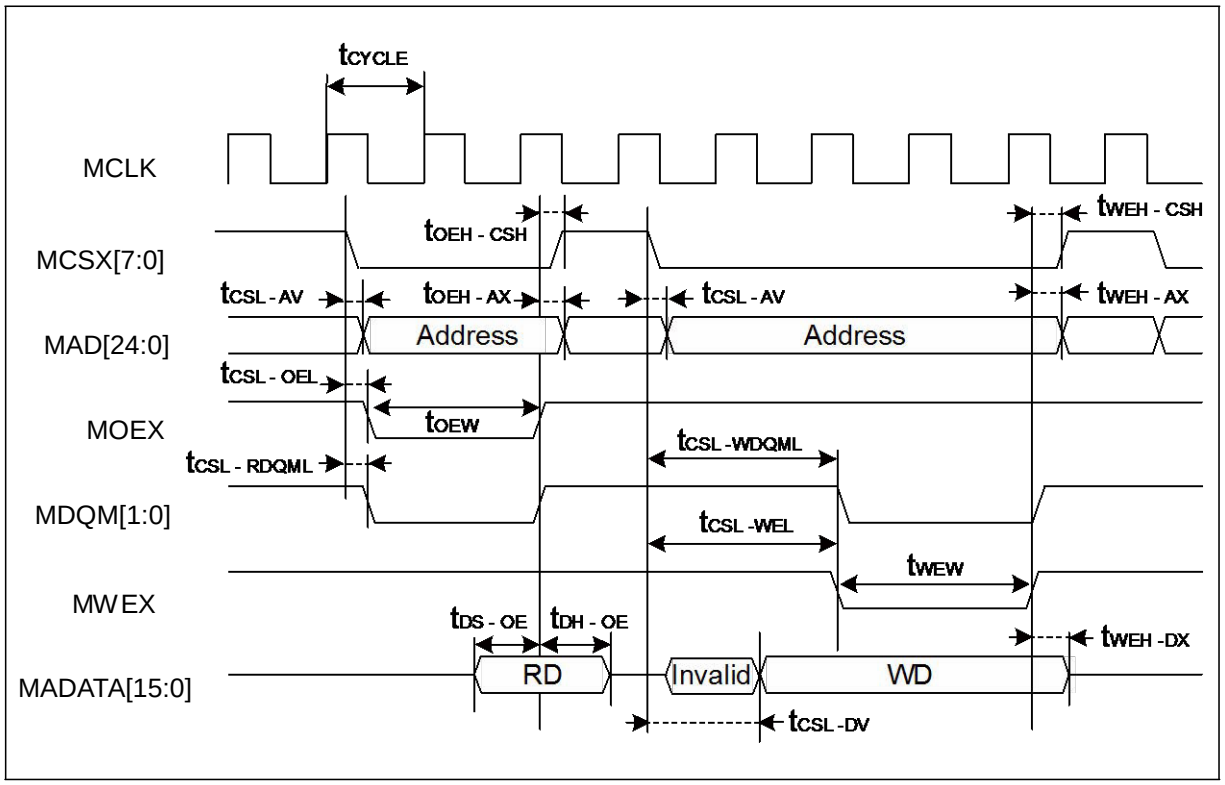
3. DC Characteristics

(1) Current rating

(V_{CC} = AV_{CC} = 1.65V to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions		Value Typ	Value Max	Unit	Remarks
Power supply current	I_{CC}	VCC	Normal operation (PLL)	CPU : 40 MHz, Peripheral : 40 MHz *1, *3	17.5	23.7	mA	
				CPU : 40 MHz, Peripheral : the clock stops NOP operation *1, *3	8	11	mA	
			Normal operation (built-in high-speed CR)	CPU/ Peripheral : 4 MHz*2 *1	1.9	3.1	mA	
			Normal operation (sub oscillation)	CPU/ Peripheral : 32 kHz *1, *4	120	810	µA	
			Normal operation (built-in low-speed CR)	CPU/ Peripheral : 100 kHz *1	140	830	µA	
	I_{CCS}		SLEEP operation (PLL)	Peripheral : 40 MHz *1, *3	11	15	mA	
			SLEEP operation (built-in high-speed CR)	Peripheral : 4 MHz*2 *1	0.82	1.7	mA	
			SLEEP operation (sub oscillation)	Peripheral : 32 kHz *1, *4	105	800	µA	
			SLEEP operation (built-in low-speed CR)	Peripheral : 100 kHz *1	125	810	µA	
	I_{CCH}		STOP mode	Ta = + 25°C, When LVD is off *1	11	38	µA	
				Ta = + 85°C, When LVD is off *1	-	370	µA	
	I_{CCT}		TIMER mode (sub oscillation)	Ta = + 25°C, When LVD is off *1, *4	15	45	µA	
				Ta = + 85°C, When LVD is off *1, *4	-	440	µA	
	I_{CCR}		RTC mode (sub oscillation)	Ta = + 25°C, When LVD is off *1, *4	13	40	µA	
				Ta = + 85°C, When LVD is off *1, *4	-	380	µA	

*1: When all ports are fixed.
*2: When setting it to 4 MHz by trimming.
*3:When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)
*4: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)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MCLK
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MAD[24:0]
MOEX
MDQM[1:0]
MWEX
MADATA[15:0]
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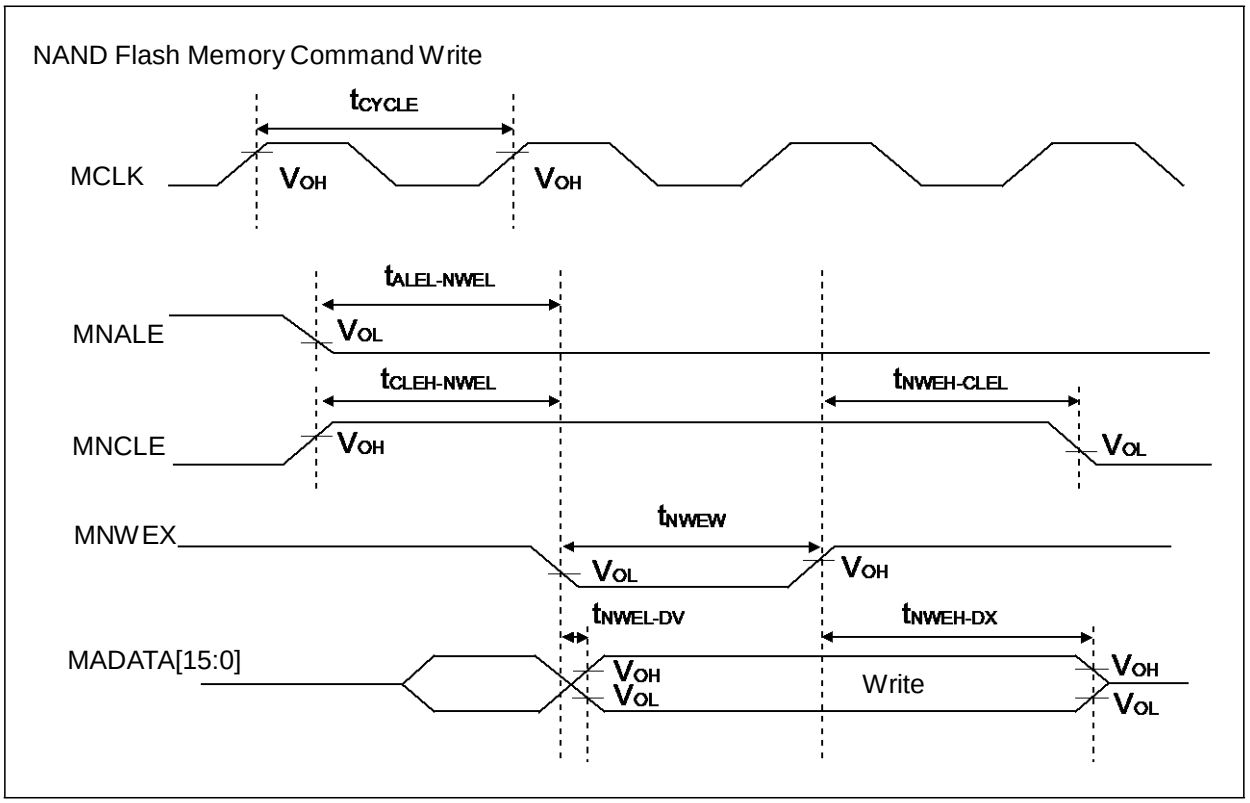
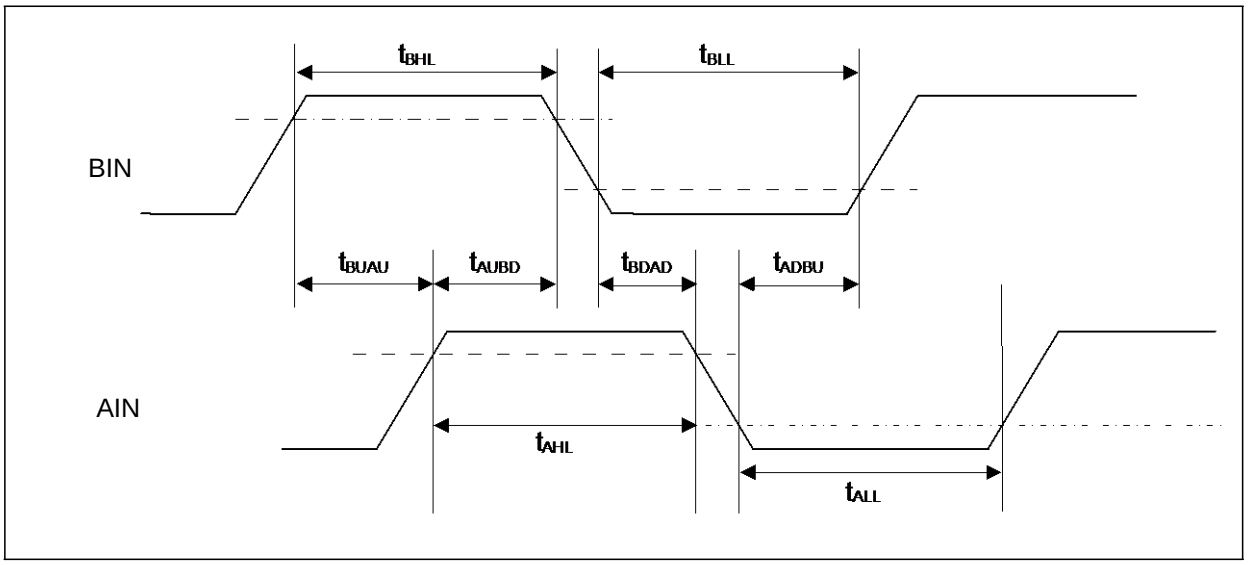
tWEH - CSH
tCSL - AV
tOEH - AX
tCSL - AV
tWEH - AX
Address
Address
tCSL - OEL
tOEW
tCSL - RDQML
tCSL -WDQML
tCSL -WEL
tWEW
tDS - OE
tDH - OE
tWEH -DX
RD
Invalid
WD
tCSL -DV

NAND Flash Memory Command Write




BIN
AIN
tBHL
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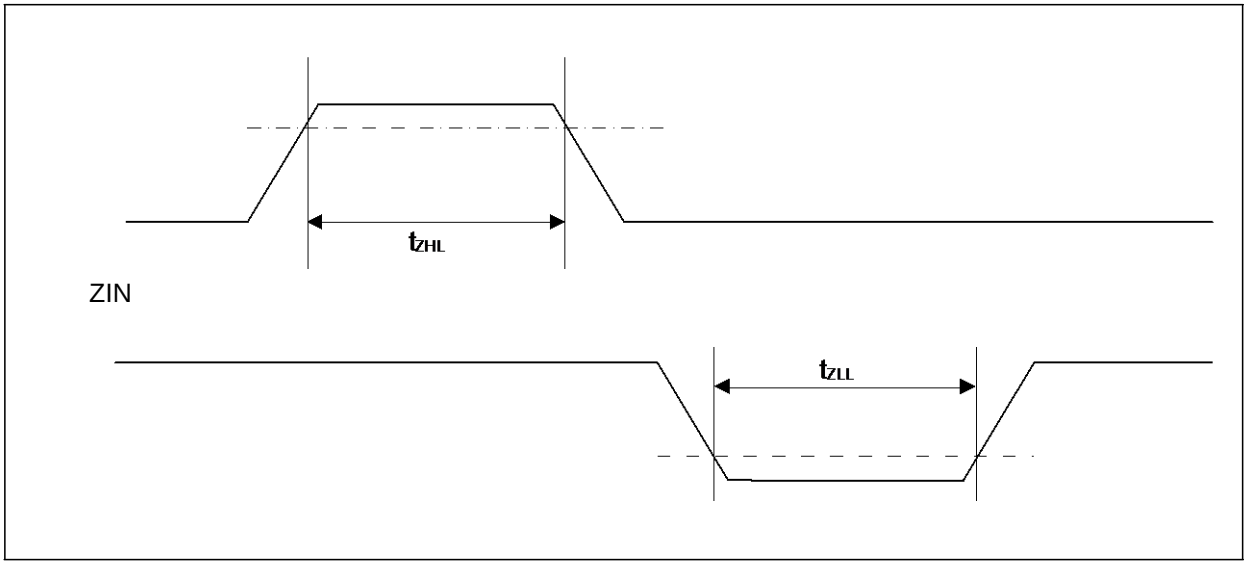
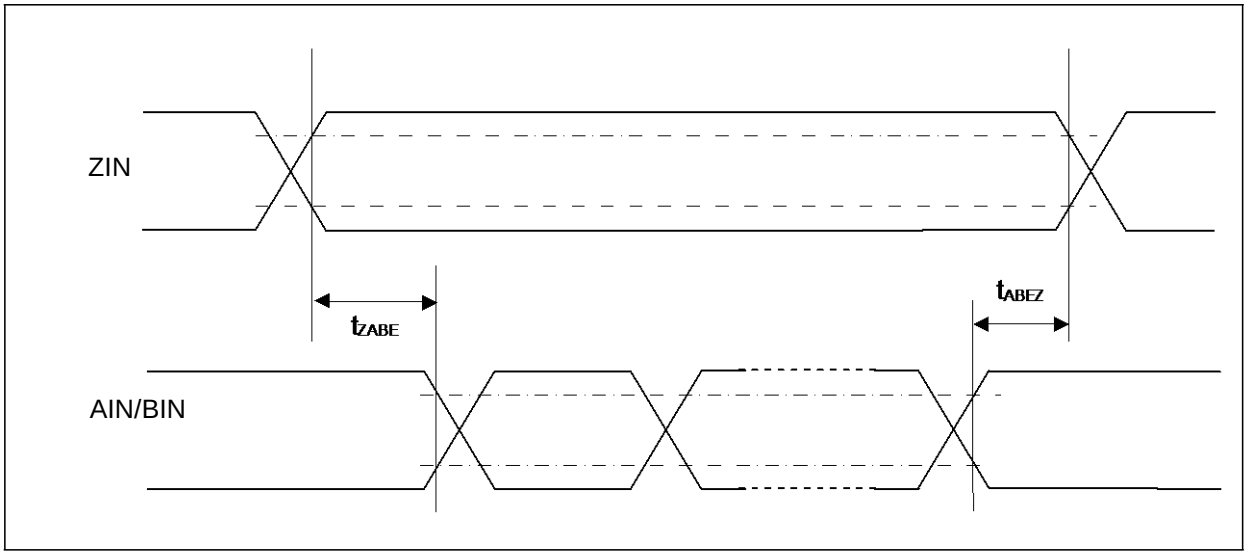
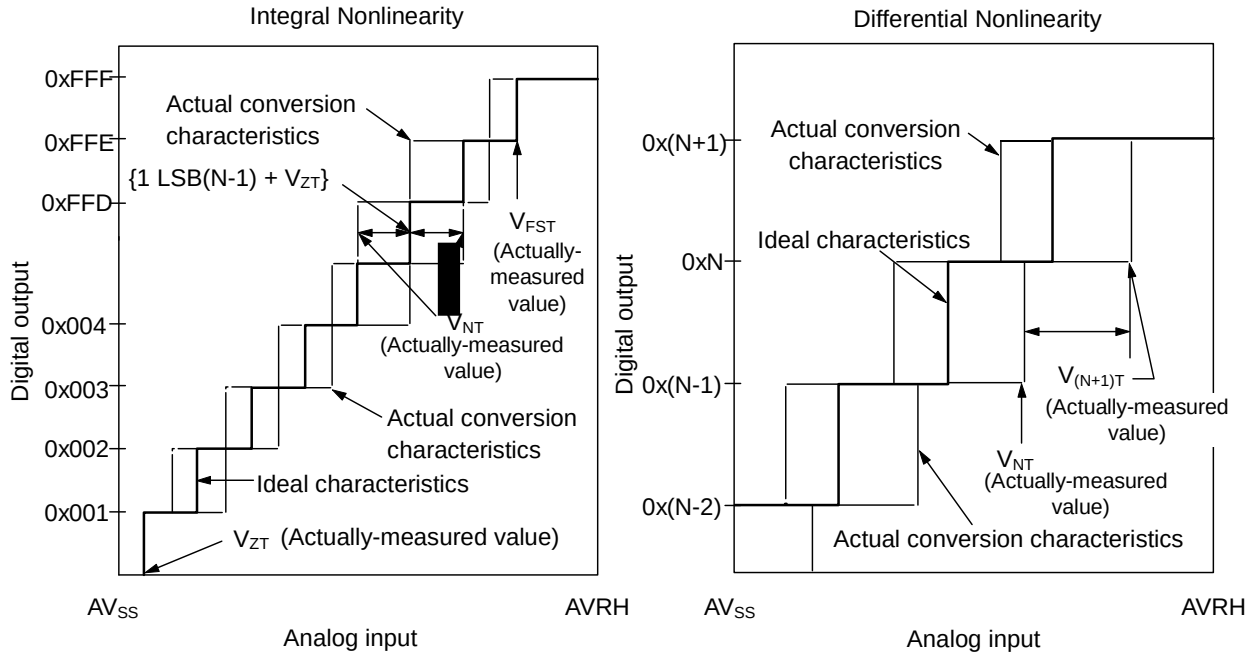
tADBU
tAHL
tALL


ZIN
tZHL
tZLL


ZIN
AIN/BIN
tZABE
tABEZ

- Definition of 12-bit A/D Converter Terms

  - Resolution : Analog variation that is recognized by an A/D converter.
  - Integral Nonlinearity : Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
  - Differential Nonlinearity : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT}-\{1LSB\times(N-1)+V_{ZT}\}}{1LSB}\ [LSB]$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T}-V_{NT}}{1LSB} - 1\ [LSB]$$

$$1LSB = \frac{V_{FST}-V_{ZT}}{4094}$$

N : A/D converter digital output value.
V_{ZT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

(2) Interrupt of Low-Voltage Detection

(Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00100	1.56	1.70	1.84	V	When voltage drops
Released voltage	VDH		1.61	1.75	1.89	V	When voltage rises
Detected voltage	VDL	SVHI = 00101	1.61	1.75	1.89	V	When voltage drops
Released voltage	VDH		1.66	1.80	1.94	V	When voltage rises
Detected voltage	VDL	SVHI = 00110	1.66	1.80	1.94	V	When voltage drops
Released voltage	VDH		1.70	1.85	2.00	V	When voltage rises
Detected voltage	VDL	SVHI = 00111	1.70	1.85	2.00	V	When voltage drops
Released voltage	VDH		1.75	1.90	2.05	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	1.75	1.90	2.05	V	When voltage drops
Released voltage	VDH		1.79	1.95	2.11	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	1.79	1.95	2.11	V	When voltage drops
Released voltage	VDH		1.84	2.00	2.16	V	When voltage rises
Detected voltage	VDL	SVHI = 01010	1.84	2.00	2.16	V	When voltage drops
Released voltage	VDH		1.89	2.05	2.21	V	When voltage rises
Detected voltage	VDL	SVHI = 01011	1.89	2.05	2.21	V	When voltage drops
Released voltage	VDH		1.93	2.10	2.27	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	2.30	2.50	2.70	V	When voltage drops
Released voltage	VDH		2.39	2.60	2.81	V	When voltage rises
Detected voltage	VDL	SVHI = 01101	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		2.48	2.70	2.92	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		2.58	2.80	3.02	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 10000	2.67	2.90	3.13	V	When voltage drops
Released voltage	VDH		2.76	3.00	3.24	V	When voltage rises
Detected voltage	VDL	SVHI = 10001	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI = 10010	2.85	3.10	3.35	V	When voltage drops
Released voltage	VDH		2.94	3.20	3.46	V	When voltage rises
Detected voltage	VDL	SVHI = 10011	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	5200 × t_{CYCP}*	µs	
LVD detection delay time	T_{LVDDL}	-	-	-	200	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

■ ORDERING INFORMATION

Part number	Package
MB9AF154MAPMC	Plastic・LQFP 80-pin (0.5mm pitch), (FPT-80P-M37)
MB9AF155MAPMC	
MB9AF156MAPMC	
MB9AF154MAPMC1	Plastic・LQFP 80-pin (0.65mm pitch), (FPT-80P-M40)
MB9AF155MAPMC1	
MB9AF156MAPMC1	
MB9AF154MABGL	Plastic・PFBGA 96-pin (0.5mm pitch), (BGA-96P-M07)
MB9AF155MABGL	
MB9AF156MABGL	
MB9AF154NAPMC	Plastic・LQFP 100-pin (0.5mm pitch), (FPT-100P-M23)
MB9AF155NAPMC	
MB9AF156NAPMC	
MB9AF154NAPQC	Plastic・QFP 100-pin (0.65mm pitch), (FPT-100P-M36)
MB9AF155NAPQC	
MB9AF156NAPQC	
MB9AF154NABGL	Plastic・PFBGA 112-pin (0.8mm pitch), (BGA-112P-M04)
MB9AF155NABGL	
MB9AF156NABGL	
MB9AF154RAPMC	Plastic・LQFP 120-pin (0.5mm pitch), (FPT-120P-M37)
MB9AF155RAPMC	
MB9AF156RAPMC	