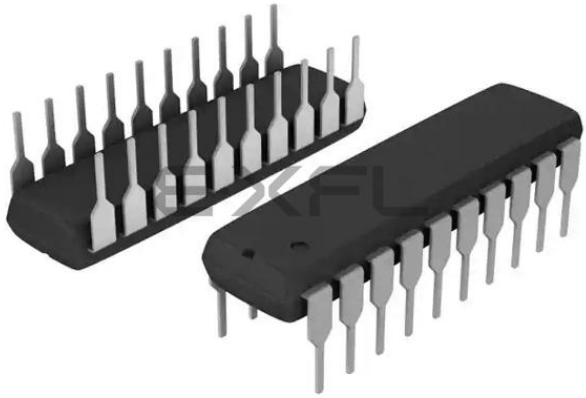

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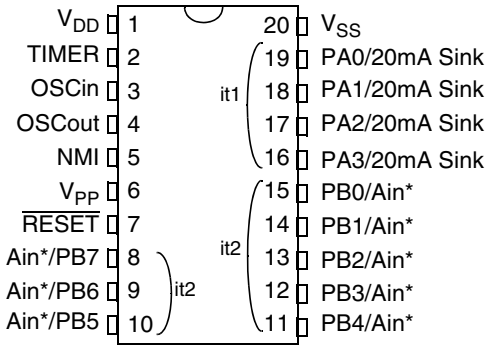
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST6
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	12
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st62t20cb3

2 PIN DESCRIPTION

Figure 2. 20-Pin Package Pinout



itX associated interrupt vector
* Depending on device. Please refer to I/O Port section.

Table 1. Device Pin Description

Pin n°	Pin Name	Type	Main Function (after Reset)	Alternate Function
1	V_{DD}	S	Main power supply	
2	TIMER	I/O	Timer input or output	
3	OSCin	I	External clock input or resonator oscillator inverter input	
4	OSCout	O	Resonator oscillator inverter output or resistor input for RC oscillator	
5	NMI	I	Non maskable interrupt (falling edge sensitive)	
6	V_{PP}		Must be held at Vss for normal operation, if a 12.5V level is applied to the pin during the reset phase, the device enters EPROM programming mode.	
7	$\overline{\text{RESET}}$	I/O	Top priority non maskable interrupt (active low)	
8	PB7/Ain*	I/O	Pin B7 (IPU)	Analog input
9	PB6/Ain*	I/O	Pin B6 (IPU)	Analog input
10	PB5/Ain*	I/O	Pin B5 (IPU)	Analog input
11	PB4/Ain*	I/O	Pin B4 (IPU)	Analog input
12	PB3/Ain*	I/O	Pin B3 (IPU)	Analog input
13	PB2/Ain*	I/O	Pin B2 (IPU)	Analog input
14	PB1/Ain*	I/O	Pin B1 (IPU)	Analog input
15	PB0/Ain*	I/O	Pin B0 (IPU)	Analog input
16	PA3/ 20mA Sink	I/O	Pin A3 (IPU)	
17	PA2/ 20mA Sink	I/O	Pin A2 (IPU)	
18	PA1/ 20mA Sink	I/O	Pin A1 (IPU)	

MEMORY MAP (Cont'd)

3.1.6.2 Data ROM Window memory addressing

In cases where some data (look-up tables for example) are stored in program memory, reading these data requires the use of the Data ROM window mechanism. To do this:

1. The DRWR register has to be loaded with the 64-byte block number where the data are located (in program memory). This number also gives the start address of the block.

2. Then, the offset address of the byte in the Data ROM Window (corresponding to the offset in the 64-byte block in program memory) has to be loaded in a register (A, X,...).

When the above two steps are completed, the data can be read.

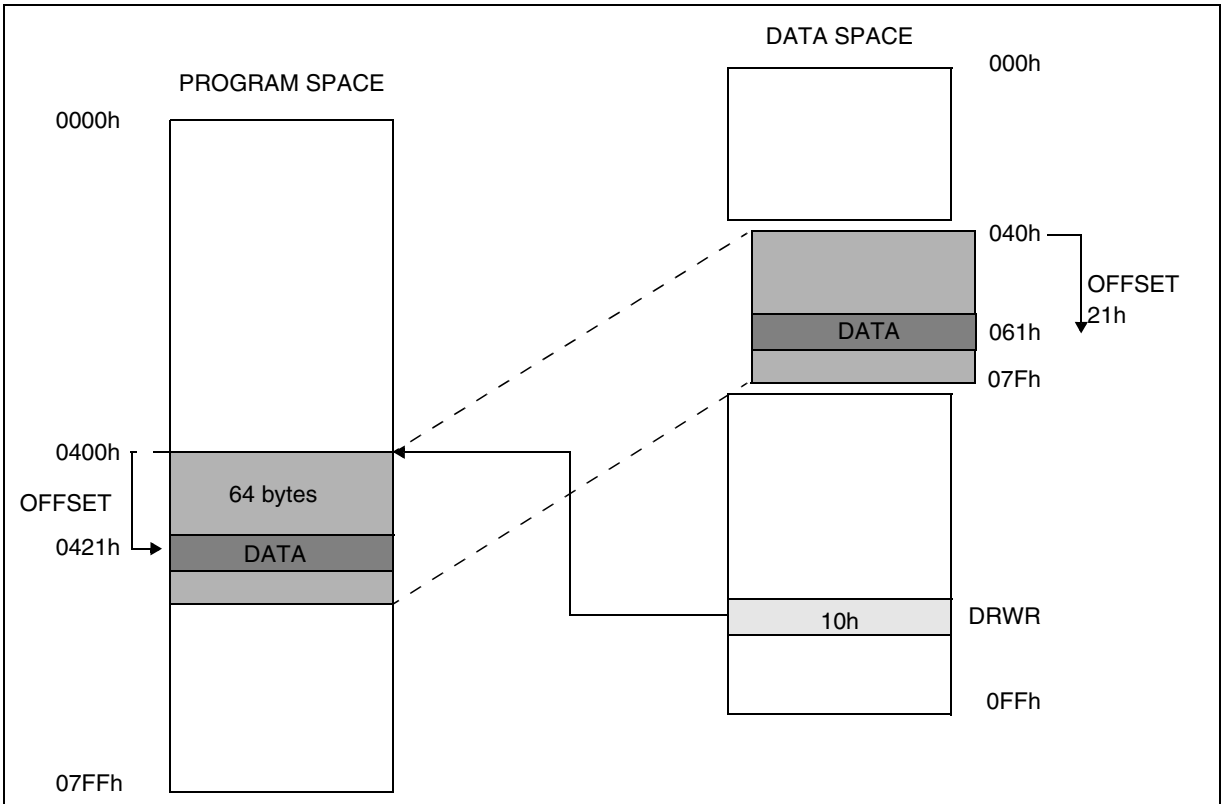
To understand how to determine the DRWR and the content of the register, please refer to the example shown in Figure 6. In any case the calculation is automatically handled by the ST6 development tools.

Please refer to the user manual of the correspoding tool.

3.1.6.3 Recommendations

Care is required when handling the DRWR register as it is write only. For this reason, the DRWR contents should not be changed while executing an interrupt service routine, as the service routine cannot save and then restore the register's previous contents. If it is impossible to avoid writing to the DRWR during the interrupt service routine, an image of the register must be saved in a RAM location, and each time the program writes to the DRWR, it must also write to the image register. The image register must be written first so that, if an interrupt occurs between the two instructions, the DRWR is not affected.

Figure 6. Data ROM Window Memory Addressing



DATA address in Program memory : 421h
DRWR content : 421h / 3Fh (64) = 10H data is located in 64-bytes window number 10h
64-byte window start address : 10h x 3Fh = 400h
Register (A, X,...)content : Offset = (421h - 400h) + 40h (Data ROM Window start address in data space) = 61h

3.3 OPTION BYTES

Each device is available for production in user programmable versions (OTP) as well as in factory coded versions (ROM). OTP devices are shipped to customers with a default content (00h), while ROM factory coded parts contain the code supplied by the customer. This implies that OTP devices have to be configured by the customer using the Option Bytes while the ROM devices are factory-configured.

The two option bytes allow the hardware configuration of the microcontroller to be selected.
The option bytes have no address in the memory map and can be accessed only in programming mode (for example using a standard ST6 programming tool).
In masked ROM devices, the option bytes are fixed in hardware by the ROM code (see Section 11.6.2 "ROM VERSION" on page 98). It is therefore impossible to read the option bytes.

The option bytes can be only programmed once. It is not possible to change the selected options after they have been programmed.

In order to reach the power consumption value indicated in Section 10.4, the option byte must be programmed to its default value. Otherwise, an over-consumption will occur.

MSB OPTION BYTE

Bits 15:10 = **Reserved**, must be always cleared.

Bit 9 = **EXTCNTL** *External STOP MODE control.*
0: EXTCNTL mode not available. STOP mode is not available with the watchdog active.
1: EXTCNTL mode available. STOP mode is available with the watchdog active by setting NMI pin to one.

Bit 8 = **LVD** *Low Voltage Detector* on/off.
This option bit enable or disable the Low Voltage Detector (LVD) feature.
0: Low Voltage Detector disabled
1: Low Voltage Detector enabled

LSB OPTION BYTE

Bit 7 = **PROTECT** *Readout Protection.*
This option bit enables or disables external access to the internal program memory.
0: Program memory not read-out protected
1: Program memory read-out protected

Bit 6 = **OSC** *Oscillator selection*.
This option bit selects the main oscillator type.
0: Quartz crystal, ceramic resonator or external clock
1: RC network

Bit 5 = **Reserved**, must be always cleared.

Bit 4 = **Reserved**, must be always set.

Bit 3 = **NMI PULL** *NMI Pull-Up* on/off.
This option bit enables or disables the internal pull-up on the NMI pin.
0: Pull-up disabled
1: Pull-up enabled

Bit 2 = **TIM PULL** *TIMER Pull-Up* on/off.
This option bit enables or disables the internal pull-up on the TIMER pin.
0: Pull-up disabled
1: Pull-up enabled

Bit 1 = **WDACT** *Hardware or software watchdog.*
This option bit selects the watchdog type.
0: Software (watchdog to be enabled by software)
1: Hardware (watchdog always enabled)

Bit 0 = **OSGEN** *Oscillator Safeguard* on/off.
This option bit enables or disables the oscillator Safeguard (OSG) feature.
0: Oscillator Safeguard disabled
1: Oscillator Safeguard enabled

	MSB OPTION BYTE								LSB OPTION BYTE							
	15							8	7							0
	Reserved						EXT CTL	LVD	PRO-TECT	OSC	Res.	Res.	NMI PULL	TIM PULL	WD ACT	OSG EN
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

4 CENTRAL PROCESSING UNIT

4.1 INTRODUCTION

The CPU Core of ST6 devices is independent of the I/O or Memory configuration. As such, it may be thought of as an independent central processor communicating with on-chip I/O, Memory and Peripherals via internal address, data, and control buses.

4.2 MAIN FEATURES

- 40 basic instructions
- 9 main addressing modes
- Two 8-bit index registers
- Two 8-bit short direct registers
- Low power modes
- Maskable hardware interrupts
- 6-level hardware stack

4.3 CPU REGISTERS

The ST6 Family CPU core features six registers and three pairs of flags available to the programmer. These are described in the following paragraphs.

Accumulator (A). The accumulator is an 8-bit general purpose register used in all arithmetic calculations, logical operations, and data manipulations. The accumulator can be addressed in Data Space as a RAM location at address FFh. Thus the ST6 can manipulate the accumulator just like any other register in Data Space.

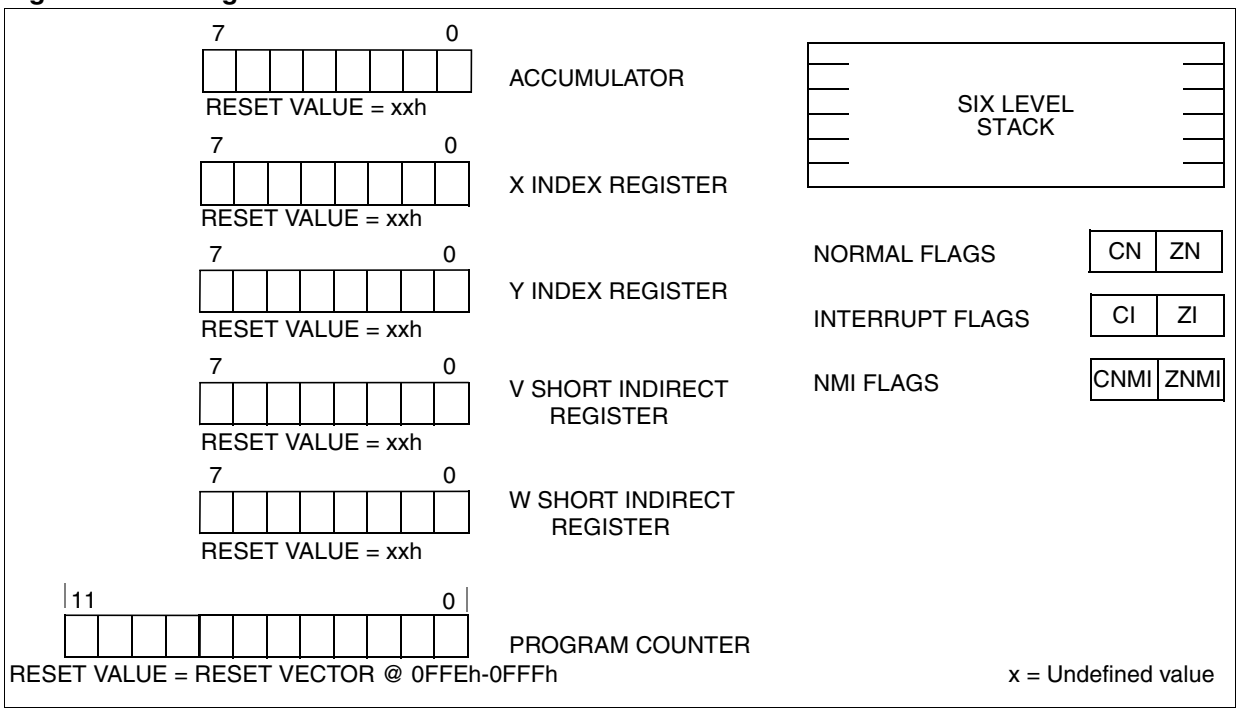
Index Registers (X, Y). These two registers are used in Indirect addressing mode as pointers to memory locations in Data Space. They can also be accessed in Direct, Short Direct, or Bit Direct addressing modes. They are mapped in Data Space at addresses 80h (X) and 81h (Y) and can be accessed like any other memory location.

Short Direct Registers (V, W). These two registers are used in Short Direct addressing mode. This means that the data stored in V or W can be accessed with a one-byte instruction (four CPU cycles). V and W can also be accessed using Direct and Bit Direct addressing modes. They are mapped in Data Space at addresses 82h (V) and 83h (W) and can be accessed like any other memory location.

Note: The X and Y registers can also be used as Short Direct registers in the same way as V and W.

Program Counter (PC). The program counter is a 12-bit register which contains the address of the next instruction to be executed by the core. This ROM location may be an opcode, an operand, or the address of an operand.

Figure 7. CPU Registers



5 CLOCKS, SUPPLY AND RESET

5.1 CLOCK SYSTEM

The main oscillator of the MCU can be driven by any of these clock sources:

– external clock signal

– external AT-cut parallel-resonant crystal

– external ceramic resonator

– external RC network (R_{NET}).

In addition, an on-chip Low Frequency Auxiliary Oscillator (LFAO) is available as a back-up clock system or to reduce power consumption.

An optional Oscillator Safeguard (OSG) filters spikes from the oscillator lines, and switches to the LFAO backup oscillator in the event of main oscillator failure. It also automatically limits the internal clock frequency (f_{INT}) as a function of V_{DD}, in order to guarantee correct operation. These functions are illustrated in Figure 10, and Figure 11.

Table 6 illustrates various possible oscillator configurations using an external crystal or ceramic resonator, an external clock input, an external resistor (R_{NET}), or the lowest cost solution using only the LFAO.

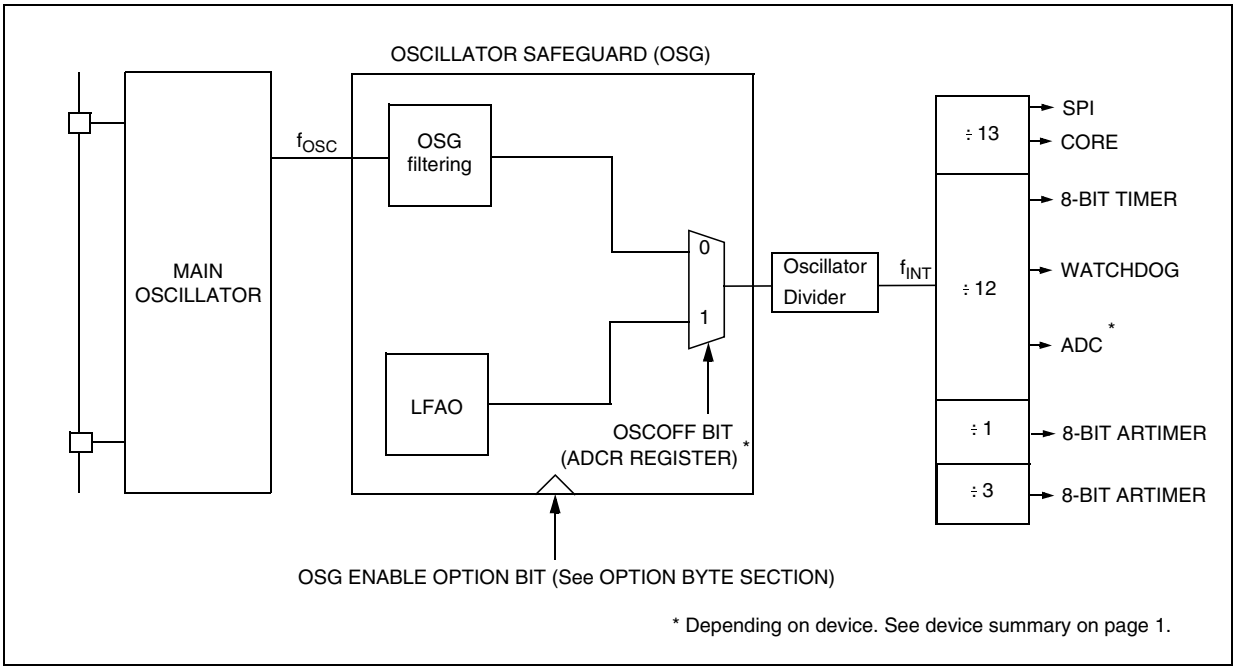
For more details on configuring the clock options, refer to the Option Bytes section of this document.

The internal MCU clock frequency (f_{INT}) is divided by 12 to drive the Timer, the Watchdog timer and the A/D converter, by 13 to drive the CPU core and the SPI and by 1 or 3 to drive the ARTIMER, as shown in Figure 9.

With an 8 MHz oscillator, the fastest CPU cycle is therefore 1.625µs.

A CPU cycle is the smallest unit of time needed to execute any operation (for instance, to increment the Program Counter). An instruction may require two, four, or five CPU cycles for execution.

Figure 9. Clock Circuit Block Diagram



5.2 LOW VOLTAGE DETECTOR (LVD)

The on-chip Low Voltage Detector is enabled by setting a bit in the option bytes (refer to the Option Bytes section of this document).

The LVD allows the device to be used without any external RESET circuitry. In this case, the $\overline{\text{RESET}}$ pin should be left unconnected.

If the LVD is not used, an external circuit is mandatory to ensure correct Power On Reset operation, see figure in the Reset section. For more details, please refer to the application note AN669.

The LVD generates a static Reset when the supply voltage is below a reference value. This means that it secures the power-up as well as the power-down keeping the ST6 in reset.

The V_{IT-} reference value for a voltage drop is lower than the V_{IT+} reference value for power-on in order to avoid a parasitic reset when the MCU starts running and sinks current on the supply (hysteresis).

The LVD Reset circuitry generates a reset when V_{DD} is below:

– V_{IT+} when V_{DD} is rising

– V_{IT-} when V_{DD} is falling

The LVD function is illustrated in Figure 12.

If the LVD is enabled, the MCU can be in only one of two states:

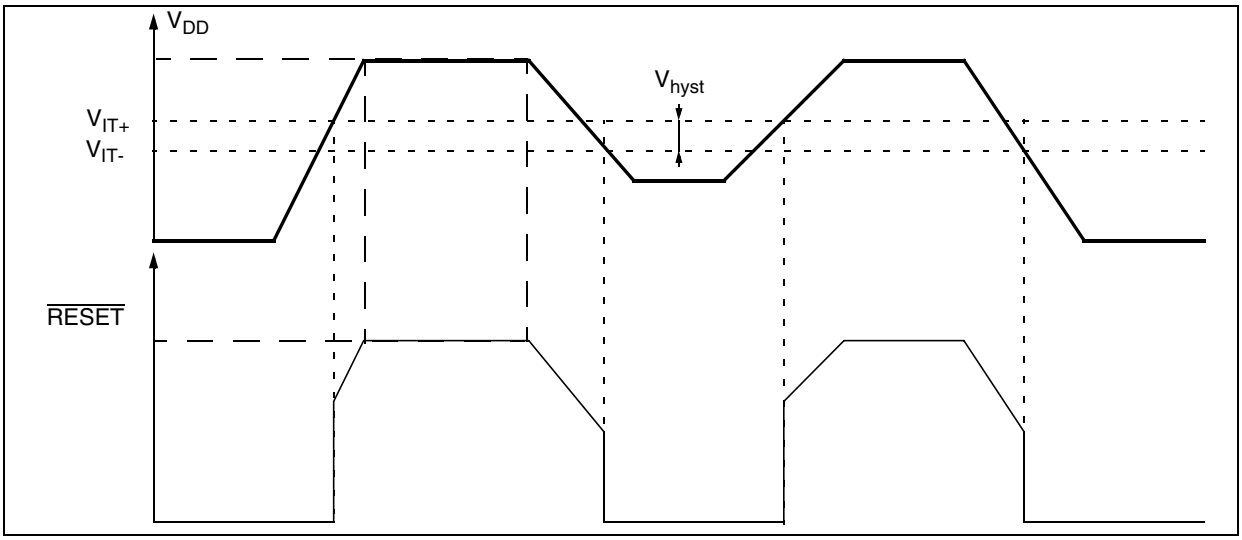
– Over the input threshold voltage, it is running under full software control

– Below the input threshold voltage, it is in static safe reset

In these conditions, secure operation is guaranteed without the need for external reset hardware.

During a Low Voltage Detector Reset, the $\overline{\text{RESET}}$ pin is held low, thus permitting the MCU to reset other devices.

Figure 12. Low Voltage Detector Reset



RESET (Cont'd)

5.3.4 Watchdog Reset

The MCU provides a Watchdog timer function in order to be able to recover from software hang-ups. If the Watchdog register is not refreshed before an end-of-count condition is reached, a Watchdog reset is generated.

After a Watchdog reset, the MCU restarts in the same way as if a Reset was generated by the $\overline{\text{RESET}}$ pin.

Note: When a watchdog reset occurs, the $\overline{\text{RESET}}$ pin is tied low for very short time period, to flag the reset phase. This time is not long enough to reset external circuits.

For more details refer to the Watchdog Timer chapter.

5.3.5 LVD Reset

Two different RESET sequences caused by the internal LVD circuitry can be distinguished:

- Power-On RESET
- Voltage Drop RESET

During an LVD reset, the $\overline{\text{RESET}}$ pin is pulled low when $V_{DD}<V_{IT+}$ (rising edge) or $V_{DD}<V_{IT-}$ (falling edge).

For more details, refer to the LVD chapter.

Caution: Do not externally connect directly the $\overline{\text{RESET}}$ pin to V_{DD}, this may cause damage to the component in case of internal RESET (Watchdog or LVD).

Figure 15. Simple External Reset Circuitry

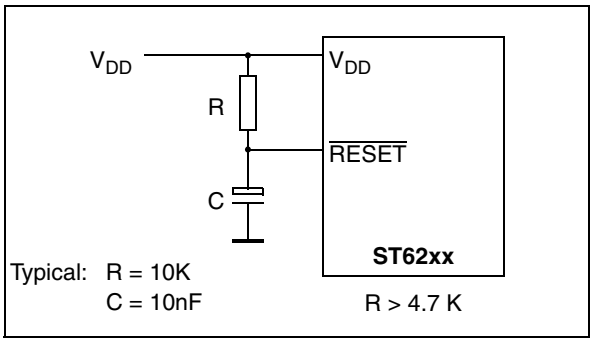
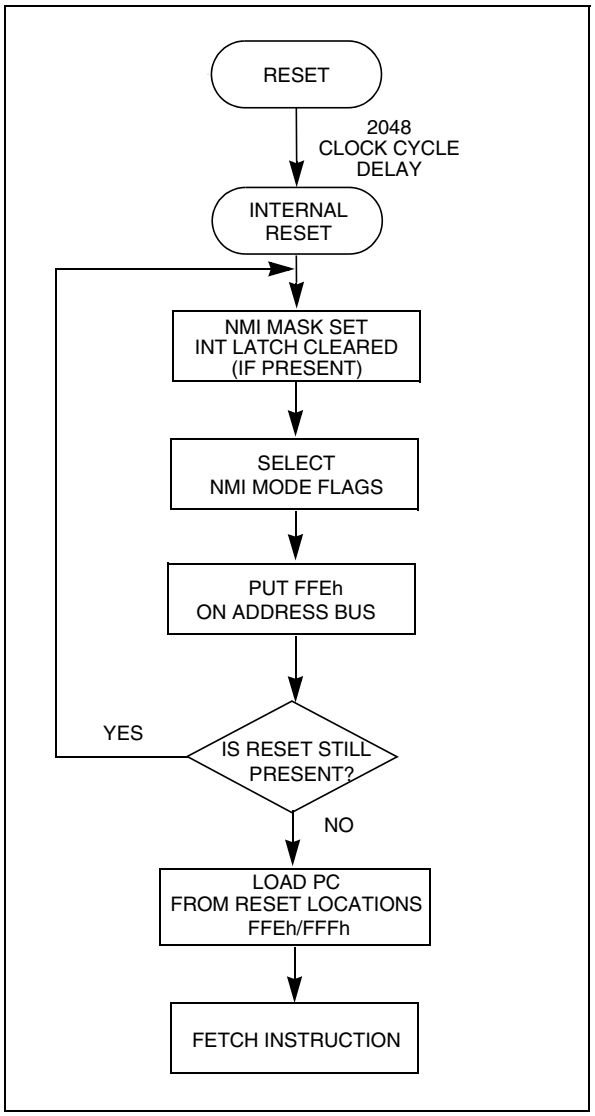


Figure 16. Reset Processing



I/O PORTS (Cont'd)

7.2.5 Instructions NOT to be used to access Port Data registers (SET, RES, INC and DEC)

DO NOT USE READ-MODIFY-WRITE INSTRUCTIONS (SET, RES, INC and DEC) ON PORT DATA REGISTERS IF ANY PIN OF THE PORT IS CONFIGURED IN INPUT MODE.

These instructions make an implicit read and write back of the entire register. In port input mode, however, the data register reads from the input pins directly, and not from the data register latches. Since data register information in input mode is used to set the characteristics of the input pin (interrupt, pull-up, analog input), these may be unintentionally reprogrammed depending on the state of the input pins.

As a general rule, it is better to only use single bit instructions on data registers when the whole (8-bit) port is in output mode. In the case of inputs or of mixed inputs and outputs, it is advisable to keep a copy of the data register in RAM. Single bit instructions may then be used on the RAM copy, after which the whole copy register can be written to the port data register:

```
SET bit, datacopy
LD a, datacopy
LD DRA, a
```

7.2.6 Recommendations

1. Safe I/O State Switching Sequence

Switching the I/O ports from one state to another should be done in a sequence which ensures that no unwanted side effects can occur. The recommended safe transitions are illustrated in Figure 24 The Interrupt Pull-up to Input Analog transition (and vice-vesra) is potentially risky and should be avoided when changing the I/O operating mode.

2. Handling Unused Port Bits

On ports that have less than 8 external pins connected:

– Leave the unbonded pins in reset state and do not change their configuration.

– Do not use instructions that act on a whole port register (INC, DEC, or read operations). Unavailable bits must be masked by software (AND instruction). Thus, when a read operation performed on an incomplete port is followed by a comparison, use a mask.

3. High Impedance Input

On any CMOS device, it is not recommended to connect high impedance on input pins. The choice of these impedance has to be done with respect to the maximum leakage current defined in the datasheet. The risk is to be close or out of specification on the input levels applied to the device.

7.3 LOW POWER MODES

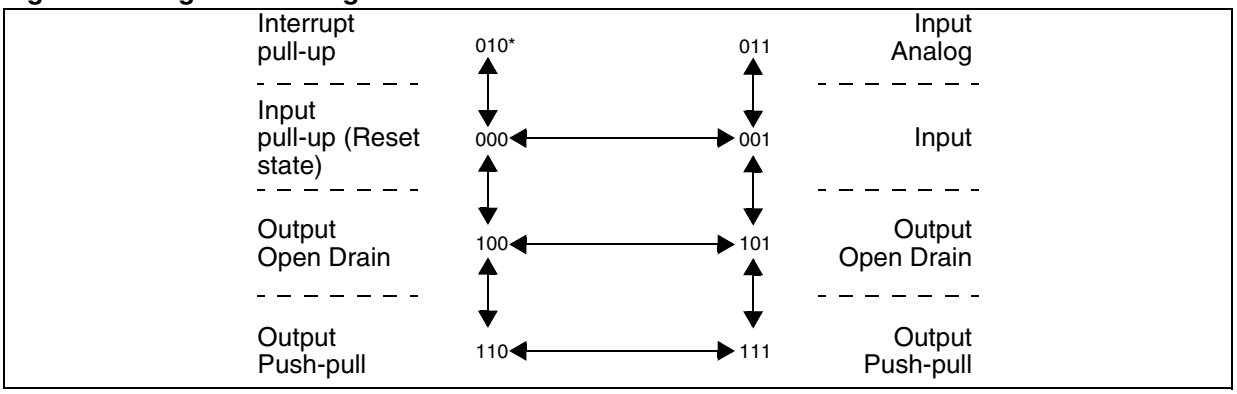
The WAIT and STOP instructions allow the ST62xx to be used in situations where low power consumption is needed. The lowest power consumption is achieved by configuring I/Os in output push-pull low mode.

Mode	Description
WAIT	No effect on I/O ports. External interrupts cause the device to exit from WAIT mode.
STOP	No effect on I/O ports. External interrupts cause the device to exit from STOP mode.

7.4 INTERRUPTS

The external interrupt event generates an interrupt if the corresponding configuration is selected with DDR, DR and OR registers (see Table 9) and the GEN-bit in the IOR register is set.

Figure 24. Diagram showing Safe I/O State Transitions



Note *. xxx = DDR, OR, DR Bits respectively

WATCHDOG TIMER (Cont'd)

8.1.7 Register Description

WATCHDOG REGISTER (WDGR)

Address: 0D8h - Read/Write

Reset Value: 1111 1110 (FEh)

7							0
T0	T1	T2	T3	T4	T5	SR	C

Bits 7:2 = **T[5:0]** *Downcounter bits*
Caution: These bits are reversed and shifted with respect to the physical counter: bit-7 (T0) is the LSB of the Watchdog downcounter and bit-2 (T5) is the MSB.

Bit 1 = **SR**: *Software Reset bit*
Software can generate a reset by clearing this bit while the C bit is set. When C = 0 (Watchdog deactivated) the SR bit is the MSB of the 7-bit timer.
0: Generate (write)

1: No software reset generated, MSB of 7-bit timer

Bit 0 = **C** *Watchdog Control bit*.
If the hardware option is selected (WDACT bit in Option byte), this bit is forced high and cannot be changed by the user (the Watchdog is always active). When the software option is selected (WDACT bit in Option byte), the Watchdog function is activated by setting the C bit, and cannot then be deactivated (except by resetting the MCU).

When C is kept cleared the counter can be used as a 7-bit timer.
0: Watchdog deactivated
1: Watchdog activated

8-BIT TIMER (Cont'd)

8.2.4 Functional Description

There are three operating modes, which are selected by the TOUT and DOUT bits (see TSCR register). These three modes correspond to the two clocks which can be connected to the 7-bit prescaler ($f_{INT} \div 12$ or TIMER pin signal), and to the output mode.

The settings for the different operating modes are summarized Table 13.

Table 13. Timer Operating Modes

TOUT	DOUT	Timer Function	Application
0	0	Event Counter (input)	External counter clock source
0	1	Gated input (input)	External Pulse length measurement
1	0	Output "0" (output)	Output signal generation
1	1	Output "1" (output)	

8.2.4.1 Gated Mode

(TOUT = "0", DOUT = "1")

In this mode, the prescaler is decremented by the Timer clock input, but only when the signal on the TIMER pin is held high ($f_{INT}/12$ gated by TIMER pin). See Figure 28 and Figure 29.

This mode is selected by clearing the TOUT bit in the TSCR register (i.e. as input) and setting the DOUT bit.

Note: In this mode, if the TIMER pin is multiplexed, the corresponding port control bits have to be set in input with pull-up configuration through the DDR, OR and DR registers. For more details, please refer to the I/O Ports section.

Figure 28. f_{TIMER} Clock in Gated Mode

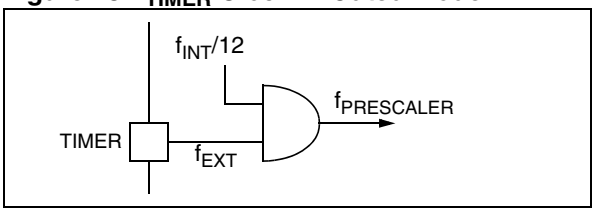
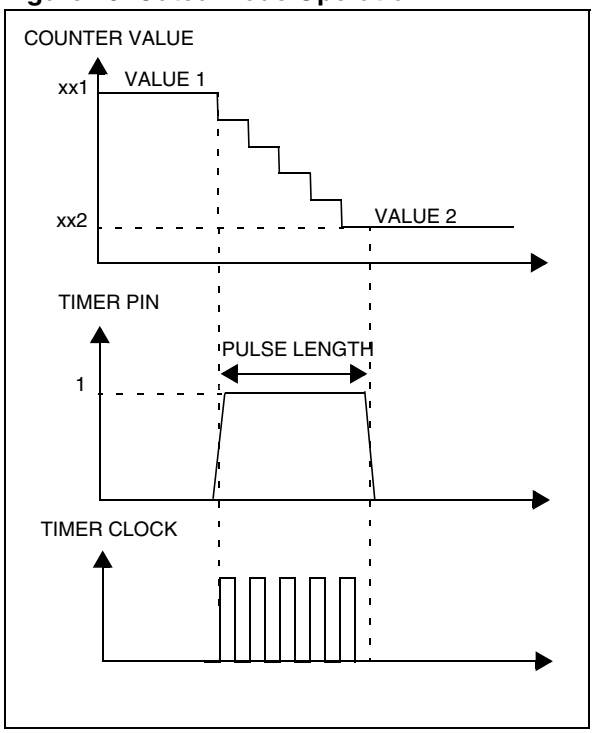


Figure 29. Gated Mode Operation



9.3 INSTRUCTION SET

The ST6 offers a set of 40 basic instructions which, when combined with nine addressing modes, yield 244 usable opcodes. They can be divided into six different types: load/store, arithmetic/logic, conditional branch, control instructions, jump/call, and bit manipulation. The following paragraphs describe the different types.

All the instructions belonging to a given type are presented in individual tables.

Load & Store. These instructions use one, two or three bytes depending on the addressing mode. For LOAD, one operand is the Accumulator and the other operand is obtained from data memory using one of the addressing modes.

For Load Immediate, one operand can be any of the 256 data space bytes while the other is always immediate data.

Table 17. Load & Store Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
LD A, X	Short Direct	1	4	Δ	*
LD A, Y	Short Direct	1	4	Δ	*
LD A, V	Short Direct	1	4	Δ	*
LD A, W	Short Direct	1	4	Δ	*
LD X, A	Short Direct	1	4	Δ	*
LD Y, A	Short Direct	1	4	Δ	*
LD V, A	Short Direct	1	4	Δ	*
LD W, A	Short Direct	1	4	Δ	*
LD A, rr	Direct	2	4	Δ	*
LD rr, A	Direct	2	4	Δ	*
LD A, (X)	Indirect	1	4	Δ	*
LD A, (Y)	Indirect	1	4	Δ	*
LD (X), A	Indirect	1	4	Δ	*
LD (Y), A	Indirect	1	4	Δ	*
LDI A, #N	Immediate	2	4	Δ	*
LDI rr, #N	Immediate	3	4	*	*

Legend:

X, Y Index Registers,
V, W Short Direct Registers
Immediate data (stored in ROM memory)
rr Data space register
Δ Affected
* Not Affected

INSTRUCTION SET (Cont'd)

Arithmetic and Logic. These instructions are used to perform arithmetic calculations and logic operations. In AND, ADD, CP, SUB instructions one operand is always the accumulator while, depending on the addressing mode, the other can be either a data space memory location or an immediate value. In CLR, DEC, INC instructions the operand can be any of the 256 data space addresses. In COM, RLC, SLA the operand is always the accumulator.

Table 18. Arithmetic & Logic Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
ADD A, (X)	Indirect	1	4	Δ	Δ
ADD A, (Y)	Indirect	1	4	Δ	Δ
ADD A, rr	Direct	2	4	Δ	Δ
ADDI A, #N	Immediate	2	4	Δ	Δ
AND A, (X)	Indirect	1	4	Δ	Δ
AND A, (Y)	Indirect	1	4	Δ	Δ
AND A, rr	Direct	2	4	Δ	Δ
ANDI A, #N	Immediate	2	4	Δ	Δ
CLR A	Short Direct	2	4	Δ	Δ
CLR r	Direct	3	4	*	*
COM A	Inherent	1	4	Δ	Δ
CP A, (X)	Indirect	1	4	Δ	Δ
CP A, (Y)	Indirect	1	4	Δ	Δ
CP A, rr	Direct	2	4	Δ	Δ
CPI A, #N	Immediate	2	4	Δ	Δ
DEC X	Short Direct	1	4	Δ	*
DEC Y	Short Direct	1	4	Δ	*
DEC V	Short Direct	1	4	Δ	*
DEC W	Short Direct	1	4	Δ	*
DEC A	Direct	2	4	Δ	*
DEC rr	Direct	2	4	Δ	*
DEC (X)	Indirect	1	4	Δ	*
DEC (Y)	Indirect	1	4	Δ	*
INC X	Short Direct	1	4	Δ	*
INC Y	Short Direct	1	4	Δ	*
INC V	Short Direct	1	4	Δ	*
INC W	Short Direct	1	4	Δ	*
INC A	Direct	2	4	Δ	*
INC rr	Direct	2	4	Δ	*
INC (X)	Indirect	1	4	Δ	*
INC (Y)	Indirect	1	4	Δ	*
RLC A	Inherent	1	4	Δ	Δ
SLA A	Inherent	2	4	Δ	Δ
SUB A, (X)	Indirect	1	4	Δ	Δ
SUB A, (Y)	Indirect	1	4	Δ	Δ
SUB A, rr	Direct	2	4	Δ	Δ
SUBI A, #N	Immediate	2	4	Δ	Δ

Notes:
X,Y Index Registers
V, W Short Direct Registers
Δ Affected
Immediate data (stored in ROM memory)
* Not Affected
rr Data space register

Opcode Map Summary (Continued)

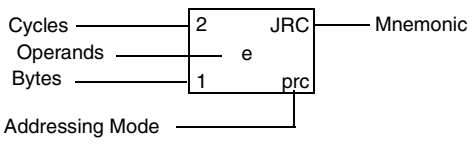
LOW / HI	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	LOW / HI
0 **0000**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b0,rr 2 b.d	2 JRZ e 1 pcr	4 LDI rr,nn 3 imm	2 JRC e 1 prc	4 LD a,(y) 1 ind	**0** **0000**
1 **0001**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b0,rr 2 b.d	2 JRZ e 1 pcr	4 DEC x 1 sd	2 JRC e 1 prc	4 LD a,rr 2 dir	**1** **0001**
2 **0010**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b4,rr 2 b.d	2 JRZ e 1 pcr	4 COM a	2 JRC e 1 prc	4 CP a,(y) 1 ind	**2** **0010**
3 **0011**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b4,rr 2 b.d	2 JRZ e 1 pcr	4 LD x,a 1 sd	2 JRC e 1 prc	4 CP a,rr 2 dir	**3** **0011**
4 **0100**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b2,rr 2 b.d	2 JRZ e 1 pcr	2 RETI 1 inh	2 JRC e 1 prc	4 ADD a,(y) 1 ind	**4** **0100**
5 **0101**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b2,rr 2 b.d	2 JRZ e 1 pcr	4 DEC y 1 sd	2 JRC e 1 prc	4 ADD a,rr 2 dir	**5** **0101**
6 **0110**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b6,rr 2 b.d	2 JRZ e 1 pcr	2 STOP 1 inh	2 JRC e 1 prc	4 INC (y) 1 ind	**6** **0110**
7 **0111**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b6,rr 2 b.d	2 JRZ e 1 pcr	4 LD y,a 1 sd	2 JRC e 1 prc	4 INC rr 2 dir	**7** **0111**
8 **1000**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b1,rr 2 b.d	2 JRZ e 1 pcr	# 	2 JRC e 1 prc	4 LD (y),a 1 ind	**8** **1000**
9 **1001**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b1,rr 2 b.d	2 JRZ e 1 pcr	4 DEC v 1 sd	2 JRC e 1 prc	4 LD rr,a 2 dir	**9** **1001**
A **1010**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b5,rr 2 b.d	2 JRZ e 1 pcr	4 RCL a 1 inh	2 JRC e 1 prc	4 AND a,(y) 1 ind	**A** **1010**
B **1011**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b5,rr 2 b.d	2 JRZ e 1 pcr	4 LD v,a 1 sd	2 JRC e 1 prc	4 AND a,rr 2 dir	**B** **1011**
C **1100**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b3,rr 2 b.d	2 JRZ e 1 pcr	2 RET 1 inh	2 JRC e 1 prc	4 SUB a,(y) 1 ind	**C** **1100**
D **1101**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b3,rr 2 b.d	2 JRZ e 1 pcr	4 DEC w 1 sd	2 JRC e 1 prc	4 SUB a,rr 2 dir	**D** **1101**
E **1110**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b7,rr 2 b.d	2 JRZ e 1 pcr	2 WAIT 1 inh	2 JRC e 1 prc	4 DEC (y) 1 ind	**E** **1110**
F **1111**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b7,rr 2 b.d	2 JRZ e 1 pcr	4 LD w,a 1 sd	2 JRC e 1 prc	4 DEC rr 2 dir	**F** **1111**

Abbreviations for Addressing Modes:

dir	Direct
sd	Short Direct
imm	Immediate
inh	Inherent
ext	Extended
b.d	Bit Direct
bt	Bit Test
pcr	Program Counter Relative
ind	Indirect

Legend:

#	Indicates Illegal Instructions
e	5-bit Displacement
b	3-bit Address
rr	1-byte Data space address
nn	1-byte immediate data
abc	12-bit address
ee	8-bit Displacement



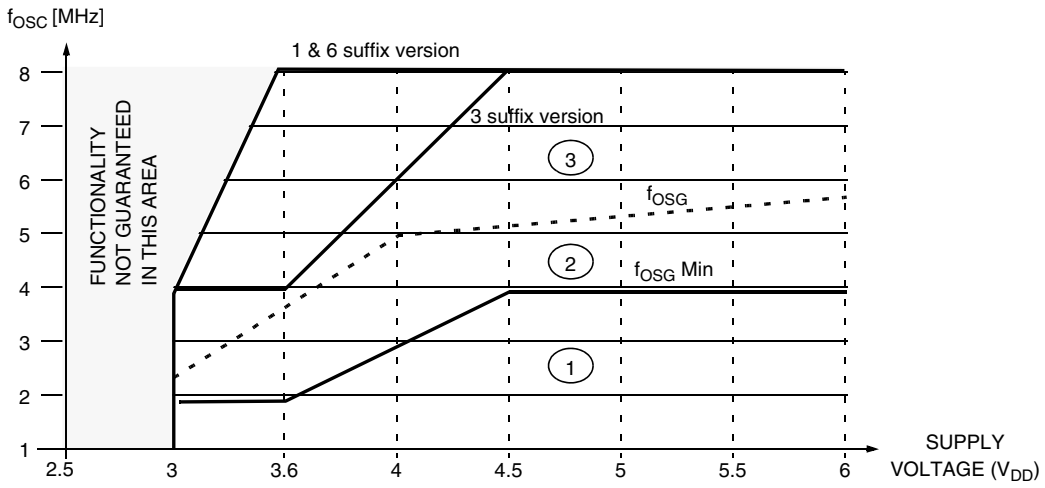
10.3 OPERATING CONDITIONS

10.3.1 General Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage	see Figure 38	3.0	6	V
f_{OSC}	Oscillator frequency	V_{DD}=3.0V, 1 & 6 Suffix	0 [1]	4	MHz
		V_{DD}=3.0V, 3 Suffix	0 [1]	4	
		V_{DD}=3.6V, 1 & 6Suffix	0 [1]	8	
		V_{DD}=3.6V, 3 Suffix	0 [1]	4	
V_{DD}	Operating Supply Voltage	f_{OSC}=4MHz, 1 & 6 Suffix	3.0	6.0	V
		f_{OSC}=4MHz, 3 Suffix	3.0	6.0	
		f_{OSC}=8MHz, 1 & 6 Suffix	3.6	6.0	
		f_{OSC}=8MHz, 3 Suffix	4.5	6.0	
T_A	Ambient temperature range	1 Suffix Version	0	70	°C
		6 Suffix Version	-40	85	
		3 Suffix Version	-40	125	

Notes:
1. An oscillator frequency above 1.2MHz is recommended for reliable A/D results.
2. Operating conditions with T_A=-40 to +125°C.

Figure 38. f_{OSC} Maximum Operating Frequency Versus V_{DD} Supply Voltage for OTP & ROM devices



1. In this area, operation is guaranteed at the quartz crystal frequency.
2. When the OSG is disabled, operation in this area is guaranteed at the crystal frequency. When the OSG is enabled, operation in this area is guaranteed at a frequency of at least f_{OSG} Min.
3. When the OSG is disabled, operation in this area is guaranteed at the quartz crystal frequency. When the OSG is enabled, access to this area is prevented. The internal frequency is kept at f_{OSG}.

OPERATING CONDITIONS (Cont'd)

10.3.2 Operating Conditions with Low Voltage Detector (LVD)

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{IT+}	Reset release threshold (V_{DD} rise)		3.9	4.1	4.3	V
V_{IT-}	Reset generation threshold (V_{DD} fall)		3.6	3.8	4	
V_{hys}	LVD voltage threshold hysteresis	V_{IT+}-V_{IT-}	50	300	700	mV
Vt_{POR}	V_{DD} rise time rate [2]					mV/s
$t_{g(VDD)}$	Filtered glitch delay on V_{DD} [3]	Not detected by the LVD		30		ns

Notes:

1. LVD typical data are based on T_A=25°C. They are given only as design guidelines and are not tested.
2. The minimum V_{DD} rise time rate is needed to insure a correct device power-on and LVD reset. Not tested in production.
3. Data based on characterization results, not tested in production.

Figure 39. LVD Threshold Versus V_{DD} and f_{OSC} [3]

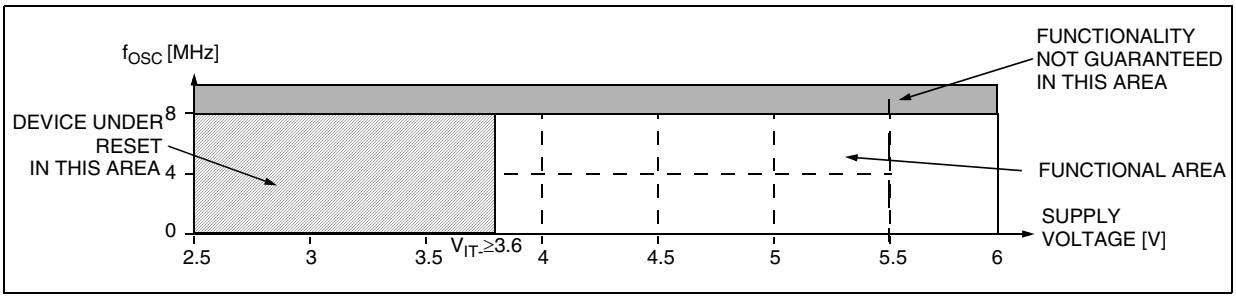


Figure 40. Typical LVD Thresholds Versus Temperature for OTP devices

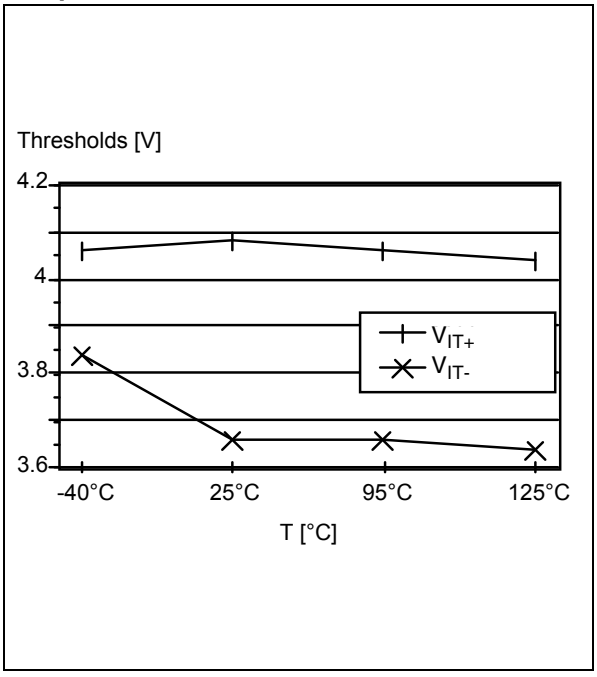
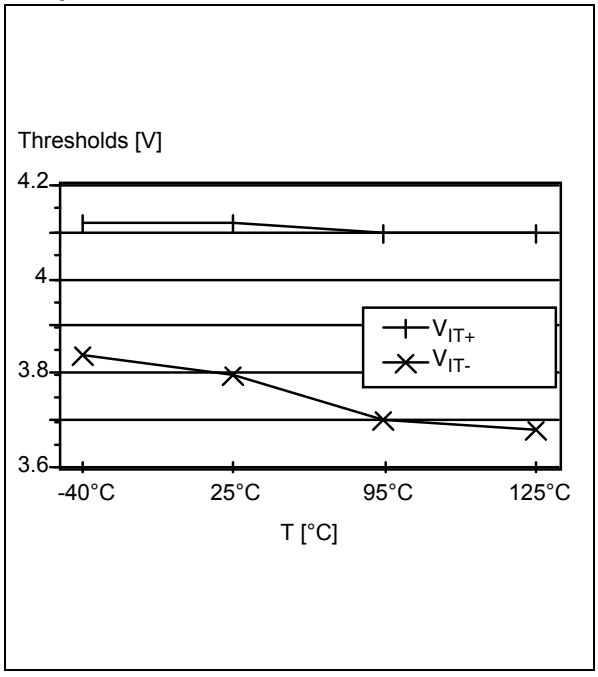


Figure 41. Typical LVD thresholds vs. Temperature for ROM devices



10.4 SUPPLY CURRENT CHARACTERISTICS

The following current consumption specified for the ST6 functional operating modes over temperature range does not take into account the clock source current consumption. To get the total device consumption, the two current values must be added (except for STOP mode for which the clock is stopped).

10.4.1 RUN Modes

Symbol	Parameter	Conditions		Typ [1]	Max [2]	Unit
I_{DD}	Supply current in RUN mode [3] (see Figure 42 & Figure 43)	$4.5V \le V_{DD} \le 6.0V$	f_{OSC}=32kHz f_{OSC}=1MHz f_{OSC}=2MHz f_{OSC}=4MHz f_{OSC}=8MHz	0.5 1.3 1.6 2.2 3.3	0.7 1.7 2.4 3.3 4.8	mA
	Supply current in RUN mode [3] (see Figure 42 & Figure 43)	$3V \le V_{DD} \le 3.6V$	f_{OSC}=32kHz f_{OSC}=1MHz f_{OSC}=2MHz f_{OSC}=4MHz f_{OSC}=8MHz	0.3 0.6 0.9 1.0 1.8	0.4 0.8 1.2 1.5 2.3	

Notes:

1. Typical data are based on T_A=25°C, V_{DD}=5V (4.5V≤V_{DD}≤6.0V range) and V_{DD}=3.3V (3V≤V_{DD}≤3.6V range).
2. Data based on characterization results, tested in production at V_{DD} max. and f_{OSC} max.
3. CPU running with memory access, all I/O pins in input with pull-up mode (no load), all peripherals in reset state; clock input (OSC_{IN}) driven by external square wave, OSG and LVD disabled, option bytes not programmed.

Figure 42. Typical I_{DD} in RUN vs. f_{CPU}

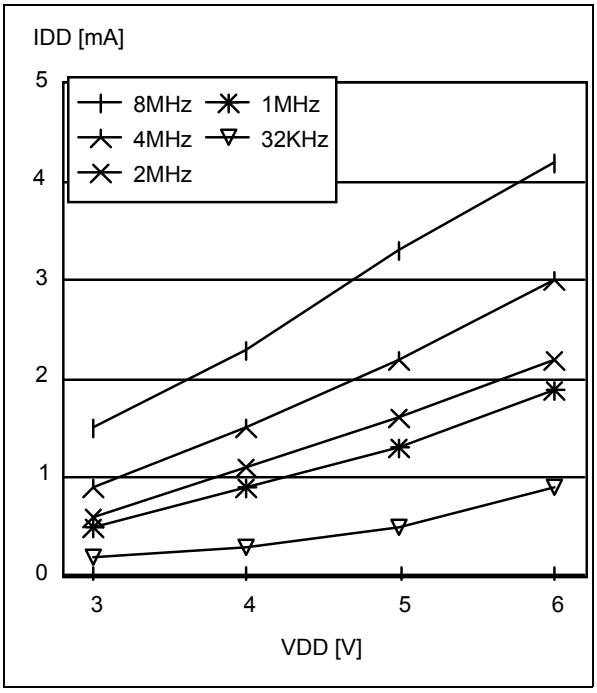
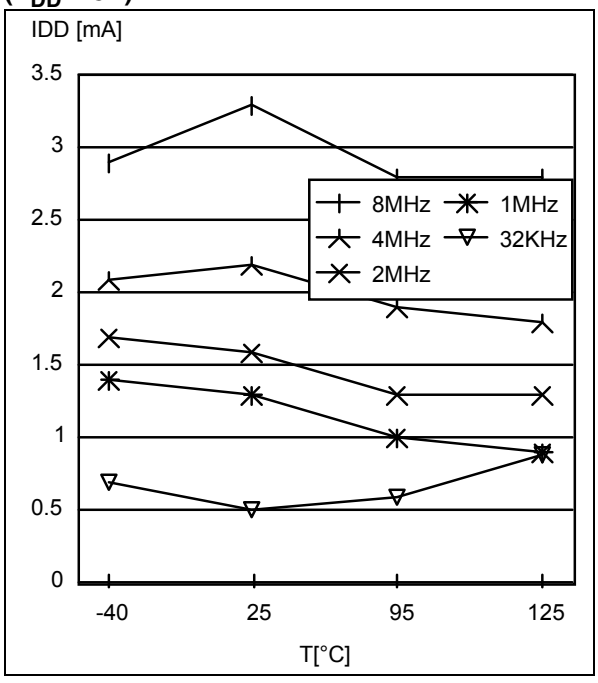


Figure 43. Typical I_{DD} in RUN vs. Temperature (V_{DD} = 5V)



SUPPLY CURRENT CHARACTERISTICS (Cont'd)

10.4.2 WAIT Modes

Symbol	Parameter	Conditions			Typ [1]	Max [2]	Unit
I_{DD}	Supply current in WAIT mode [3] Option bytes not programmed (see Figure 44)	$4.5V \le V_{DD} \le 6.0V$	OTP devices	f_{OSC}=32kHz	330	550	µA
				f_{OSC}=1MHz	350	600	
				f_{OSC}=2MHz	370	650	
				f_{OSC}=4MHz	410	700	
				f_{OSC}=8MHz	480	800	
	Supply current in WAIT mode [3] Option bytes programmed to 00H (see Figure 45)			f_{OSC}=32kHz	18	60	
				f_{OSC}=1MHz	26	80	
				f_{OSC}=2MHz	41	120	
				f_{OSC}=4MHz	57	180	
				f_{OSC}=8MHz	70	200	
	Supply current in WAIT mode [3] (see Figure 46)		ROM devices	f_{OSC}=32kHz	190	300	
				f_{OSC}=1MHz	210	350	
				f_{OSC}=2MHz	240	400	
				f_{OSC}=4MHz	280	500	
				f_{OSC}=8MHz	350	600	
	Supply current in WAIT mode [3] Option bytes not programmed (see Figure 44)	$3V \le V_{DD} \le 3.6V$	OTP devices	f_{OSC}=32kHz	80	120	
				f_{OSC}=1MHz	90	140	
				f_{OSC}=2MHz	100	150	
				f_{OSC}=4MHz	120	200	
				f_{OSC}=8MHz	150	250	
	Supply current in WAIT mode [3] Option bytes programmed to 00H (see Figure 45)			f_{OSC}=32kHz	5	30	
				f_{OSC}=1MHz	8	40	
				f_{OSC}=2MHz	16	50	
				f_{OSC}=4MHz	18	60	
				f_{OSC}=8MHz	20	100	
	Supply current in WAIT mode [3] Option bytes not programmed (see Figure 46)		ROM devices	f_{OSC}=32kHz	60	100	
				f_{OSC}=1MHz	65	110	
				f_{OSC}=2MHz	80	120	
				f_{OSC}=4MHz	100	150	
				f_{OSC}=8MHz	130	210	

Notes:

1. Typical data are based on T_A=25°C, V_{DD}=5V ($4.5V \le V_{DD} \le 6.0V$ range) and V_{DD}=3.3V ($3V \le V_{DD} \le 3.6V$ range).
2. Data based on characterization results, tested in production at V_{DD} max. and f_{OSC} max.
3. All I/O pins in input with pull-up mode (no load), all peripherals in reset state; clock input (OSC_{IN}) driven by external square wave, OSG and LVD disabled.

CLOCK AND TIMING CHARACTERISTICS (Cont'd)

10.5.3 Crystal and Ceramic Resonator Oscillators

The ST6 internal clock can be supplied with several different Crystal/Ceramic resonator oscillators. Only parallel resonant crystals can be used. All the information given in this paragraph are based on characterization results with specified typical external components. Refer to the crystal/ceramic resonator manufacturer for more details (frequency, package, accuracy...).

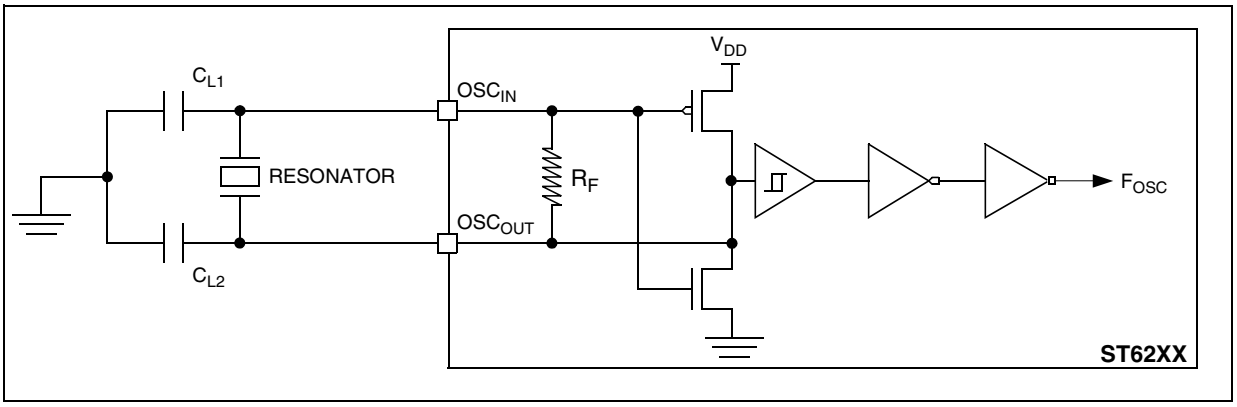
Symbol	Parameter	Conditions	Typ	Unit
R_F	Feedback resistor		3	MΩ
C_{L1} C_{L2}	Recommended load capacitances versus equivalent crystal or ceramic resonator frequency	f_{OSC}=32 kHz, f_{OSC}=1 MHz f_{OSC}=2 MHz f_{OSC}=4 MHz f_{OSC}=8 MHz	120 47 33 33 22	pF

Oscillator	Typical Crystal or Ceramic Resonators				C_{L1} [pF]	C_{L2} [pF]	$t_{SU(osc)}$ [ms] 1)
	Reference		Freq.	Characteristic 1)			
Ceramic	MURATA	CSB455E	455KHz	Δf_{OSC}=[±0.5KHz$_{tolerance}$,±0.3%$_{\Delta Ta}$,±0.5%$_{aging}$]	220	220	
		CSB1000J	1MHz	Δf_{OSC}=[±0.5KHz$_{tolerance}$,±0.3%$_{\Delta Ta}$,±0.5%$_{aging}$]	100	100	
		CSTCC2.00MG0H6	2MHz	Δf_{OSC}=[±0.5%$_{tolerance}$,±0.5%$_{\Delta Ta}$,±0.3%$_{aging}$]	47	47	
		CSTCC4.00MG0H6	4MHz	Δf_{OSC}=[±0.5%$_{tolerance}$,±0.3%$_{\Delta Ta}$,±0.3%$_{aging}$]	47	47	
		CSTCC8.00MG	8MHz	Δf_{OSC}=[±0.5%$_{tolerance}$,±0.3%$_{\Delta Ta}$,±0.3%$_{aging}$]	15	15	

Notes:

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. $t_{SU(OSC)}$ is the typical oscillator start-up time measured between V_{DD}=2.8V and the fetch of the first instruction (with a quick V_{DD} ramp-up from 0 to 5V (<50µs).
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value. Refer to crystal/ceramic resonator manufacturer for more details.

Figure 50. Typical Application with a Crystal or Ceramic Resonator



EMC CHARACTERISTICS (Cont'd)

10.7.2 Absolute Electrical Sensitivity

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the AN1181 application note.

10.7.2.1 Electro-Static Discharge (ESD)

Electro-Static Discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends of the number of supply pins of the device (3 parts*(n+1) supply pin). Two models are usually simulated: Human Body Model and Machine Model. This test conforms to the JESD22-A114A/A115A standard. See Figure 57 and the following test sequences.

Human Body Model Test Sequence

– C_L is loaded through S1 by the HV pulse generator.
– S1 switches position from generator to R.
– A discharge from C_L through R (body resistance) to the ST6 occurs.
– S2 must be closed 10 to 100ms after the pulse delivery period to ensure the ST6 is not left in charge state. S2 must be opened at least 10ms prior to the delivery of the next pulse.

Machine Model Test Sequence

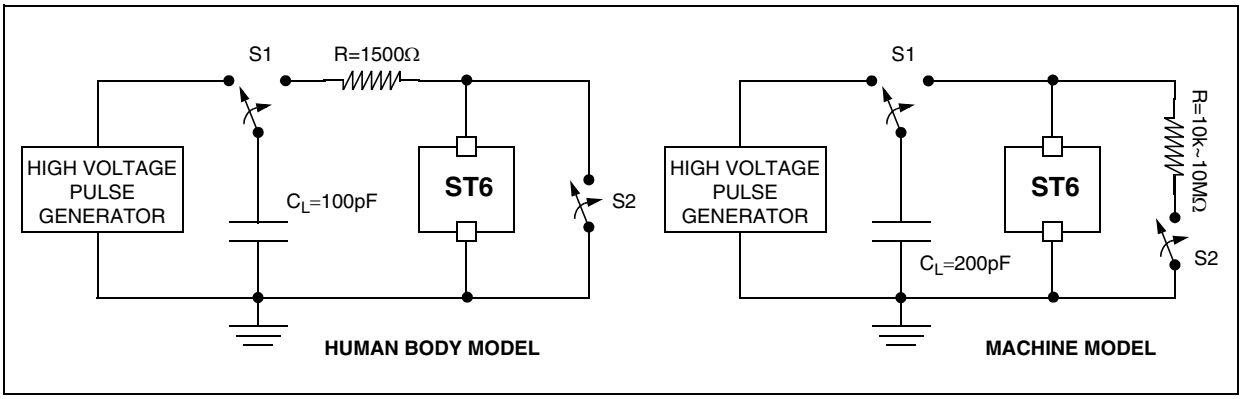
– C_L is loaded through S1 by the HV pulse generator.
– S1 switches position from generator to ST6.
– A discharge from C_L to the ST6 occurs.
– S2 must be closed 10 to 100ms after the pulse delivery period to ensure the ST6 is not left in charge state. S2 must be opened at least 10ms prior to the delivery of the next pulse.
– R (machine resistance), in series with S2, ensures a slow discharge of the ST6.

Absolute Maximum Ratings

Symbol	Ratings	Conditions	Maximum value [1]	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25°C	2000	V
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)	T_A=+25°C	200	

Notes:
1. Data based on characterization results, not tested in production.

Figure 57. Typical Equivalent ESD Circuits



I/O PORT PIN CHARACTERISTICS (Cont'd)

Figure 68. Typical V_{OH} vs V_{DD}