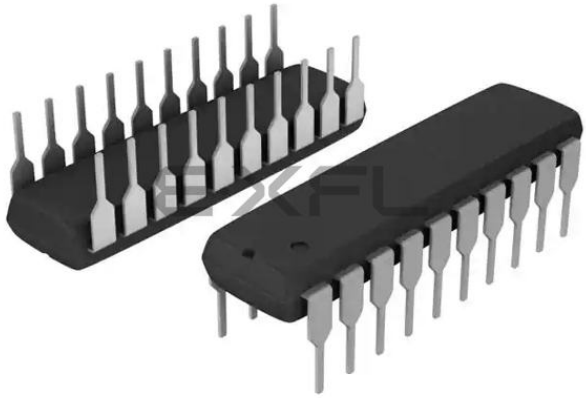


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST6
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	12
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st62t20cb6

Table of Contents

1 INTRODUCTION

The ST6208C, 09C, 10C and 20C devices are low cost members of the ST62xx 8-bit HCMOS family of microcontrollers, which is targeted at low to medium complexity applications. All ST62xx devices are based on a building block approach: a common core is surrounded by a number of on-chip peripherals.

The ST62E20C is the erasable EPROM version of the ST62T08C, T09C, T10C and T20C devices, which may be used during the development phase for the ST62T08C, T09C, T10C and T20C target devices, as well as the respective ST6208C, 09C, 10C and 20C ROM devices.

OTP and EPROM devices are functionally identical. OTP devices offer all the advantages of user programmability at low cost, which make them the ideal choice in a wide range of applications where frequent code changes, multiple code versions or last minute programmability are required.

The ROM based versions offer the same functionality, selecting the options defined in the programmable option bytes of the OTP/EPROM versions in the ROM option list (See Section 11.6 on page 96).

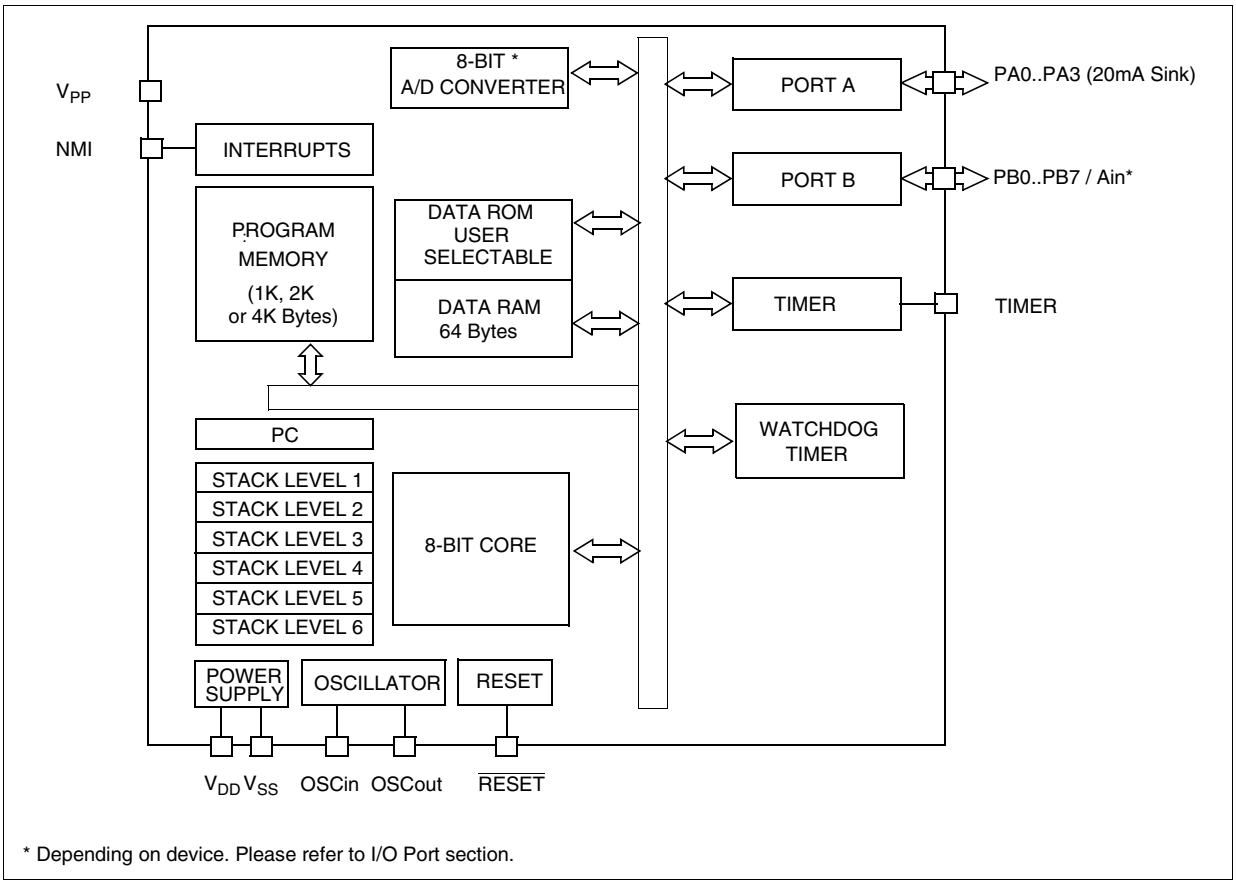
The ST62P08C/P09C/P10C/P20C are the **F**actory **A**dvanced **S**ervice **T**echnique ROM (FASTROM) versions of ST62T08C, T09C, T10C and T20C OTP devices.

They offer the same functionality as OTP devices, but they do not have to be programmed by the customer (See Section 11 on page 90).

These compact low-cost devices feature a Timer comprising an 8-bit counter with a 7-bit programmable prescaler, an 8-bit A/D Converter with up to 8 analog inputs (depending on device) and a Digital Watchdog timer, making them well suited for a wide range of automotive, appliance and industrial applications.

For easy reference, all parametric data are located in Section 11 on page 90.

Figure 1. Block Diagram



* Depending on device. Please refer to I/O Port section.

MEMORY MAP (Cont'd)

Table 2. Hardware Register Map

Address	Block	Register Label	Register Name	Reset Status	Remarks
080h to 083h	CPU	X,Y,V,W	X,Y index registers V,W short direct registers	xxh	R/W
0C0h 0C1h	I/O Ports	DRA [1) 2) 3)] DRB [1) 2) 3)]	Port A Data Register Port B Data Register	00h 00h	R/W R/W
0C2h 0C3h	Reserved (2 Bytes)				
0C4h 0C5h	I/O Ports	DDRA [2)] DDRB [2)]	Port A Direction Register Port B Direction Register	00h 00h	R/W R/W
0C6h 0C7h	Reserved (2 Bytes)				
0C8h	CPU	IOR	Interrupt Option Register	xxh	Write-only
0C9h	ROM	DRWR	Data ROM Window register	xxh	Write-only
0CAh 0CBh	Reserved (2 Bytes)				
0CCh 0CDh	I/O Ports	ORA [2)] ORB [2)]	Port A Option Register Port B Option Register	00h 00h	R/W R/W
0CEh 0CFh	Reserved (2 bytes)				
0D0h 0D1h	ADC [4)]	ADR ADCR	A/D Converter Data Register A/D Converter Control Register	xxh 40h	Read-only Ro/Wo
0D2h 0D3h 0D4h	Timer1	PSCR TCR TSCR	Timer 1 Prescaler Register Timer 1 Downcounter Register Timer 1 Status Control Register	7Fh 0FFh 00h	R/W R/W R/W
0D5h to 0D7h	Reserved (3 Bytes)				
0D8h	Watchdog Timer	WDGR	Watchdog Register	0FEh	R/W
0D9h to 0FEh	Reserved (38 Bytes)				
0FFh	CPU	A	Accumulator	xxh	R/W

Legend:
x = undefined, R/W = Read/Write, Ro = Read-only Bit(s) in the register, Wo = Write-only Bit(s) in the register.

Notes:
1. The contents of the I/O port DR registers are readable only in output configuration. In input configuration, the values of the I/O pins are returned instead of the DR register contents.
2. The bits associated with unavailable pins must always be kept at their reset value.
3. Do not use single-bit instructions (SET, RES...) on Port Data Registers if any pin of the port is configured in input mode (refer to Section 7 "I/O PORTS" on page 37 for more details)
4. Depending on device. See device summary on page 1.

MEMORY MAP (Cont'd)

3.1.6.2 Data ROM Window memory addressing

In cases where some data (look-up tables for example) are stored in program memory, reading these data requires the use of the Data ROM window mechanism. To do this:

1. The DRWR register has to be loaded with the 64-byte block number where the data are located (in program memory). This number also gives the start address of the block.

2. Then, the offset address of the byte in the Data ROM Window (corresponding to the offset in the 64-byte block in program memory) has to be loaded in a register (A, X,...).

When the above two steps are completed, the data can be read.

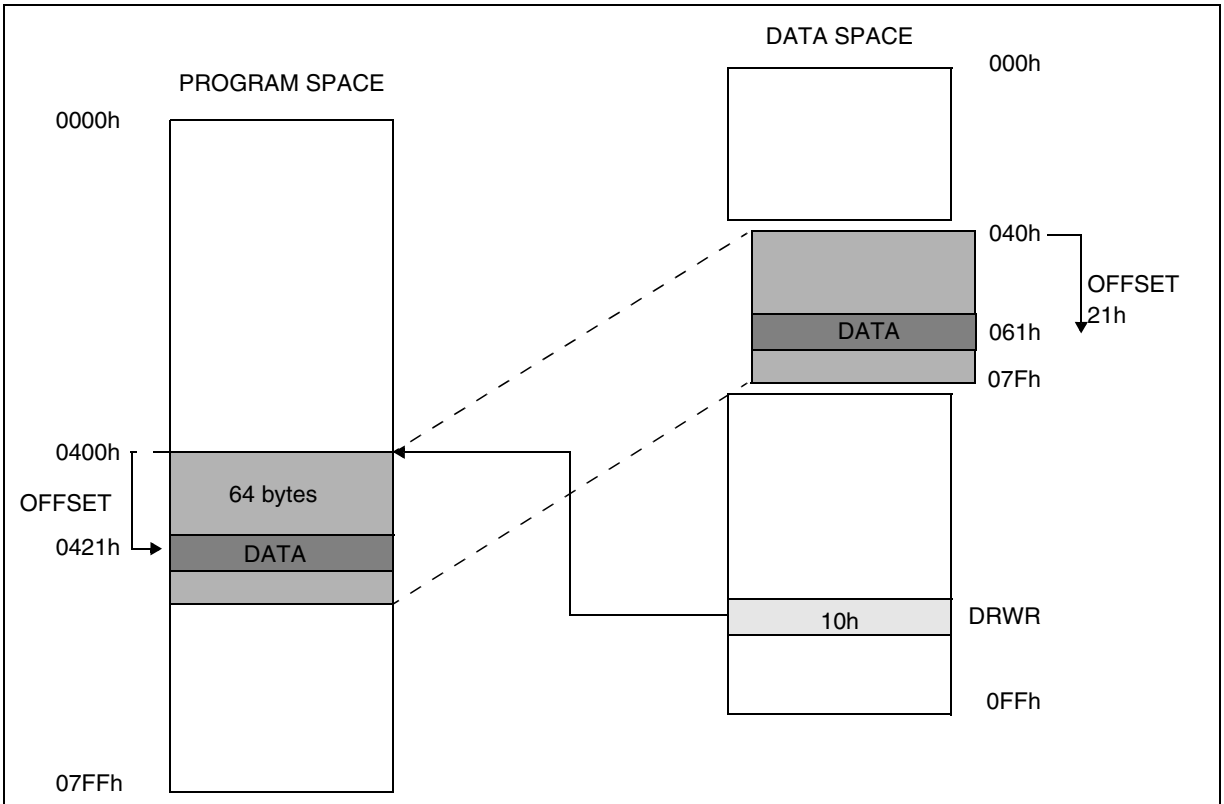
To understand how to determine the DRWR and the content of the register, please refer to the example shown in Figure 6. In any case the calculation is automatically handled by the ST6 development tools.

Please refer to the user manual of the correspoding tool.

3.1.6.3 Recommendations

Care is required when handling the DRWR register as it is write only. For this reason, the DRWR contents should not be changed while executing an interrupt service routine, as the service routine cannot save and then restore the register's previous contents. If it is impossible to avoid writing to the DRWR during the interrupt service routine, an image of the register must be saved in a RAM location, and each time the program writes to the DRWR, it must also write to the image register. The image register must be written first so that, if an interrupt occurs between the two instructions, the DRWR is not affected.

Figure 6. Data ROM Window Memory Addressing



DATA address in Program memory : 421h
DRWR content : 421h / 3Fh (64) = 10H data is located in 64-bytes window number 10h
64-byte window start address : 10h x 3Fh = 400h
Register (A, X,...)content : Offset = (421h - 400h) + 40h (Data ROM Window start address in data space) = 61h

5.9 EXTERNAL INTERRUPTS (I/O Ports)

External interrupt vectors can be loaded into the PC register if the corresponding external interrupt occurred and if the GEN bit is set. These interrupts allow the processor to exit from STOP mode.

The external interrupt polarity is selected through the IOR register.

External interrupts are linked to vectors #1 and # 2.

Interrupt requests on vector #1 can be configured either as edge or level-sensitive using the LES bit in the IOR Register.

Interrupt requests from vector #2 are always edge sensitive. The edge polarity can be configured using the ESB bit in the IOR Register.

In edge-sensitive mode, a latch is set when a edge occurs on the interrupt source line and is cleared when the associated interrupt routine is started. So, an interrupt request can be stored until completion of the currently executing interrupt routine, before being processed. If several interrupt requests occurs before completion of the current interrupt routine, only the first request is stored.

Storing of interrupt requests is not possible in level sensitive mode. To be taken into account, the low level must be present on the interrupt pin when the MCU samples the line after instruction execution.

5.9.1 Notes on using External Interrupts

ESB bit Spurious Interrupt on Vector #2

If a pin associated with interrupt vector #2 is configured as interrupt with pull-up, whenever vector #2 is configured to be rising edge sensitive (by setting the ESB bit in the IOR register), an interrupt is latched although a rising edge may not have occured on the associated pin.

This is due to the vector #2 circuitry.The workaround is to discard this first interrupt request in the routine (using a flag for example).

Masking of One Interrupt by Another on Vector #2.

When two or more port pins (associated with interrupt vector #2) are configured together as input with interrupt (falling edge sensitive), as long as one pin is stuck at '0', the other pin can never generate an interrupt even if an active edge occurs at this pin. The same thing occurs when one pin is stuck at '1' and interrupt vector #2 is configured as rising edge sensitive.

To avoid this the first pin must input a signal that goes back up to '1' right after the falling edge. Otherwise, in the interrupt routine for the first pin, deactivate the “input with interrupt” mode using the port control registers (DDR, OR, DR). An active edge on another pin can then be latched.

I/O port Configuration Spurious Interrupt on Vector #2

If a pin associated with interrupt vector #2 is in ‘input with pull-up’ state, a ‘0’ level is present on the pin and the ESB bit = 0, when the I/O pin is configured as interrupt with pull-up by writing to the DDRx, ORx and DRx register bits, an interrupt is latched although a falling edge may not have occurred on the associated pin.

In the opposite case, if the pin is in interrupt with pull-up state , a 0 level is present on the pin and the ESB bit =1, when the I/O port is configured as input with pull-up by writing to the DDRx, ORx and DRx bits, an interrupt is latched although a rising edge may not have occurred on the associated pin.

I/O PORTS (Cont'd)

7.5 REGISTER DESCRIPTION

DATA REGISTER (DR)

Port x Data Register
DRx with x = A or B.

Address DRA: 0C0h - Read/Write
Address DRB: 0C1h - Read/Write

Reset Value: 0000 0000 (00h)

7							0
D7	D6	D5	D4	D3	D2	D1	D0

Bits 7:0 = **D[7:0]** Data register bits.

Reading the DR register returns either the DR register latch content (pin configured as output) or the digital value applied to the I/O pin (pin configured as input).

Caution: In input mode, modifying this register will modify the I/O port configuration (see Table 9).

Do not use the Single bit instructions on I/O port data registers. See (Section 7.2.5).

DATA DIRECTION REGISTER (DDR)

Port x Data Direction Register
DDRx with x = A or B.

Address DDRA: 0C4h - Read/Write
Address DDRB: 0C5h - Read/Write

Reset Value: 0000 0000 (00h)

7							0
DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0

Bits 7:0 = **DD[7:0]** Data direction register bits.

The DDR register gives the input/output direction configuration of the pins. Each bit is set and cleared by software.
0: Input mode
1: Output mode

OPTION REGISTER (OR)

Port x Option Register
ORx with x = A or B.

Address ORA: 0CCh - Read/Write
Address ORB: 0CDh - Read/Write

Reset Value: 0000 0000 (00h)

7							0
O7	O6	O5	O4	O3	O2	O1	O0

Bits 7:0 = **O[7:0]** Option register bits.

The OR register allows to distinguish in output mode if the push-pull or open drain configuration is selected.

Output mode:
0: Open drain output(with P-Buffer deactivated)
1: Push-pull Output

Input mode: See Table 9.

Each bit is set and cleared by software.

Caution: Modifying this register, will also modify the I/O port configuration in input mode. (see Table 9).

Table 11. I/O Port Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
Reset Value of all I/O port registers		0	0	0	0	0	0	0	0
0C0h	**DRA**	MSB							LSB
0C1h	**DRB**								
0C4h	**DDRA**	MSB							LSB
0C5h	**DDRB**								
0CCh	**ORA**	MSB							LSB
0CDh	**ORB**								

8-BIT TIMER (Cont'd)

8.2.3 Counter/Prescaler Description

Prescaler

The prescaler input can be the internal frequency f_{INT} divided by 12 or an external clock applied to the TIMER pin. The prescaler decrements on the rising edge, depending on the division factor programmed by the PS[2:0] bits in the TSCR register.

The state of the 7-bit prescaler can be read in the PSCR register.

When the prescaler reaches 0, it is automatically reloaded with 7Fh.

Counter

The free running 8-bit downcounter is fed by the output of the programmable prescaler, and is decremented on every rising edge of the $f_{COUNTER}$ clock signal coming from the prescaler.

It is possible to read or write the contents of the counter on the fly, by reading or writing the timer counter register (TCR).

When the downcounter reaches 0, it is automatically reloaded with the value 0FFh.

Counter Clock and Prescaler

The counter clock frequency is given by:

$$f_{COUNTER} = f_{PRESCALER} / 2^{PS[2:0]}$$

where $f_{PRESCALER}$ can be:

– $f_{INT}/12$

– f_{EXT} (input on TIMER pin)

– $f_{INT}/12$ gated by TIMER pin

The timer input clock feeds the 7-bit programmable prescaler. The prescaler output can be programmed by selecting one of the 8 available prescaler taps using the PS[2:0] bits in the Status/Control Register (TSCR). Thus the division factor of the prescaler can be set to 2^n (where n equals 0, to 7). See Figure 27.

The clock input is enabled by the PSI (Prescaler Initialize) bit in the TSCR register. When PSI is reset, the counter is frozen and the prescaler is loaded with the value 7Fh. When PSI is set, the prescaler and the counter run at the rate of the selected clock source.

Counter and Prescaler Initialization

After RESET, the counter and the prescaler are initialized to 0FFh and 7Fh respectively.

The 7-bit prescaler can be initialized to 7Fh by clearing the PSI bit. Direct write access to the prescaler is also possible when PSI =1. Then, any value between 0 and 7Fh can be loaded into it.

The 8-bit counter can be initialized separately by writing to the TCR register.

8.2.3.1 8-bit Counting and Interrupt Capability on Counter Underflow

Whatever the division factor defined for the prescaler, the Timer Counter works as an 8-bit downcounter. The input clock frequency is user selectable using the PS[2:0] bits.

When the downcounter decrements to zero, the TMZ (Timer Zero) bit in the TSCR is set. If the ETI (Enable Timer Interrupt) bit in the TSCR is also set, an interrupt request is generated.

The Timer interrupt can be used to exit the MCU from WAIT or STOP mode.

The TCR can be written at any time by software to define a time period ending with an underflow event, and therefore manage delay or timer functions.

TMZ is set when the downcounter reaches zero; however, it may also be set by writing 00h in the TCR register or by setting bit 7 of the TSCR register.

The TMZ bit must be cleared by user software when servicing the timer interrupt to avoid undesired interrupts when leaving the interrupt service routine.

Note: A write to the TCR register will predominate over the 8-bit counter decrement to 00h function, i.e. if a write and a TCR register decrement to 00h occur simultaneously, the write will take precedence, and the TMZ bit is not set until the 8-bit counter underflows again.

8-BIT TIMER (Cont'd)

8.2.4.2 Event Counter Mode

(TOUT = "0", DOUT = "0")

In this mode, the TIMER pin is the input clock of the Timer prescaler which is decremented on every rising edge of the input clock (allowing event count). See Figure 30 and Figure 31.

This mode is selected by clearing the TOUT bit in the TSCR register (i.e. as input) and clearing the DOUT bit.

Note: In this mode, if the TIMER pin is multiplexed, the corresponding port control bits have to be set in input with pull-up configuration.

Figure 30. f_{TIMER} Clock in Event Counter Mode

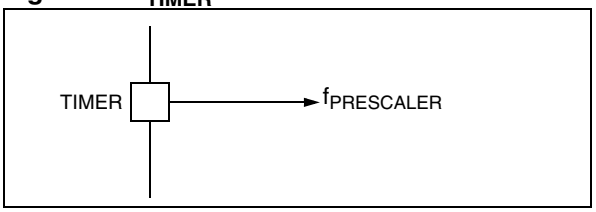
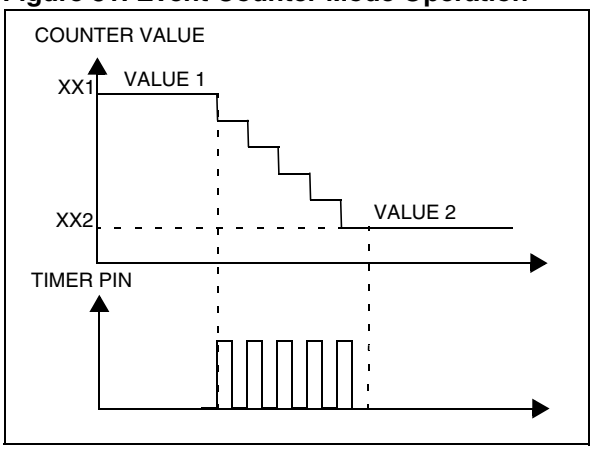


Figure 31. Event Counter Mode Operation



8.2.4.3 Output Mode

(TOUT = "1", DOUT = "data out")

In Output mode, the TIMER pin is connected to the DOUT latch, hence the Timer prescaler is clocked by the prescaler clock input (f_{INT}/12). See Figure 32.

The user can select the prescaler division ratio using the PS[2:0] bits in the TSCR register. When TCR decrements to zero, it sets the TMZ bit in the TSCR. The TMZ bit can be tested under program control to perform a timer function whenever it goes high and has to be cleared by the user. The low-to-high TMZ bit transition is used to latch the DOUT bit in the TSCR and, if the TOUT bit is set, DOUT is transferred to the TIMER pin. This operating mode allows external signal generation on the TIMER pin. See Figure 33.

This mode is selected by setting the TOUT bit in the TSCR register (i.e. as output) and setting the DOUT bit to output a high level or clearing the DOUT bit to output a low level.

Note: As soon as the TOUT bit is set, The timer pin is configured as output push-pull regardless of the corresponding I/O port control registers setting (if the TIMER pin is multiplexed).

Figure 32. Output Mode Control

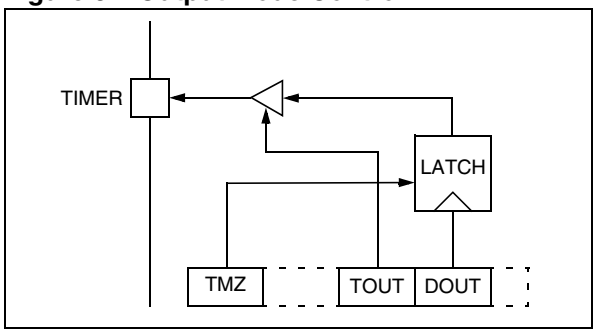
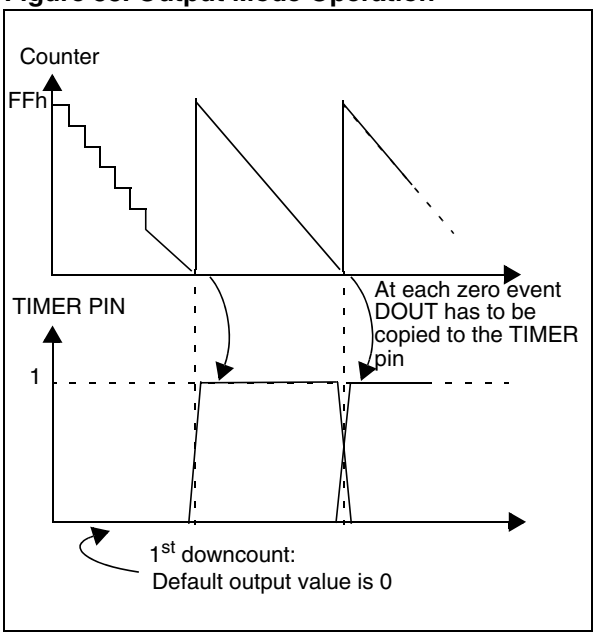


Figure 33. Output Mode Operation



8-BIT TIMER (Cont'd)

8.2.5 Low Power Modes

Mode	Description
WAIT	No effect on timer. Timer interrupt events cause the device to exit from WAIT mode.
STOP	Timer registers are frozen except in Event Counter mode (with external clock on TIMER pin).

8.2.6 Interrupts

Interrupt Event	Event Flag	Enable Bit	Exit from Wait	Exit from Stop
Timer Zero Event	TMZ	ETI	Yes	Yes

A/D CONVERTER (Cont'd)

8.3.5 Low Power Modes

Mode	Description
WAIT	No effect on A/D Converter. ADC interrupts cause the device to exit from Wait mode.
STOP	A/D Converter disabled.

Note: The A/D converter may be disabled by clearing the PDS bit. This feature allows reduced power consumption when no conversion is needed.

8.3.6 Interrupts

Interrupt Event	Event Flag	Enable Bit	Exit from Wait	Exit from Stop
End of Conversion	EOC	EAI	Yes	No

Note: The EOC bit is cleared only when a new conversion is started (it cannot be cleared by writing 0). To avoid generating further EOC interrupt, the EAI bit has to be cleared within the ADC interrupt subroutine.

8.3.7 Register Description

A/D CONVERTER CONTROL REGISTER (ADCR)

Address: 0D1h - Read/Write (Bit 6 Read Only, Bit 5 Write Only)

Reset value: 0100 0000 (40h)

7							0
EAI	EOC	STA	PDS	ADCR 3	OSC OFF	ADCR 1	ADCR 0

Bit 7 = **EAI** Enable A/D Interrupt.
0: ADC interrupt disabled
1: ADC interrupt enabled

Bit 6 = **EOC** End of conversion. Read Only
When a conversion has been completed, this bit is set by hardware and an interrupt request is generated if the EAI bit is set. The EOC bit is automatically cleared when the STA bit is set. Data in the data conversion register are valid only when this bit is set to "1".
0: Conversion is not complete
1: Conversion can be read from the ADR register

Bit 5 = **STA**: Start of Conversion. Write Only.
0: No effect
1: Start conversion

Note: Setting this bit automatically clears the EOC bit. If the bit is set again when a conversion is in progress, the present conversion is stopped and a new one will take place. This bit is write only, any attempt to read it will show a logical zero.

Bit 4 = **PDS** Power Down Selection.

0: A/D converter is switched off
1: A/D converter is switched on

Bit 3 = **ADCR3 Reserved**, must be cleared.

Bit 2 = **OSCOFF** Main Oscillator off.

0: Main Oscillator enabled
1: Main Oscillator disabled

Note: This bit does not apply to the ADC peripheral but to the main clock system. Refer to the Clock System section.

Bits 1:0 = **ADCR[1:0] Reserved**, must be cleared.

A/D CONVERTER DATA REGISTER (ADR)

Address: 0D0h - Read only

Reset value: xxxx xxxx (xxh)

7							0
ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0

Bits 7:0 = **ADR[7:0]**: 8 Bit A/D Conversion Result.

Table 16. ADC Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0D0h	**ADR** Reset Value	ADR7 0	ADR6 0	ADR5 0	ADR4 0	ADR3 0	ADR2 0	ADR1 0	ADR0 0
0D1h	**ADCR** Reset Value	EAI 0	EOC 1	STA 0	PDS 0	ADCR3 0	OSCOFF 0	ADCR1 0	ADCR0 0

9 INSTRUCTION SET

9.1 ST6 ARCHITECTURE

The ST6 architecture has been designed for maximum efficiency while keeping byte usage to a minimum; in short, to provide byte-efficient programming. The ST6 core has the ability to set or clear any register or RAM location bit in Data space using a single instruction. Furthermore, programs can branch to a selected address depending on the status of any bit in Data space.

9.2 ADDRESSING MODES

The ST6 has nine addressing modes, which are described in the following paragraphs. Three different address spaces are available: Program space, Data space, and Stack space. Program space contains the instructions which are to be executed, plus the data for immediate mode instructions. Data space contains the Accumulator, the X, Y, V and W registers, peripheral and Input/Output registers, the RAM locations and Data ROM locations (for storage of tables and constants). Stack space contains six 12-bit RAM cells used to stack the return addresses for subroutines and interrupts.

Immediate. In immediate addressing mode, the operand of the instruction follows the opcode location. As the operand is a ROM byte, the immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

Direct. In direct addressing mode, the address of the byte which is processed by the instruction is stored in the location which follows the opcode. Direct addressing allows the user to directly address the 256 bytes in Data Space memory with a single two-byte instruction.

Short Direct. The core can address the four RAM registers X, Y, V, W (locations 80h, 81h, 82h, 83h) in short-direct addressing mode. In this case, the instruction is only one byte and the selection of the location to be processed is contained in the opcode. Short direct addressing is a subset of direct addressing mode. (Note that 80h and 81h are also indirect registers).

Extended. In extended addressing mode, the 12-bit address needed to define the instruction is obtained by concatenating the four least significant bits of the opcode with the byte following the opcode. The instructions (JP, CALL) which use extended addressing mode are able to branch to any address in the 4 Kbyte Program space.

Extended addressing mode instructions are two bytes long.

Program Counter Relative. Relative addressing mode is only used in conditional branch instructions. The instruction is used to perform a test and, if the condition is true, a branch with a span of -15 to +16 locations next to the address of the relative instruction. If the condition is not true, the instruction which follows the relative instruction is executed. Relative addressing mode instructions are one byte long. The opcode is obtained by adding the three most significant bits which characterize the test condition, one bit which determines whether it is a forward branch (when it is 0) or backward branch (when it is 1) and the four least significant bits which give the span of the branch (0h to Fh) which must be added or subtracted from the address of the relative instruction to obtain the branch destination address.

Bit Direct. In bit direct addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode points to the address of the byte in which the specified bit must be set or cleared. Thus, any bit in the 256 locations of Data space memory can be set or cleared.

Bit Test & Branch. Bit test and branch addressing mode is a combination of direct addressing and relative addressing. Bit test and branch instructions are three bytes long. The bit identification and the test condition are included in the opcode byte. The address of the byte to be tested is given in the next byte. The third byte is the jump displacement, which is in the range of -127 to +128. This displacement can be determined using a label, which is converted by the assembler.

Indirect. In indirect addressing mode, the byte processed by the register-indirect instruction is at the address pointed to by the content of one of the indirect registers, X or Y (80h, 81h). The indirect register is selected by bit 4 of the opcode. Register indirect instructions are one byte long.

Inherent. In inherent addressing mode, all the information necessary for executing the instruction is contained in the opcode. These instructions are one byte long.

Opcode Map Summary. The following table contains an opcode map for the instructions used by the ST6

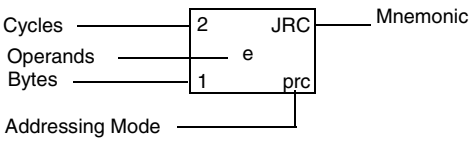
LOW / HI	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	LOW / HI
0 0000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b0,rr,ee 3 bt	2 JRZ e 1 pcr	2 NOP #	2 JRC e 1 prc	4 LD a,(x) 1 ind	0 0000
1 0001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b0,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC x 1 sd	2 JRC e 1 prc	4 LDI a,nn 2 imm	1 0001
2 0010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b4,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 CP a,(x) 1 ind	2 0010
3 0011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b4,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,x 1 sd	2 JRC e 1 prc	4 CPI a,nn 2 imm	3 0011
4 0100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b2,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 ADD a,(x) 1 ind	4 0100
5 0101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b2,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC y 1 sd	2 JRC e 1 prc	4 ADDI a,nn 2 imm	5 0101
6 0110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b6,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 INC (x) 1 ind	6 0110
7 0111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b6,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,y 1 sd	2 JRC e 1 prc	#	7 0111
8 1000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b1,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 LD (x),a 1 ind	8 1000
9 1001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b1,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC v 1 sd	2 JRC e 1 prc	#	9 1001
A 1010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b5,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 AND a,(x) 1 ind	A 1010
B 1011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b5,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,v 1 sd	2 JRC e 1 prc	4 ANDI a,nn 2 imm	B 1011
C 1100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b3,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 SUB a,(x) 1 ind	C 1100
D 1101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b3,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC w 1 sd	2 JRC e 1 prc	4 SUBI a,nn 2 imm	D 1101
E 1110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b7,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 DEC (x) 1 ind	E 1110
F 1111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b7,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,w 1 sd	2 JRC e 1 prc	#	F 1111

Abbreviations for Addressing Modes:

dir	Direct
sd	Short Direct
imm	Immediate
inh	Inherent
ext	Extended
b.d	Bit Direct
bt	Bit Test
pcr	Program Counter Relative
ind	Indirect

Legend:

#	Indicates Illegal Instructions
e	5-bit Displacement
b	3-bit Address
rr	1-byte Data space address
nn	1-byte immediate data
abc	12-bit address
ee	8-bit displacement



10.5 CLOCK AND TIMING CHARACTERISTICS

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A.

10.5.1 General Timings

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$t_{c(INST)}$	Instruction cycle time		2	4	5	t_{CPU}
		f_{CPU}=8 MHz	3.25	6.5	8.125	µs
$t_{v(IT)}$	Interrupt reaction time [2] $t_{v(IT)} = \Delta t_{c(INST)} + 6$		6		11	t_{CPU}
		f_{CPU}=8 MHz	9.75		17.875	µs

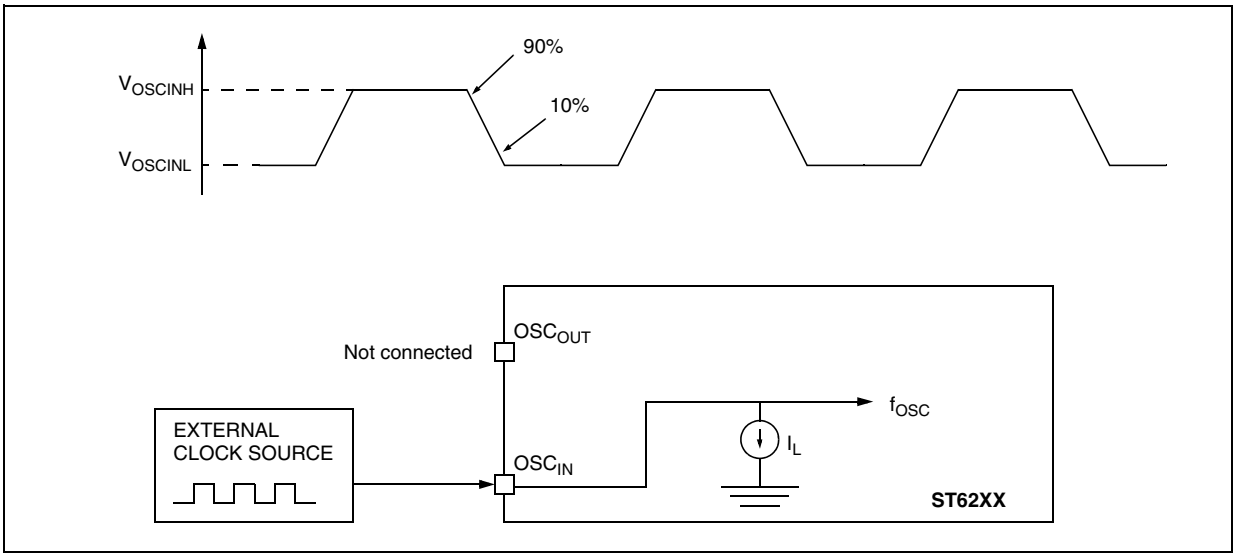
10.5.2 External Clock Source

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OSCINH}	OSC_{IN} input pin high level voltage	See Figure 49	$0.7xV_{DD}$		V_{DD}	V
V_{OSCINL}	OSC_{IN} input pin low level voltage		V_{SS}		$0.3xV_{DD}$	
I_L	OSCx Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			± 2	µA

Notes:

1. Data based on typical application software.
2. Time measured between interrupt event and interrupt vector fetch. $\Delta t_{c(INST)}$ is the number of t_{CPU} cycles needed to finish the current instruction execution.

Figure 49. Typical Application with an External Clock Source



EMC CHARACTERISTICS (Cont'd)

10.7.2 Absolute Electrical Sensitivity

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the AN1181 application note.

10.7.2.1 Electro-Static Discharge (ESD)

Electro-Static Discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends of the number of supply pins of the device (3 parts*(n+1) supply pin). Two models are usually simulated: Human Body Model and Machine Model. This test conforms to the JESD22-A114A/A115A standard. See Figure 57 and the following test sequences.

Human Body Model Test Sequence

– C_L is loaded through S1 by the HV pulse generator.
– S1 switches position from generator to R.
– A discharge from C_L through R (body resistance) to the ST6 occurs.
– S2 must be closed 10 to 100ms after the pulse delivery period to ensure the ST6 is not left in charge state. S2 must be opened at least 10ms prior to the delivery of the next pulse.

Machine Model Test Sequence

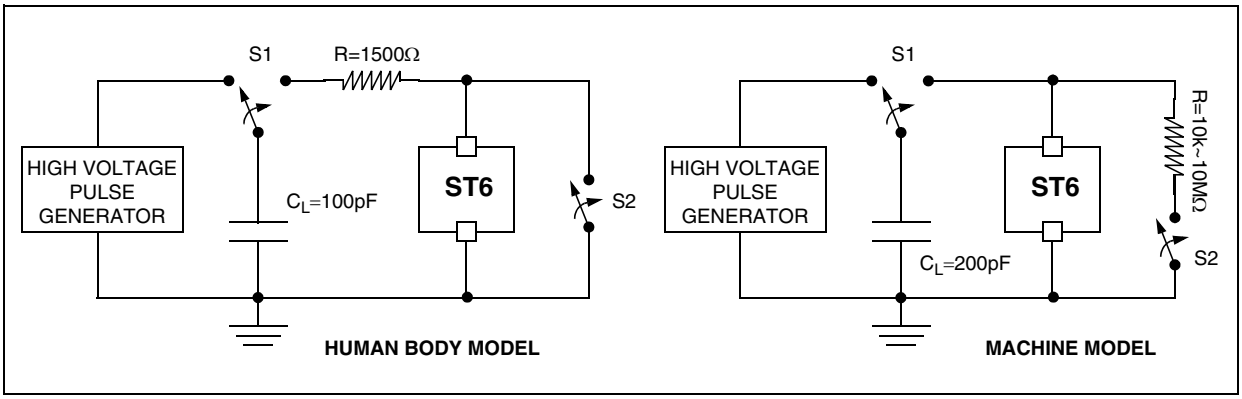
– C_L is loaded through S1 by the HV pulse generator.
– S1 switches position from generator to ST6.
– A discharge from C_L to the ST6 occurs.
– S2 must be closed 10 to 100ms after the pulse delivery period to ensure the ST6 is not left in charge state. S2 must be opened at least 10ms prior to the delivery of the next pulse.
– R (machine resistance), in series with S2, ensures a slow discharge of the ST6.

Absolute Maximum Ratings

Symbol	Ratings	Conditions	Maximum value [1]	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25°C	2000	V
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)	T_A=+25°C	200	

Notes:
1. Data based on characterization results, not tested in production.

Figure 57. Typical Equivalent ESD Circuits



CONTROL PIN CHARACTERISTICS (Cont'd)

10.10 TIMER PERIPHERAL CHARACTERISTICS

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (TIMER).

10.10.1 Watchdog Timer

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(WDG)}$	Watchdog time-out duration		3,072		196,608	t_{INT}
		f_{CPU}=4MHz	0.768		49.152	ms
		f_{CPU}=8MHz	0.384		24.576	ms

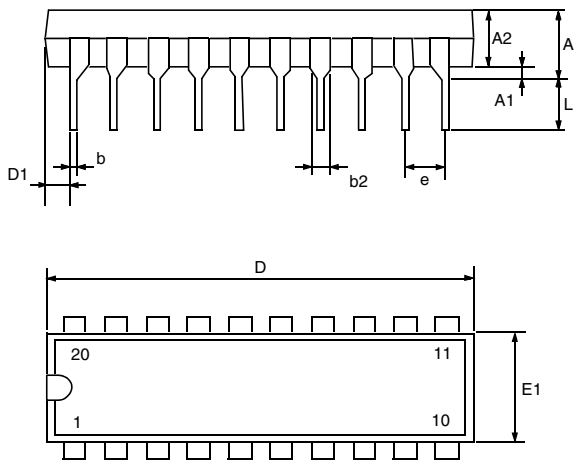
10.10.2 8-Bit Timer

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{EXT}	Timer external clock frequency		0		f_{INT}/4	MHz
t_w	Pulse width at TIMER pin	VDD>4.5V	125			ns
		VDD=3V	1			µs

11 GENERAL INFORMATION

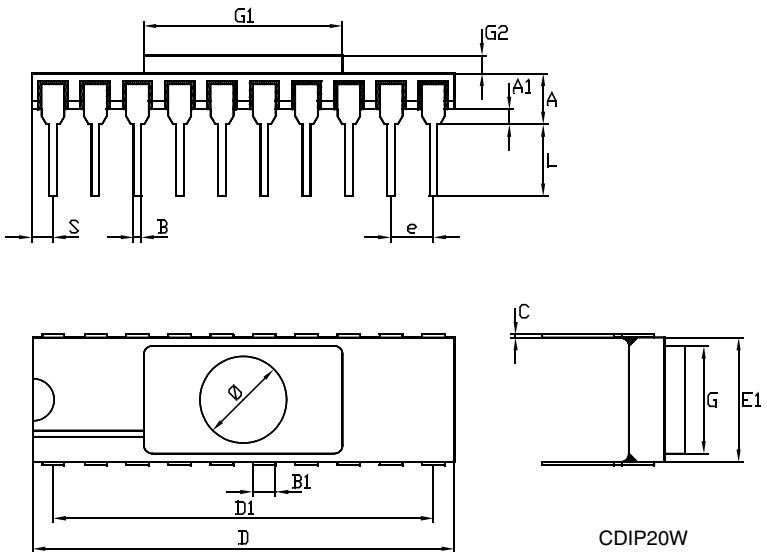
11.1 PACKAGE MECHANICAL DATA

Figure 74. 20-Pin Plastic Dual In-Line Package, 300-mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	24.89	26.16	26.92	0.980	1.030	1.060
D1	0.13			0.005		
e		2.54			0.100	
eB			10.92			0.430
E1	6.10	6.35	7.11	0.240	0.250	0.280
L	2.92	3.30	3.81	0.115	0.130	0.150
	Number of Pins					
N	20					

Figure 75. 20-Pin Ceramic Side-Brazed Dual In-Line Package

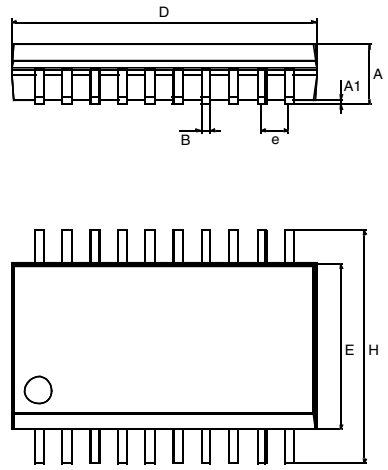


CDIP20W

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.63			0.143
A1	0.38			0.015		
B	3.56	0.46	0.56	0.140	0.018	0.022
B1	1.14	12.70	1.78	0.045	0.500	0.070
C	0.20	0.25	0.36	0.008	0.010	0.014
D	24.89	25.40	25.91	0.980	1.000	1.020
D1		22.86			0.900	
E1	6.99	7.49	8.00	0.275	0.295	0.315
e		2.54			0.100	
G	6.35	6.60	6.86	0.250	0.260	0.270
G1	9.47	9.73	9.98	0.373	0.383	0.393
G2		1.14			0.045	
L	2.92	3.30	3.81	0.115	0.130	0.150
S		12.70			0.500	
Ø		4.22			0.166	
	Number of Pins					
N	20					

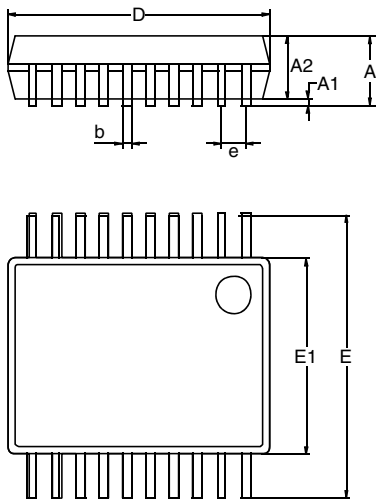
PACKAGE MECHANICAL DATA (Cont'd)

Figure 76. 20-Pin Plastic Small Outline Package, 300-mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.00		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
α	0°		8°	0°		8°
L	0.40		1.27	0.016		0.050
	Number of Pins					
N	20					

Figure 77. 20-Pin Plastic Shrink Small Outline Package



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			2.00			0.079
A1	0.05			0.002		
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22		0.38	0.009		0.015
c	0.09		0.25	0.004		0.010
D	6.90	7.20	7.50	0.272	0.283	0.295
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
e		0.65			0.026	
θ	0°	4°	8°	0°	4°	8°
L	0.55	0.75	0.95	0.022	0.030	0.037
	Number of Pins					
N	20					

14 SUMMARY OF CHANGES

Description of the changes between the current release of the specification and the previous one.

Revision	Main Changes	Date
3.3	Removed references to 32768 clock cycle delay in Section 5 and Section 6 Changed note 2 in Section 10.6.2 on page 76: added text on data retention and programmability.	October 03
4	Updated device summary on page 1 Replaced soldering information by ECOPACK® information in Section 11.3 on page 93 Updated disclaimer on last page	January 2009

15 TO GET MORE INFORMATION

To get the latest information on this product please use the STMicroelectronics web server.

➟ http://www.st.com/