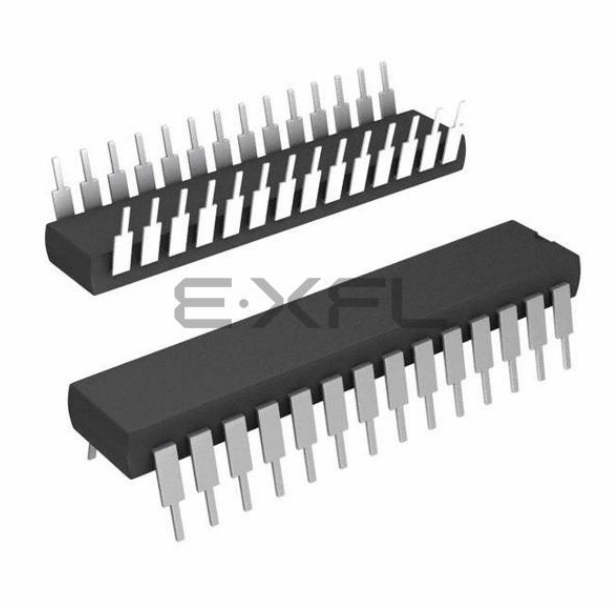

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18455-e-sp

13.4.9 WRERR Bit

The WRERR bit can be used to determine if a write error occurred. WRERR will be set if one of the following conditions occurs:

- If WR is set while the NVMADRH:NMVADRL points to a write-protected address
- A Reset occurs while a self-write operation was in progress
- An unlock sequence was interrupted

The WRERR bit is normally set by hardware, but can be set by the user for test purposes. Once set, WRERR must be cleared in software.

Table 13-3. Actions for PFM When WR = 1

Free	LWLO	Actions for PFM when WR = 1	Comments
1	x	Erase the 32-word row of NVMADRH:NVMADRL location.	• If WP is enabled, WR is cleared and WRERR is set • All 32 words are erased • NVMDATH:NVMDATL is ignored
0	1	Copy NVMDATH:NVMDATL to the write latch corresponding to NVMADR LSBs.	• Write protection is ignored • No memory access occurs
0	0	Write the write-latch data to PFM row.	• If WP is enabled, WR is cleared and WRERR is set • Write latches are reset to 3FFh • NVMDATH:NVMDATL is ignored

Related Links

13.4.4 NVMREG Erase of Program Memory

14.7.1 PORTA

Name: PORTA
Address: 0x00C

PORTA Register
Note: Writes to PORTA are actually written to the corresponding LATA register.
Reads from PORTA register return actual I/O pin values.

Bit	7	6	5	4	3	2	1	0
	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 0, 1, 2, 3, 4, 5, 6, 7 – RAn Port I/O Value bits
Reset States: POR/BOR = xxxxxxxx
All Other Resets = uuuuuuuu

Value	Description
1	Port pin is ≥ V_{IH}
0	Port pin is ≤ V_{IL}

14.7.14 WPUA

Name: WPUA
Address: 0x1F39

Weak Pull-up Register

Bit	7	6	5	4	3	2	1	0
	WPUA7	WPUA6	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 – WPUAn Weak Pull-up PORTA Control bits

Value	Description
1	Weak Pull-up enabled
0	Weak Pull-up disabled

16.5.3 PMD2

Name: PMD2
Address: 0x798

PMD Control Register 2

Bit	7	6	5	4	3	2	1	0
	NCO1MD							
Access	R/W							
Reset	0							

Bit 7 – NCO1MD Disable Numerically Control Oscillator bit

Value	Description
1	NCO1 module disabled
0	NCO1 module enabled

20.8.10 ADACQ

Name: ADACQ
Address: 0x10C

ADC Acquisition Time Control Register

Bit	15	14	13	12	11	10	9	8
				ACQH[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ACQL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 12:8 – ACQH[4:0] Acquisition (charge share time) Select bits (High Byte)

Value	Description
1 to 8191	Number of ADC clock periods in the acquisition time
0	Acquisition time is not included in the data conversion cycle(1)

Bits 7:0 – ACQL[7:0] Acquisition (charge share time) Select bits (Low Byte)

Value	Description
1 to 8191	Number of ADC clock periods in the acquisition time
0	Acquisition time is not included in the data conversion cycle(1)

Note:

1. If ADPRE is not equal to '0', then ADACQ = 0b0_0000_0000_0000 means Acquisition time is 8192 clocks of the selected ADC clock.

26.14.3 TMRxCLK

Name: TMRxCLK
Address: 0x211,0x217,0x21D

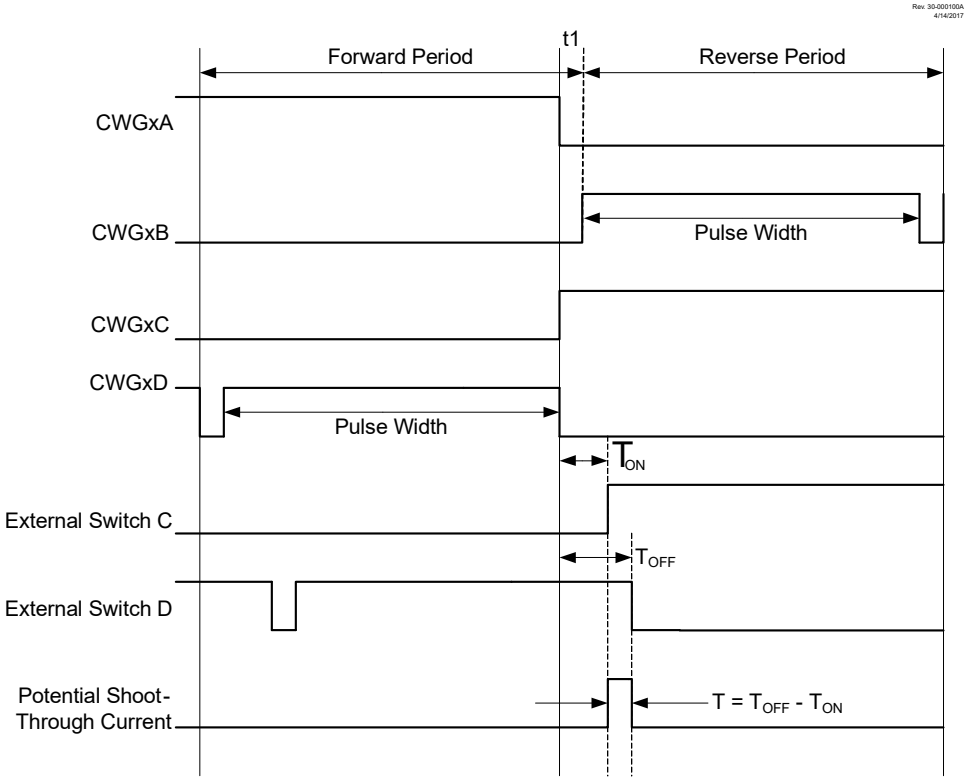
Timer Clock Source Selection Register

Bit	7	6	5	4	3	2	1	0
				CS[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – CS[4:0] Timer Clock Source Selection bits
Refer to the clock source selection table.

Reset States: POR/BOR = 00000
All Other Resets = uuuuu

Figure 31-8. Example of PWM Direction Change at Near 100% Duty Cycle



31.2.4 Steering Modes

In both Synchronous and Asynchronous Steering modes, the modulated input signal can be steered to any combination of four CWG outputs. A fixed-value will be presented on all the outputs not used for the PWM output. Each output has independent polarity, steering, and shutdown options. Dead-band control is not used in either steering mode.

Related Links

1.4.2.2 Long Bit Names

32.12.2 MDxCON1

Name: MDxCON1
Address: 0x0898

Modulation Control Register 1

Bit	7	6	5	4	3	2	1	0
			CHPOL	CHSYNC			CLPOL	CLSYNC
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit 5 – CHPOL Modulator High Carrier Polarity Select bit

Value	Description
1	Selected high carrier signal is inverted
0	Selected high carrier signal is not inverted

Bit 4 – CHSYNC Modulator High Carrier Synchronization Enable bit

Value	Description
1	Modulator waits for a falling edge on the high time carrier signal before allowing a switch to the low time carrier
0	Modulator output is not synchronized to the high time carrier signal

Bit 1 – CLPOL Modulator Low Carrier Polarity Select bit

Value	Description
1	Selected low carrier signal is inverted
0	Selected low carrier signal is not inverted

Bit 0 – CLSYNC Modulator Low Carrier Synchronization Enable bit

Value	Description
1	Modulator waits for a falling edge on the low time carrier signal before allowing a switch to the high time carrier
0	Modulator output is not synchronized to the low time carrier signal

Note:

1. Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

33.8.11 CLCDATA

Name: CLCDATA
Address: 0x1E0F

CLC Data Ouput Register

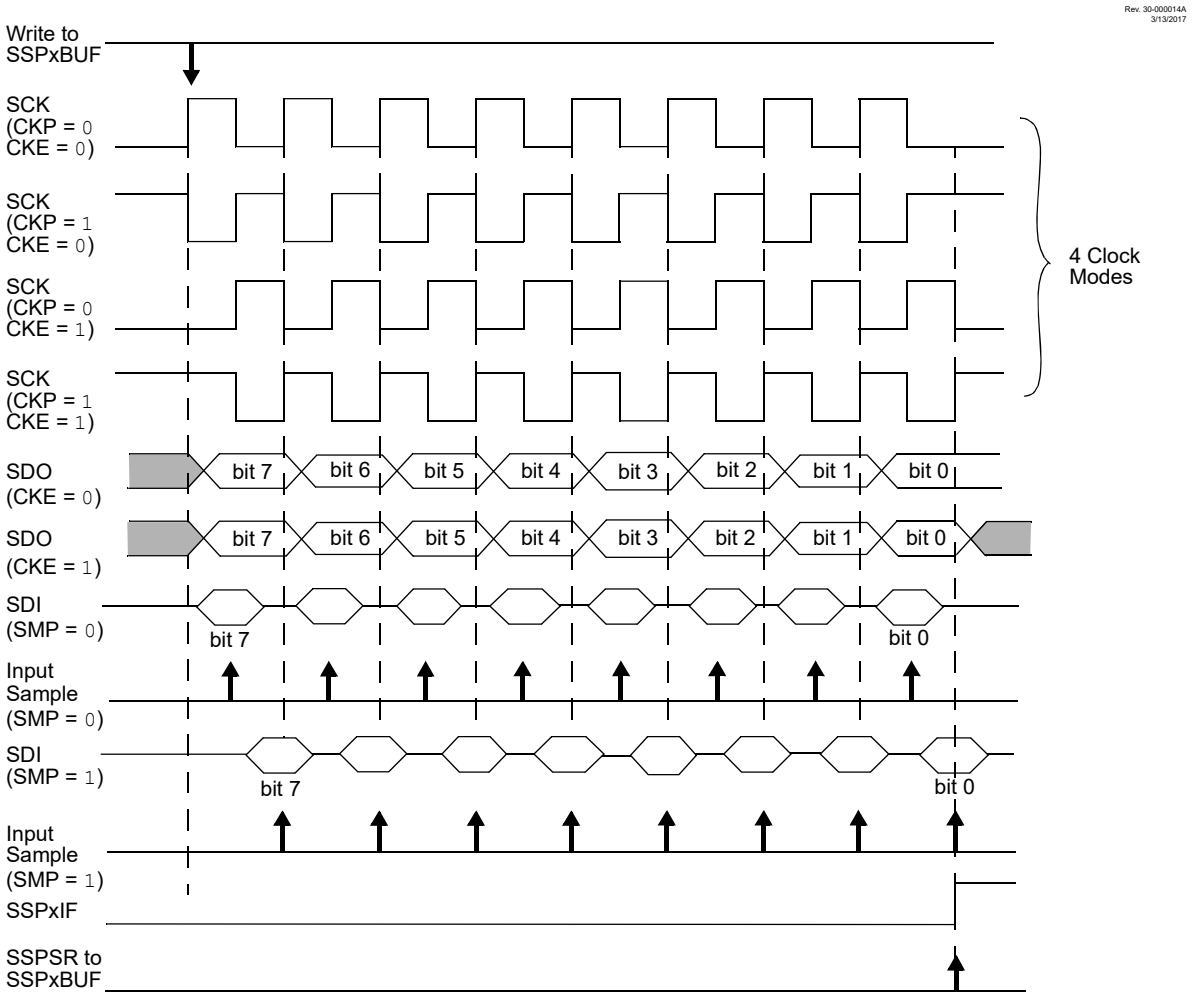
Mirror copy of

Bit	7	6	5	4	3	2	1	0
					MLC4OUT	MLC3OUT	MLC2OUT	MLC1OUT
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 0, 1, 2, 3 – MLCxOUT
Mirror copy of CLCx_out bit

Value	Description
1	CLCx_out is 1
0	CLCx_out is 0

Figure 35-4. SPI Mode Waveform (Master Mode)



35.2.2 SPI Slave Mode

In Slave mode, the data is transmitted and received as external clock pulses appear on SCK. When the last bit is latched, the SSPxIF interrupt flag bit is set.

Before enabling the module in SPI Slave mode, the clock line must match the proper Idle state. The clock line can be observed by reading the SCK pin. The Idle state is determined by the CKP bit.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in Sleep mode, the slave can transmit/receive data. The shift register is clocked from the SCK pin input and when a byte is received, the device will generate an interrupt. If enabled, the device will wake-up from Sleep.

35.2.3 Daisy-Chain Configuration

The SPI bus can sometimes be connected in a daisy-chain configuration. The first slave output is connected to the second slave input, the second slave output is connected to the third slave input, and so on. The final slave output is connected to the master input. Each slave sends out, during a second group of clock pulses, an exact copy of what was received during the first group of clock pulses. The whole

is held low until SSPxADD is updated to receive a high byte again. When SSPxADD is updated the UA bit is cleared. This ensures the module is ready to receive the high address byte on the next communication.

A high and low address match as a write request is required at the start of all 10-bit addressing communication. A transmission can be initiated by issuing a Restart once the slave is addressed, and clocking in the high address with the R/$\overline{W}$ bit set. The slave hardware will then acknowledge the read request and prepare to clock out data. This is only valid for a slave after it has received a complete high and low address byte match.

35.5.2 Slave Reception

When the R/$\overline{W}$ bit of a matching received address byte is clear, the R/W bit is cleared. The received address is loaded into the SSPxBUF register and acknowledged.

When the overflow condition exists for a received address, then not Acknowledge is given. An overflow condition is defined as either bit BF is set, or bit SSPOV is set. The BOEN bit modifies this operation. For more information see SSPxCON3.

An MSSP interrupt is generated for each transferred data byte. Flag bit, SSPxIF, must be cleared by software.

When the SEN bit is set, SCL will be held low (clock stretch) following each received byte. The clock must be released by setting the CKP bit, except sometimes in 10-bit mode. See 35.5.6.2 10-bit Addressing Mode for more detail.

35.5.2.1 7-bit Addressing Reception

This section describes a standard sequence of events for the MSSP module configured as an I^2C slave in 7-bit Addressing mode. Figure 35-14 and Figure 35-15 is used as a visual reference for this description.

This is a step by step process of what typically must be done to accomplish I^2C communication.

1. Start bit detected.
2. S bit is set; SSPxIF is set if interrupt on Start detect is enabled.
3. Matching address with R/W bit clear is received.
4. The slave pulls SDA low sending an $\overline{ACK}$ to the master, and sets SSPxIF bit.
5. Software clears the SSPxIF bit.
6. Software reads received address from SSPxBUF clearing the BF flag.
7. If SEN = 1; Slave software sets CKP bit to release the SCL line.
8. The master clocks out a data byte.
9. Slave drives SDA low sending an $\overline{ACK}$ to the master, and sets SSPxIF bit.
10. Software clears SSPxIF.
11. Software reads the received byte from SSPxBUF clearing BF.
12. Steps 8-12 are repeated for all received bytes from the master.
13. Master sends Stop condition, setting P bit, and the bus goes idle.

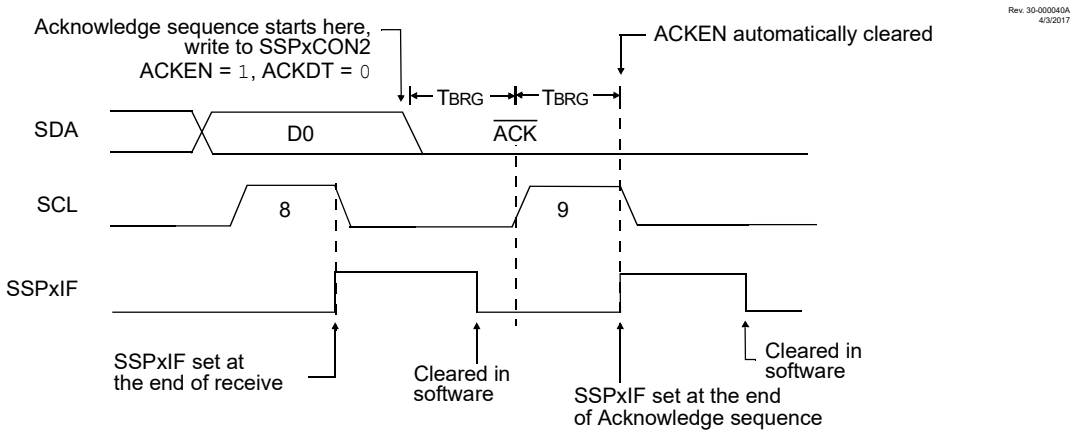
35.5.2.2 7-bit Reception with AHEN and DHEN

Slave device reception with AHEN and DHEN set operate the same as without these options with extra interrupts and clock stretching added after the eighth falling edge of SCL. These additional interrupts allow the slave software to decide whether it wants to $\overline{ACK}$ the receive address or data byte, rather than the hardware. This functionality adds support for PMBus™ that was not present on previous versions of this module.

35.6.8 Acknowledge Sequence Timing

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable ACKEN bit. When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (T_{BRG}) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts for T_{BRG}. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into Idle mode.

Figure 35-30. Acknowledge Sequence Waveform



Note: TBRG = one Baud Rate Generator period.

35.6.8.1 Acknowledge Write Collision

If the user writes the SSPxBUF when an Acknowledge sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

35.6.9 Stop Condition Timing

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable PEN bit. At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCL pin will be brought high and one T_{BRG} (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit is set. One T_{BRG} later, the PEN bit is cleared and the SSPxIF bit is set.

35.9.2 SSPxCON1

Name: SSPxCON1
Address: 0x190,0x19A

MSSP Control Register 1

Bit	7	6	5	4	3	2	1	0
	WCOL	SSPOV	SSPEN	CKP	SSPM[3:0]			
Access	R/W/HS	R/W/HS	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – WCOL
Write Collision Detect bit

Value	Mode	Description
1	SPI	A write to the SSPxBUF register was attempted while the previous byte was still transmitting (must be cleared by software)
1	I^2C Master transmit	A write to the SSPxBUF register was attempted while the I^2C conditions were not valid for a transmission to be started (must be cleared by software)
1	I^2C Slave transmit	The SSPxBUF register is written while it is still transmitting the previous word (must be cleared in software)
0	SPI or I^2C Master or Slave transmit	No collision
x	Master or Slave receive	Don't care

Bit 6 – SSPOV
Receive Overflow Indicator bit(1)

Value	Mode	Description
1	SPI Slave	A byte is received while the SSPxBUF register is still holding the previous byte. The user must read SSPxBUF, even if only transmitting data, to avoid setting overflow. (must be cleared in software)
1	I^2C Receive	A byte is received while the SSPxBUF register is still holding the previous byte (must be cleared in software)
0	SPI Slave or I^2C Receive	No overflow
x	SPI Master or I^2C Master transmit	Don't care

Bit 5 – SSPEN
Master Synchronous Serial Port Enable bit.(2)

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the Global Interrupt Enable (GIE) bit is also set then the Interrupt Service Routine at address 0004h will be called.

36.6.3 BAUDxCON

Name: BAUDxCON
Address: 0x11F,0xA1F

Baud Rate Control Register

Bit	7	6	5	4	3	2	1	0
	ABDOVF	RCIDL		SCKP	BRG16		WUE	ABDEN
Access	RO	RO		RW	RW		RW	RW
Reset	0	0		0	0		0	0

Bit 7 – ABDOVF Auto-Baud Detect Overflow bit

Value	Condition	Description
1	SYNC= 0	Auto-baud timer overflowed
0	SYNC= 0	Auto-baud timer did not overflow
X	SYNC= 1	Don't care

Bit 6 – RCIDL Receive Idle Flag bit

Value	Condition	Description
1	SYNC= 0	Receiver is Idle
0	SYNC= 0	Start bit has been received and the receiver is receiving
X	SYNC= 1	Don't care

Bit 4 – SCKP Synchronous Clock Polarity Select bit

Value	Condition	Description
1	SYNC= 0	Idle state for transmit (TX) is a low level (transmit data inverted)
0	SYNC= 0	Idle state for transmit (TX) is a high level (transmit data is non-inverted)
1	SYNC= 1	Data is clocked on rising edge of the clock
0	SYNC= 1	Data is clocked on falling edge of the clock

Bit 3 – BRG16 16-bit Baud Rate Generator Select bit

Value	Description
1	16-bit Baud Rate Generator is used
0	8-bit Baud Rate Generator is used

Bit 1 – WUE Wake-up Enable bit

Value	Condition	Description
1	SYNC= 0	Receiver is waiting for a falling edge. Upon falling edge no character will be received and flag RCxIF will be set. WUE will automatically clear after RCxIF is set.
0	SYNC= 0	Receiver is operating normally
X	SYNC= 1	Don't care

Bit 0 – ABDEN Auto-Baud Detect Enable bit

SSEL<4:0>	SMT1 Signal Source	SMT2 Signal Source
01010	CCP3OUT	CCP3OUT
01001	CCP2OUT	CCP2OUT
01000	CCP1OUT	CCP1OUT
00111	TMR6 postscaled output	TMR6 postscaled output
00110	TMR5 overflow	TMR5 overflow
00101	TMR4 postscaled output	TMR4 postscaled output
00100	TMR3 overflow	TMR3 overflow
00011	TMR2 postscaled output	TMR2 postscaled output
00010	TMR1 overflow	TMR1 overflow
00001	TMR0 overflow	TMR0 overflow
00000	Pin Selected by SMT1SIGPPS	Pin Selected by SMT2SIGPPS

Table 37-3. SMT Window Selection

WSEL<4:0>	SMT1 Window Source	SMT2 Window Source
11111-11001	Reserved	Reserved
11000	CCP5OUT	CCP5OUT
10111	NCO1OUT	NCO1OUT
10110	SMT2_overflow	SMT1_overflow
10101	CLKREFOUT	CLKREFOUT
10100	CLC4OUT	CLC4OUT
10011	CLC3OUT	CLC3OUT
10010	CLC2OUT	CLC2OUT
10001	CLC1OUT	CLC1OUT
10000	ZCDOUT	ZCDOUT
01111	C2OUT	C2OUT
01110	C1OUT	C1OUT
01101	PWM7OUT	PWM7OUT
01100	PWM6OUT	PWM6OUT
01011	CCP4OUT	CCP4OUT
01010	CCP3OUT	CCP3OUT
01001	CCP2OUT	CCP2OUT
01000	CCP1OUT	CCP1OUT

Figure 37-3. Gated Timer Mode, Repeat Acquisition Timing Diagram

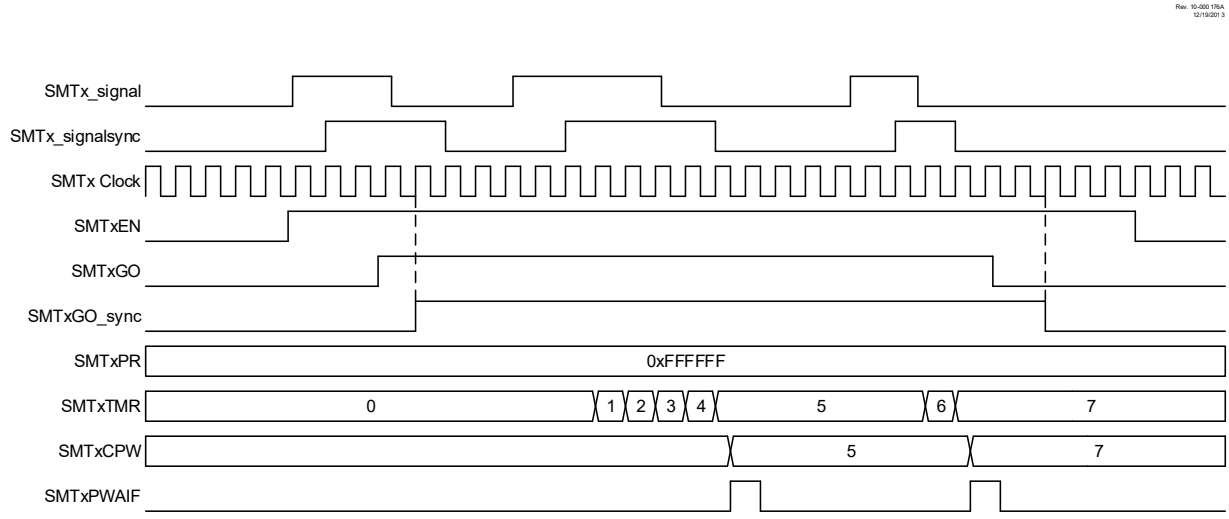
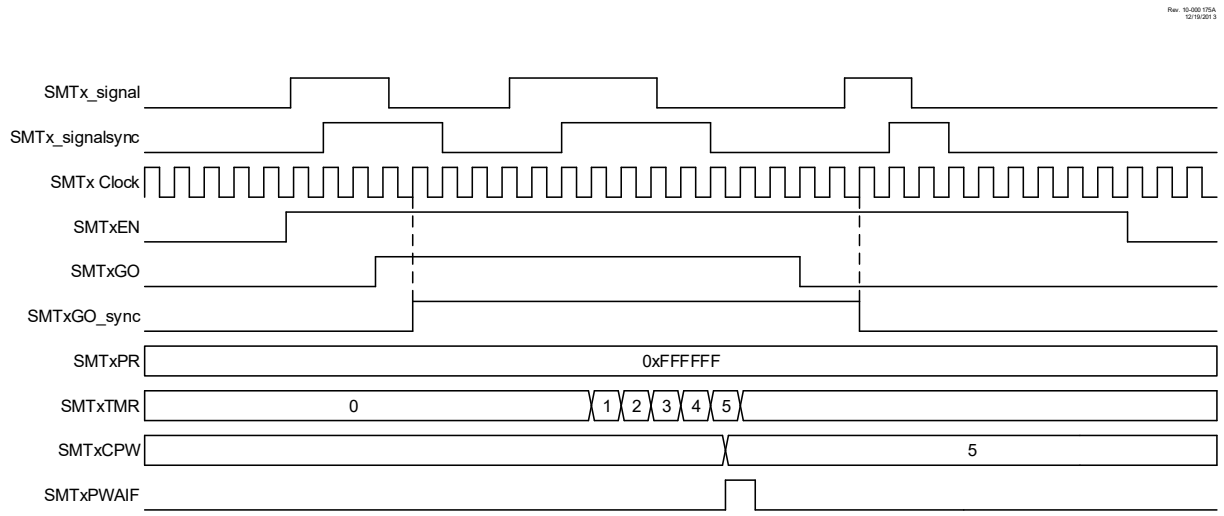


Figure 37-4. Gated Timer Mode, Single Acquisition Timing Diagram



37.1.6.3 Period and Duty Cycle Measurement Mode

In this mode, either the duty cycle or period (depending on polarity) of the input signal can be acquired relative to the SMT clock. The CPW register is updated on a falling edge of the signal, and the CPR register is updated on a rising edge of the signal, along with the SMTxTMR resetting to 0x000001. In addition, the SMTxGO bit is reset on a rising edge when the SMT is in single acquisition mode. See figures below.

Address	Name	Bit Pos.								
0x028E	T2CON	7:0	ON		CKPS[2:0]		OUTPS[3:0]			
0x028F	T2HLT	7:0	PSYNC	CPOL	CSYNC	MODE[4:0]				
0x0290	T2CLKCON	7:0					CS[3:0]			
0x0291	T2RST	7:0					RSEL[3:0]			
0x0292	T4TMR	7:0	TxTMR[7:0]							
0x0293	T4PR	7:0	TxPR[7:0]							
0x0294	T4CON	7:0	ON		CKPS[2:0]		OUTPS[3:0]			
0x0295	T4HLT	7:0	PSYNC	CPOL	CSYNC	MODE[4:0]				
0x0296	T4CLKCON	7:0					CS[3:0]			
0x0297	T4RST	7:0					RSEL[3:0]			
0x0298	T6TMR	7:0	TxTMR[7:0]							
0x0299	T6PR	7:0	TxPR[7:0]							
0x029A	T6CON	7:0	ON		CKPS[2:0]		OUTPS[3:0]			
0x029B	T6HLT	7:0	PSYNC	CPOL	CSYNC	MODE[4:0]				
0x029C	T6CLKCON	7:0					CS[3:0]			
0x029D	T6RST	7:0					RSEL[3:0]			
0x029E	Reserved									
0x029F	ADCPCON0	7:0	CPON							CPRDY
0x02A0 ... 0x02FF	Reserved									
0x0300	INDF0	7:0	INDF0[7:0]							
0x0301	INDF1	7:0	INDF1[7:0]							
0x0302	PCL	7:0	PCL[7:0]							
0x0303	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x0304	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0306	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0308	BSR	7:0			BSR[5:0]					
0x0309	WREG	7:0	WREG[7:0]							
0x030A	PCLATH	7:0		PCLATH[6:0]						
0x030B	INTCON	7:0	GIE	PEIE						INTEDG
0x030C	CCPR1	7:0	CCPRL[7:0]							
		15:8	CCPRH[7:0]							
0x030E	CCP1CON	7:0	EN		OUT	FMT	MODE[3:0]			
0x030F	CCP1CAP	7:0						CTS[2:0]		
0x0310	CCPR2	7:0	CCPRL[7:0]							
		15:8	CCPRH[7:0]							
0x0312	CCP2CON	7:0	EN		OUT	FMT	MODE[3:0]			
0x0313	CCP2CAP	7:0						CTS[2:0]		
0x0314	CCPR3	7:0	CCPRL[7:0]							
		15:8	CCPRH[7:0]							
0x0316	CCP3CON	7:0	EN		OUT	FMT	MODE[3:0]			
0x0317	CCP3CAP	7:0						CTS[2:0]		
0x0318	CCPR4	7:0	CCPRL[7:0]							

44. Packaging Information

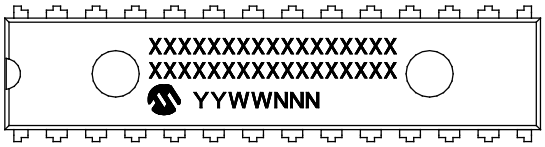
Package Marking Information

Rev. 30-009000A
5/17/2017

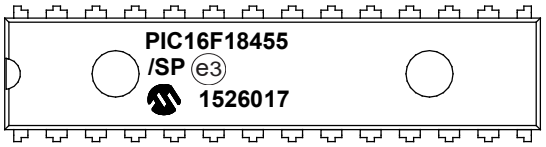
Legend:	XX...X	Customer-specific information or Microchip part number
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	b-free JEDEC ® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

Rev. 30-009028A
5/17/2017

28-Lead SPDIP (.300")

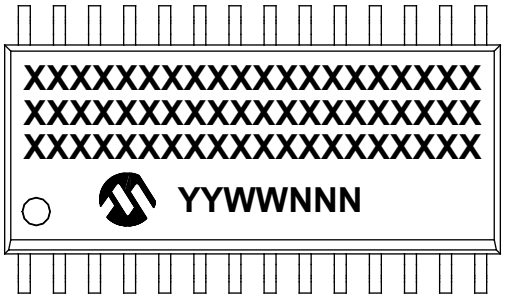


Example



Rev. 30-009028B
5/17/2017

28-Lead SOIC (7.50 mm)



Example