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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18455-e-ss

8.9 Power-up Timer (PWRT)

The Power-up Timer optionally delays device execution after a BOR or POR event. This timer is typically used to allow V_{DD} to stabilize before allowing the device to start running.

The Power-up Timer is controlled by the PWRTS bit field of the Configuration Words.

The Power-up Timer provides a nominal 64 ms timeout on POR or Brown-out Reset.

The device is held in Reset as long as PWRT is active. The PWRT delay allows additional time for the V_{DD} to rise to an acceptable level. The Power-up Timer is enabled by setting a non-zero value in the PWRTS bit field, in Configuration Words.

The Power-up Timer starts after the release of the POR and BOR.

For additional information, refer to Application Note AN607, *"Power-up Trouble Shooting"* (DS00000607).

8.10 Start-up Sequence

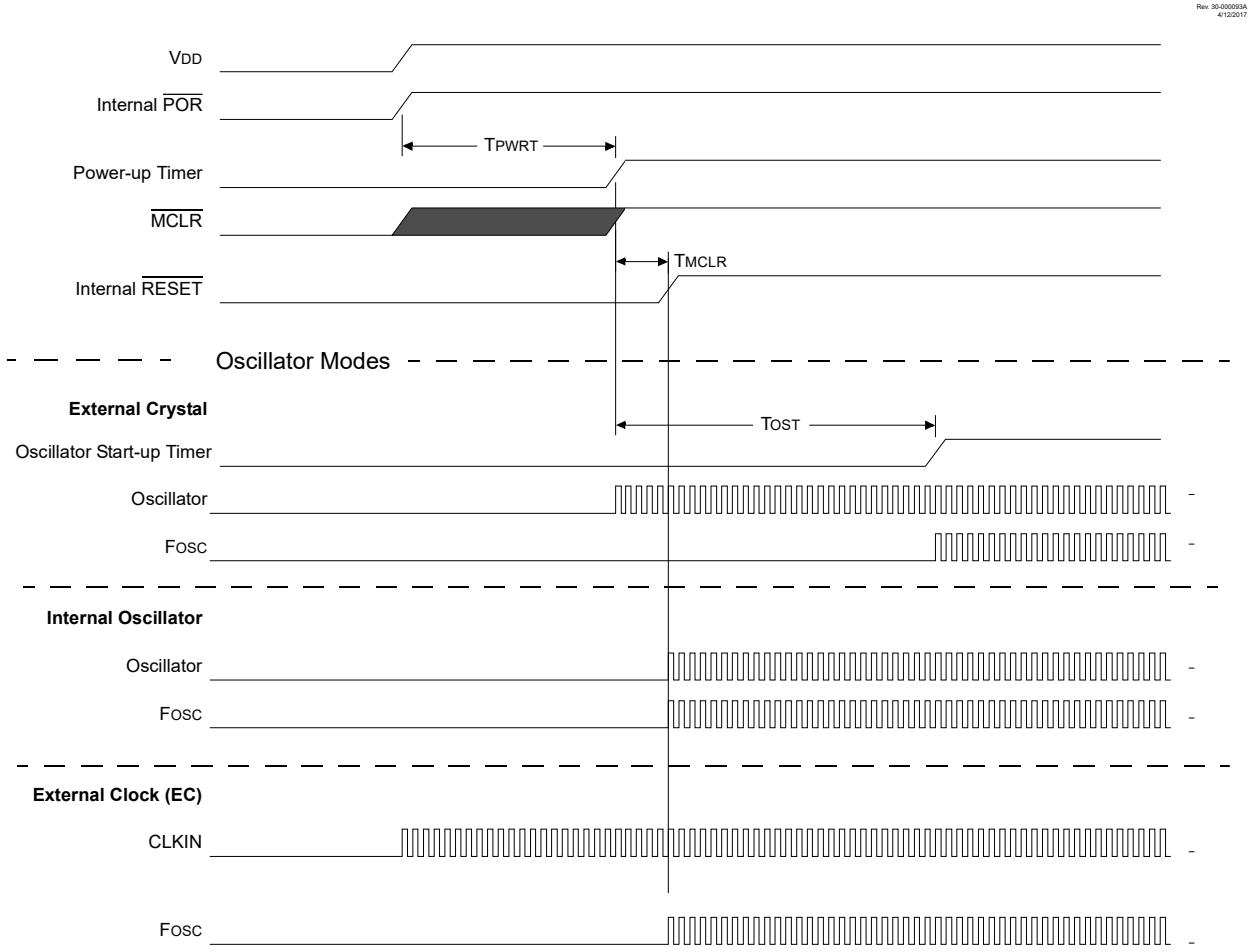
Upon the release of a POR or BOR, the following must occur before the device will begin executing:

1. Power-up Timer runs to completion (if enabled).
2. Oscillator start-up timer runs to completion (if required for selected oscillator source).
3. $\overline{\text{MCLR}}$ must be released (if enabled).

The total timeout will vary based on oscillator configuration and Power-up Timer configuration.

The Power-up Timer and oscillator start-up timer run independently of $\overline{\text{MCLR}}$ Reset. If $\overline{\text{MCLR}}$ is kept low long enough, the Power-up Timer and oscillator Start-up Timer will expire. Upon bringing $\overline{\text{MCLR}}$ high, the device will begin execution after ten F_{OSC} cycles (see figure below). This is useful for testing purposes or to synchronize more than one device operating in parallel.

Figure 8-4. Reset Start-up Sequence



Related Links

9. Oscillator Module (with Fail-Safe Clock Monitor)

8.11 Memory Execution Violation

A Memory Execution Violation Reset occurs if executing an instruction being fetched from outside the valid execution area. The different valid execution areas are defined as follows:

- Flash Memory: The *"Device Sizes and Addresses"* table shows the addresses available on the PIC16(L)F18455/56 devices based on user Flash size. Execution outside this region generates a memory execution violation.
- Storage Area Flash (SAF): If Storage Area Flash (SAF) is enabled , the SAF area is not a valid execution area.

Prefetched instructions that are not executed do not cause memory execution violations. For example, a `GOTO` instruction in the last memory location will prefetch from an invalid location; this is not an error. If an instruction from an invalid location tries to execute, the memory violation is generated immediately, and any concurrent interrupt requests are ignored. When a memory execution violation is generated, the device is reset and flag $\overline{\text{MEMV}}$ is cleared in PCON1 to signal the cause. The flag needs to be set in code after a memory execution violation.

Related Links

8.15.2 PCON0

Name: PCON0
Address: 0x813

Power Control Register 0

Bit	7	6	5	4	3	2	1	0
	STKOVF	STKUNF	$\overline{\text{WDTWV}}$	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
Access	R/W/HS	R/W/HS	R/W/HC	R/W/HC	R/W/HC	R/W/HC	R/W/HC	R/W/HC
Reset	0	0	1	1	1	1	0	q

Bit 7 – STKOVF Stack Overflow Flag bit
Reset States: POR/BOR = 0
All Other Resets = q

Value	Description
1	A Stack Overflow occurred (more CALLs than fit on the stack)
0	A Stack Overflow has not occurred or set to '0' by firmware

Bit 6 – STKUNF Stack Underflow Flag bit
Reset States: POR/BOR = 0
All Other Resets = q

Value	Description
1	A Stack Underflow occurred (more RETURNs than CALLs)
0	A Stack Underflow has not occurred or set to '0' by firmware

Bit 5 – $\overline{\text{WDTWV}}$ Watchdog Window Violation Flag bit
Reset States: POR/BOR = 1
All Other Resets = q

Value	Description
1	A WDT window violation has not occurred or set to '1' by firmware
0	A CLRWDT instruction was issued when the WDT Reset window was closed (set to '0' in hardware when a WDT window violation Reset occurs)

Bit 4 – $\overline{\text{RWDT}}$ WDT Reset Flag bit
Reset States: POR/BOR = 1
All Other Resets = q

Value	Description
1	A WDT overflow/time-out Reset has not occurred or set to '1' by firmware
0	A WDT overflow/time-out Reset has occurred (set to '0' in hardware when a WDT Reset occurs)

Bit 3 – $\overline{\text{RMCLR}}$ $\overline{\text{MCLR}}$ Reset Flag bit
Reset States: POR/BOR = 1
All Other Resets = q

10.7.2 PIE0

Name: PIE0
Address: 0x716

Peripheral Interrupt Enable Register 0

Bit	7	6	5	4	3	2	1	0
			TMR0IE	IOCIE				INTE
Access			R/W	R/W				R/W
Reset			0	0				0

Bit 5 – TMR0IE Timer0 Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 4 – IOCIE Interrupt-on-Change Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 0 – INTE External Interrupt Enable bit(1)

Value	Description
1	Enabled
0	Disabled

Note:

1. The External Interrupt INT pin is selected by INTPPS.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by PIE1-PIE8. Interrupt sources controlled by the PIE0 register do not require PEIE to be set in order to allow interrupt vectoring (when GIE is set).

Related Links

15.9.1 xxxPPS

10.7.4 PIE2

Name: PIE2
Address: 0x718

Peripheral Interrupt Enable Register 2

Bit	7	6	5	4	3	2	1	0
		ZCDIE					C2IE	C1IE
Access		R/W					R/W	R/W
Reset		0					0	0

Bit 6 – ZCDIE Zero-Cross Detect Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bits 0, 1 – CnIE Comparator ‘n’ Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by registers PIE1-PIE8.

16.5.5 PMD4

Name: PMD4
Address: 0x79A

PMD Control Register 4

Bit	7	6	5	4	3	2	1	0
		PWM7MD	PWM6MD	CCP5MD	CCP4MD	CCP3MD	CCP2MD	CCP1MD
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit 6 – PWM7MD Disable Pulse-Width Modulator PWM7 bit

Value	Description
1	PWM7 module disabled
0	PWM7 module enabled

Bit 5 – PWM6MD Disable Pulse-Width Modulator PWM6 bit

Value	Description
1	PWM6 module disabled
0	PWM6 module enabled

Bit 4 – CCP5MD Disable Pulse-Width Modulator CCP5 bit

Value	Description
1	CCP5 module disabled
0	CCP5 module enabled

Bit 3 – CCP4MD Disable Pulse-Width Modulator CCP4 bit

Value	Description
1	CCP4 module disabled
0	CCP4 module enabled

Bit 2 – CCP3MD Disable Pulse-Width Modulator CCP3 bit

Value	Description
1	CCP3 module disabled
0	CCP3 module enabled

Bit 1 – CCP2MD Disable Pulse-Width Modulator CCP2 bit

Value	Description
1	CCP2 module disabled
0	CCP2 module enabled

Bit 0 – CCP1MD Disable Pulse-Width Modulator CCP1 bit

17.6.5 IOCAN

Name: IOCAN
Address: 0x1F3E

Interrupt-on-Change Negative Edge Register Example

Bit	7	6	5	4	3	2	1	0
	IOCAN7	IOCAN6	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 – IOCANn Interrupt-on-Change Negative Edge Enable bits

Value	Description
1	Interrupt-on-Change enabled on the IOCA pin for a negative-going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0	Interrupt-on-Change disabled for the associated pin

20.8.22 ADACT

Name: ADACT
Address: 0x117

ADC AUTO Conversion Trigger Source Selection Register

Bit	7	6	5	4	3	2	1	0
				ACT[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – ACT[4:0] Auto-Conversion Trigger Select Bits

Value	Description
00000 to 11111	See ADC Auto-Conversion Trigger Sources table.

29.1.2 Open-Drain Output Option

When operating in Output mode (the Compare or PWM modes), the drivers for the CCPx pins can be optionally configured as open-drain outputs. This feature allows the voltage level on the pin to be pulled to a higher level through an external pull-up resistor and allows the output to communicate with external circuits without the need for additional level shifters.

29.2 Capture Mode

Capture mode makes use of the 16-bit odd numbered timer resources (Timer1, Timer3, etc.). When an event occurs on the capture source, the 16-bit CCPRx register captures and stores the 16-bit value of the TMRx register. An event is defined as one of the following and is configured by the MODE bits:

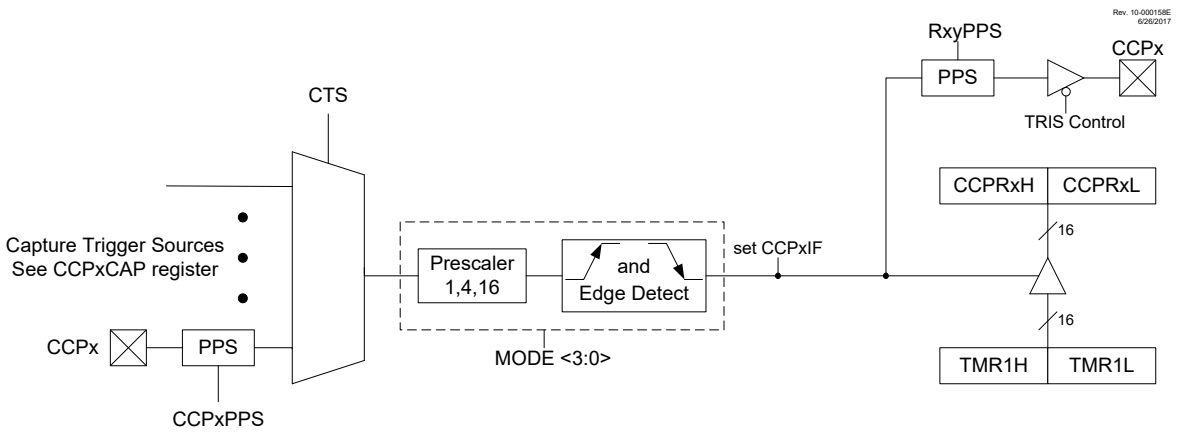
- Every falling edge of CCPx input
- Every rising edge of CCPx input
- Every 4th rising edge of CCPx input
- Every 16th rising edge of CCPx input
- Every edge of CCPx input (rising or falling)

When a capture is made, the Interrupt Request Flag bit CCPxIF of the PIRx register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRx register is read, the old captured value is overwritten by the new captured value.

Important: If an event occurs during a 2-byte read, the high and low-byte data will be from different events. It is recommended while reading the CCPRxH:CCPRxL register pair to either disable the module or read the register pair twice for data integrity.

The following figure shows a simplified diagram of the capture operation.

Figure 29-1. Capture Mode Operation Block Diagram



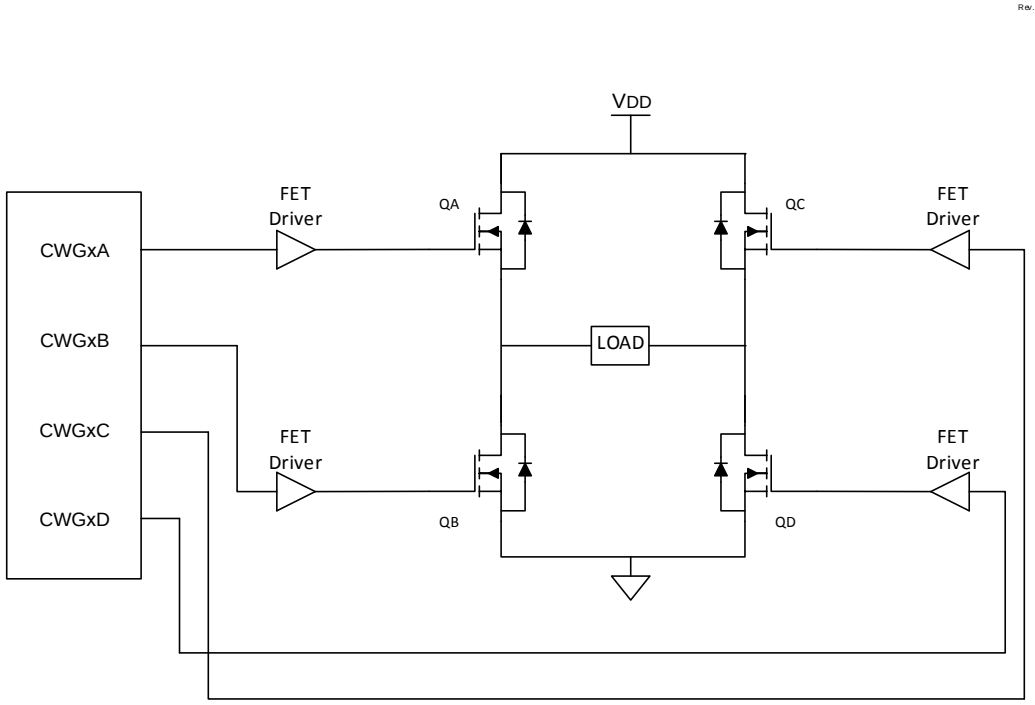
29.2.1 Capture Sources

In Capture mode, the CCPx pin should be configured as an input by setting the associated TRIS control bit.

31.2.3 Full-Bridge Modes

In Forward and Reverse Full-Bridge modes, three outputs drive static values while the fourth is modulated by the input data signal. The mode selection may be toggled between forward and reverse by toggling the MODE<0> bit of the CWGxCON0 while keeping MODE<2:1> static, without disabling the CWG module. When connected, as shown in Figure 31-5, the outputs are appropriate for a full-bridge motor driver. Each CWG output signal has independent polarity control, so the circuit can be adapted to high-active and low-active drivers. A simplified block diagram for the Full-Bridge modes is shown in Figure 31-6.

Figure 31-5. Example of Full-Bridge Application



34.6.1 CLKRCON

Name: CLKRCON
Address: 0x895

Reference Clock Control Register

Bit	7	6	5	4	3	2	1	0
	EN			DC[1:0]		DIV[2:0]		
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			1	0	0	0	0

Bit 7 – EN
Reference Clock Module Enable bit

Value	Description
1	Reference clock module enabled
0	Reference clock module is disabled

Bits 4:3 – DC[1:0]
Reference Clock Duty Cycle bits(1)

Value	Description
11	Clock outputs duty cycle of 75%
10	Clock outputs duty cycle of 50%
01	Clock outputs duty cycle of 25%
00	Clock outputs duty cycle of 0%

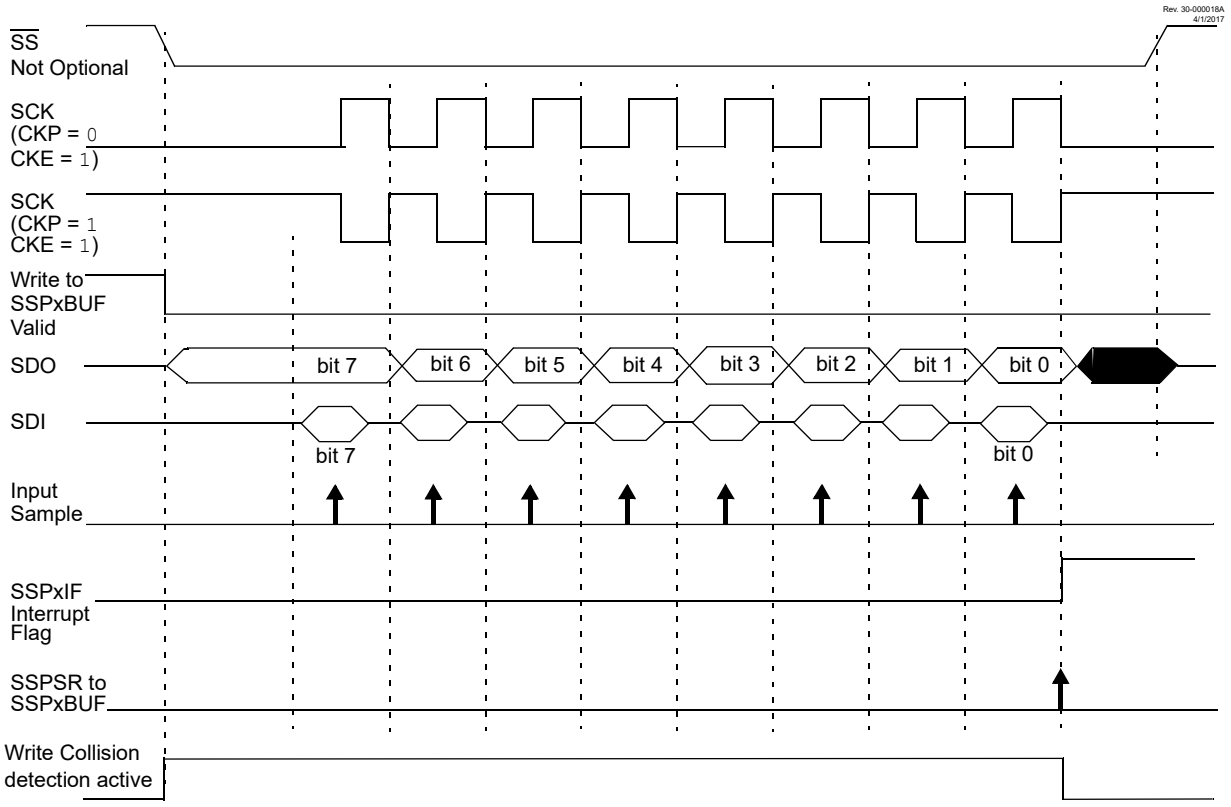
Bits 2:0 – DIV[2:0]
Reference Clock Divider bits

Value	Description
111	Base clock value divided by 128
110	Base clock value divided by 64
101	Base clock value divided by 32
100	Base clock value divided by 16
011	Base clock value divided by 8
010	Base clock value divided by 4
001	Base clock value divided by 2
000	Base clock value

Note:

1. Bits are valid for reference clock divider values of two or larger, the base clock cannot be further divided.

Figure 35-8. SPI Mode Waveform (Slave Mode with CKE = 1)



35.2.5 SPI Operation in Sleep Mode

In SPI Master mode, module clocks may be operating at a different speed than when in Full-Power mode; in the case of the Sleep mode, all clocks are halted.

Special care must be taken by the user when the MSSP clock is much faster than the system clock.

In Slave mode, when MSSP interrupts are enabled, after the master completes sending data, an MSSP interrupt will wake the controller from Sleep.

If an exit from Sleep mode is not desired, MSSP interrupts should be disabled.

In SPI Master mode, when the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all eight bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device.

35.3 I²C Mode Overview

The Inter-Integrated Circuit (I^2C) bus is a multi-master serial data communication bus. Devices communicate in a master/slave environment where the master devices initiate the communication. A

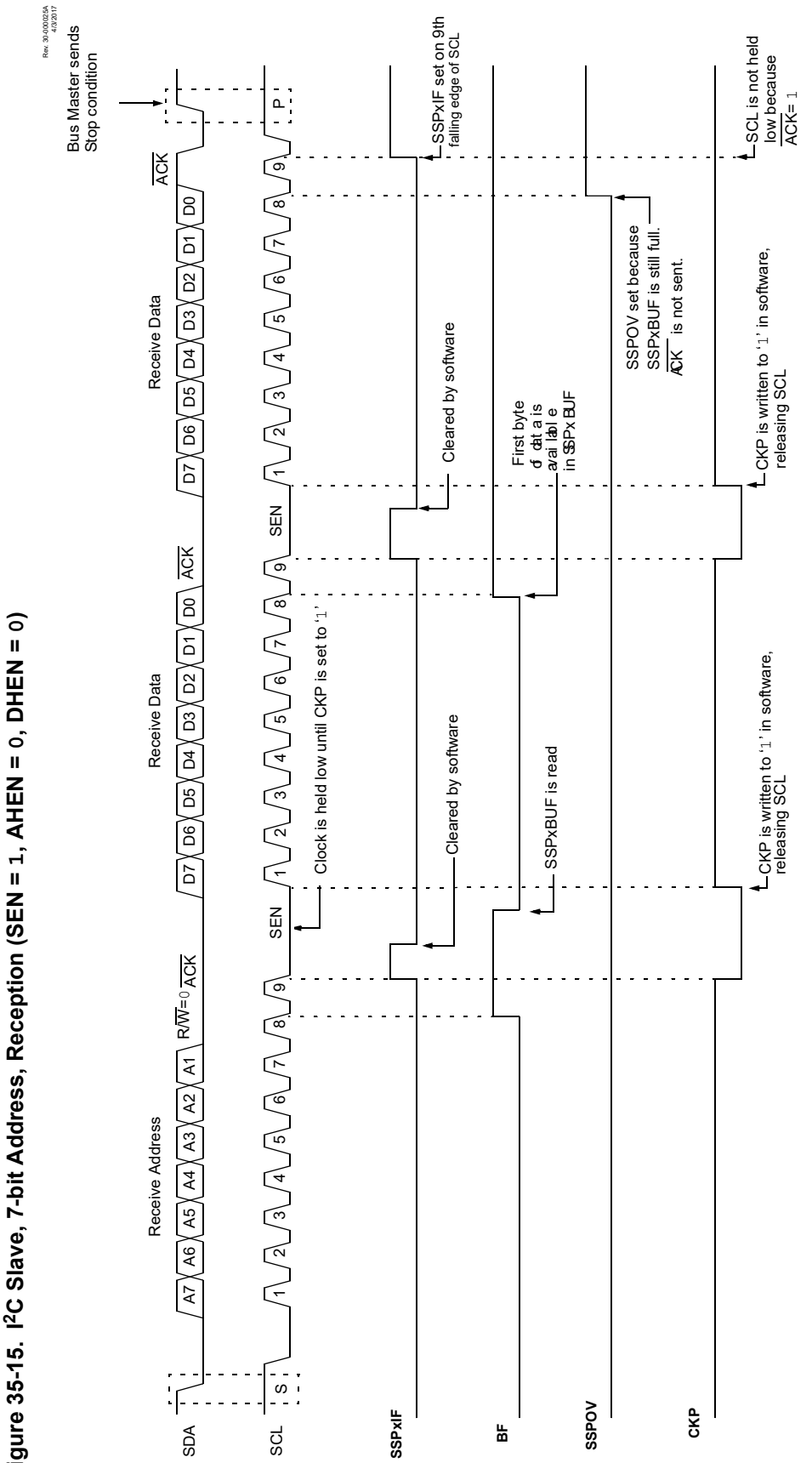


Figure 35-15. I²C Slave, 7-bit Address, Reception (SEN = 1, AHEN = 0, DHEN = 0)

38. Register Summary

Address	Name	Bit Pos.								
0x00	INDF0	7:0	INDF0[7:0]							
0x01	INDF1	7:0	INDF1[7:0]							
0x02	PCL	7:0	PCL[7:0]							
0x03	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x04	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x06	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x08	BSR	7:0			BSR[5:0]					
0x09	WREG	7:0	WREG[7:0]							
0x0A	PCLATH	7:0		PCLATH[6:0]						
0x0B	INTCON	7:0	GIE	PEIE						INTEDG
0x0C	PORTA	7:0	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
0x0D	PORTB	7:0	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
0x0E	PORTC	7:0	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
0x0F	Reserved									
0x10	PORTE	7:0					RE3			
0x11	Reserved									
0x12	TRISA	7:0	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
0x13	TRISB	7:0	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0
0x14	TRISC	7:0	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
0x15 ... 0x17	Reserved									
0x18	LATA	7:0	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0
0x19	LATB	7:0	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0
0x1A	LATC	7:0	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0
0x1B ... 0x7F	Reserved									
0x80	INDF0	7:0	INDF0[7:0]							
0x81	INDF1	7:0	INDF1[7:0]							
0x82	PCL	7:0	PCL[7:0]							
0x83	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x84	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x86	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x88	BSR	7:0			BSR[5:0]					
0x89	WREG	7:0	WREG[7:0]							
0x8A	PCLATH	7:0		PCLATH[6:0]						
0x8B	INTCON	7:0	GIE	PEIE						INTEDG
0x8C	ADLTH	7:0	LTHL[7:0]							

Address	Name	Bit Pos.								
		15:8	LTHH[7:0]							
0x8E	ADUTH	7:0	UTHL[7:0]							
		15:8	UTHH[7:0]							
0x90	ADERR	7:0	ADERRL[7:0]							
		15:8	ERRH[7:0]							
0x92	ADSTPT	7:0	STPTL[7:0]							
		15:8	STPTH[7:0]							
0x94	ADFLTR	7:0	FLTRL[7:0]							
		15:8	FLTRH[7:0]							
0x96	ADACC	7:0	ACCL[7:0]							
		15:8	ACCH[7:0]							
		23:16							ACCU[1:0]	
0x99	ADCNT	7:0	CNT[7:0]							
0x9A	ADRPT	7:0	RPT[7:0]							
0x9B	ADPREV	7:0	PREVL[7:0]							
		15:8	PREVH[7:0]							
0x9D	ADRES	7:0	RESL[7:0]							
		15:8	RESH[7:0]							
0x9F	ADPCH	7:0			PCH[5:0]					
0xA0 ... 0xFF	Reserved									
0x0100	INDF0	7:0	INDF0[7:0]							
0x0101	INDF1	7:0	INDF1[7:0]							
0x0102	PCL	7:0	PCL[7:0]							
0x0103	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x0104	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0106	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0108	BSR	7:0			BSR[5:0]					
0x0109	WREG	7:0	WREG[7:0]							
0x010A	PCLATH	7:0		PCLATH[6:0]						
0x010B	INTCON	7:0	GIE	PEIE						INTEDG
0x010C	ADACQ	7:0	ACQL[7:0]							
		15:8				ACQH[4:0]				
0x010E	ADCAP	7:0				CAP[4:0]				
0x010F	ADPRE	7:0	PREL[7:0]							
		15:8				PREH[4:0]				
0x0111	ADCON0	7:0	ON	CONT		CS		FRM		GO
0x0112	ADCON1	7:0	PPOL	IPEN	GPOL					DSEN
0x0113	ADCON2	7:0	PSIS	CRS[2:0]			ACLR	MD[2:0]		
0x0114	ADCON3	7:0		CALC[2:0]			SOI	TMD[2:0]		
0x0115	ADSTAT	7:0	OV	UTHR	LTHR	MATH		STAT[2:0]		
0x0116	ADREF	7:0				NREF			PREF[1:0]	
0x0117	ADACT	7:0				ACT[4:0]				

Address	Name	Bit Pos.								
0x0118	ADCLK	7:0			CS[5:0]					
0x0119	RC1REG	7:0	RCREG[7:0]							
0x011A	TX1REG	7:0	TXREG[7:0]							
0x011B	SP1BRG	7:0	SPBRGL[7:0]							
		15:8	SPBRGH[7:0]							
0x011D	RC1STA	7:0	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
0x011E	TX1STA	7:0	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
0x011F	BAUD1CON	7:0	ABDOVF	RCIDL		SCKP	BRG16		WUE	ABDEN
0x0120 ... 0x017F	Reserved									
0x0180	INDF0	7:0	INDF0[7:0]							
0x0181	INDF1	7:0	INDF1[7:0]							
0x0182	PCL	7:0	PCL[7:0]							
0x0183	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x0184	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0186	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0188	BSR	7:0			BSR[5:0]					
0x0189	WREG	7:0	WREG[7:0]							
0x018A	PCLATH	7:0		PCLATH[6:0]						
0x018B	INTCON	7:0	GIE	PEIE						INTEDG
0x018C	SSP1BUF	7:0	BUF[7:0]							
0x018D	SSP1ADD	7:0	ADD[7:0]							
0x018E	SSP1MSK	7:0	MSK[6:0]							MSK0
0x018F	SSP1STAT	7:0	SMP	CKE	$\overline{D/A}$	P	S	$\overline{R/W}$	UA	BF
0x0190	SSP1CON1	7:0	WCOL	SSPOV	SSPEN	CKP	SSPM[3:0]			
0x0191	SSP1CON2	7:0	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
0x0192	SSP1CON3	7:0	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
0x0193 ... 0x0195	Reserved									
0x0196	SSP2BUF	7:0	BUF[7:0]							
0x0197	SSP2ADD	7:0	ADD[7:0]							
0x0198	SSP2MSK	7:0	MSK[6:0]							MSK0
0x0199	SSP2STAT	7:0	SMP	CKE	$\overline{D/A}$	P	S	$\overline{R/W}$	UA	BF
0x019A	SSP2CON1	7:0	WCOL	SSPOV	SSPEN	CKP	SSPM[3:0]			
0x019B	SSP2CON2	7:0	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
0x019C	SSP2CON3	7:0	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
0x019D ... 0x01FF	Reserved									
0x0200	INDF0	7:0	INDF0[7:0]							
0x0201	INDF1	7:0	INDF1[7:0]							
0x0202	PCL	7:0	PCL[7:0]							

RETLW	Return literal to W			
Description:	The W register is loaded with the 8-bit literal ‘k’. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.			
Words:	1			
Cycles:	2			

Example:

```
      CALL TABLE            ; W contains table
 ; offset value
 ; W now has
 ; table value
    :
 TABLE
 ADDWF PC             ; W = offset
 RETLW k1             ; Begin table
 RETLW k2             ;
 :
 :
 RETLW kn             ; End of table
```

Before Instruction
W = 07h

After Instruction

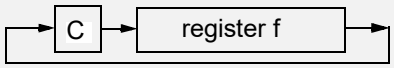
W = value of k8

RETURN	Return from Subroutine			
Syntax:	[*label*] RETURN			
Operands:	None			
Operation:	(TOS) → PC,			
Status Affected:	None			
Encoding:	0000	0000	0001	001s
Description:	Return from subroutine. The stack is POPped and the top of the stack (TOS) is loaded into the Program Counter. This is a 2-cycle instruction.			

RLF	Rotate Left f through Carry
Syntax:	[*label*] RLF f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f<n>) → dest<n + 1>, (f<7>) → C,

RLF	Rotate Left f through Carry			
	(C) → dest<0>			
Status Affected:	C			
Encoding:	0011	01da	ffff	ffff
Description:	The contents of register ‘f’ are rotated one bit to the left through the CARRY flag. If ‘d’ is ‘0’, the result is placed in W. If ‘d’ is ‘1’, the result is stored back in register ‘f’ (default). 			
Words:	1			
Cycles:	1			

Example:	RLF	REG1, 0
Before Instruction REG1 = 1110 0110 C = 0 After Instruction REG = 1110 0110 W = 1100 1100 C = 1		

RRF	Rotate Right f through Carry
Syntax:	[*label*] RRF f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f<n>) → dest<n – 1>, (f<0>) → C, (C) → dest<7>
Status Affected:	C
Description:	The contents of register ‘f’ are rotated one bit to the right through the CARRY flag. If ‘d’ is ‘0’, the result is placed in W. If ‘d’ is ‘1’, the result is placed back in register ‘f’ (default). 

PIC16F18455/56 only									
Standard Operating Conditions (unless otherwise stated), VREGPM = 1									
Param. No.	**Sym.**	**Device Characteristics**	**Min.**	**Typ.†**	**Max. +85°C**	**Max. +125°C**	**Units**	**Conditions**	
								V_{DD}	**Note**
D202	I_{PD_SOSC}	Secondary Oscillator (S_{OSC})	—	0.8	5.5	13	µA	3.0V	
D203	I_{PD_FVR}	FVR	—	28	70	75	µA	3.0V	
D204	I_{PD_BOR}	Brown-out Reset (BOR)	—	14	18	20	µA	3.0V	
D207	I_{PD_ADCA}	ADC - Non-converting	—	0.4	3	12	µA	3.0V	ADC not converting (4)
D208	I_{PD_CMP}	Comparator	—	33	49	57	µA	3.0V	

† - Data in “Typ.” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:

1. The peripheral current is the sum of the base I_{DD} and the additional current consumed when this peripheral is enabled. The peripheral ∆ current can be determined by subtracting the base I_{DD} or I_{PD}current from this limit. Max. values should be used when calculating total current consumption.
2. The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode with all I/O pins in high-impedance state and tied to V_{SS}.
3. All peripheral currents listed are on a per-peripheral basis if more than one instance of a peripheral is available.
4. ADC clock source is FRC.

42.3.4 I/O Ports

Table 42-4.

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Device Characteristics**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
Input Low Voltage							
	V_{IL}	I/O PORT:					
D300		• with TTL buffer	—	—	0.8	V	$4.5V \le V_{DD} \le 5.5V$
D301			—	—	0.15 V_{DD}	V	$1.8V \le V_{DD} \le 4.5V$
D302		• with Schmitt Trigger buffer	—	—	0.2 V_{DD}	V	$2.0V \le V_{DD} \le 5.5V$
D303		• with I^2C levels	—	—	0.3 V_{DD}	V	
D304		• with SMBus levels	—	—	0.8	V	$2.7V \le V_{DD} \le 5.5V$

Standard Operating Conditions (unless otherwise stated)							
Param No.	Sym.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions

1. Flash Memory Cell Endurance for the Flash memory is defined as: One Row Erase operation and one Self-Timed Write.
2. Required only if CONFIG4, bit LVP is disabled.
3. The MPLAB® ICD2 does not support variable V_{PP} output. Circuitry to limit the ICD2 V_{PP} voltage must be placed between the ICD2 and target system when programming or debugging with the ICD2.
4. Refer to the *"PIC16(L)F184XX Memory Programming Specification"* document for description.

Related Links

4.7.4 CONFIG4

42.3.6 Thermal Characteristics

Table 42-6.

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C					
Param No.	Sym.	Characteristic	Typ.	Units	Conditions
TH01	θ_{JA}	Thermal Resistance Junction to Ambient	55	°C/W	28-pin SPDIP package
			74	°C/W	28-pin SOIC package
			67.1	°C/W	28-pin SSOP package
			—	°C/W	28-pin VQFN 4x4 mm package
TH02	θ_{JC}	Thermal Resistance Junction to Case	36	°C/W	28-pin SPDIP package
			19	°C/W	28-pin SOIC package
			23.9	°C/W	28-pin SSOP package
			—	°C/W	28-pin VQFN 4x4 mm package
TH03	T_{JMAX}	Maximum Junction Temperature	—	°C	$T_{JMAX} = T_{AMAX} + (PD_{MAX} \times \theta_{JA})$ **(2)**
TH04	PD	Power Dissipation	—	W	$PD = P_{INTERNAL}+P_{I/O}$
TH05	$P_{INTERNAL}$	Internal Power Dissipation	—	W	$P_{INTERNAL} = I_{DD} \times V_{DD}$ **(1)**
TH06	$P_{I/O}$	I/O Power Dissipation	—	W	$P_{I/O}=\Sigma(I_{OL}*V_{OL})+\Sigma(I_{OH}*(V_{DD}-V_{OH}))$
TH07	P_{DER}	Derated Power	—	W	$P_{DER} = PD_{MAX} (T_J-T_A)/\theta_{JA}$ **(2)**

Note:

1. I_{DD} is current to run the chip alone without driving any load on the output pins.
2. T_A = Ambient Temperature, T_J = Junction Temperature.