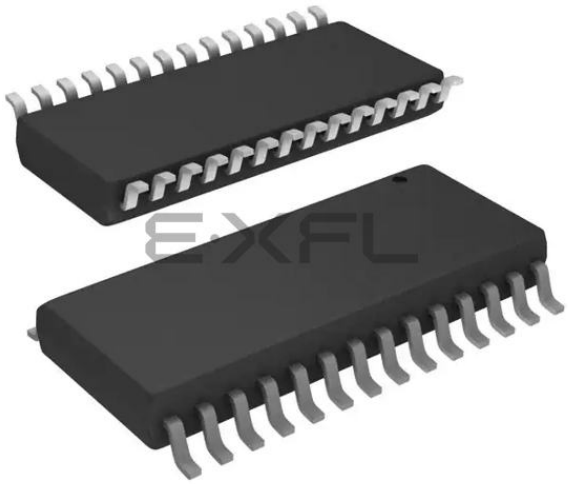

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18456-e-so

4.7.1 CONFIG1

Name: CONFIG1
Address: 0x8007

Configuration word 1

Oscillators

Bit	15	14	13	12	11	10	9	8
			FCMEN		CSWEN			$\overline{\text{CLKOUTEN}}$
Access			R/P	U	R/P	U	U	R/P
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
		RSTOSC[2:0]				FEXTOSC[2:0]		
Access	U	R/P	R/P	R/P	U	R/P	R/P	R/P
Reset	1	1	1	1	1	1	1	1

Bit 13 – FCMEN Fail-Safe Clock Monitor Enable bit

Value	Description
1	FSCM timer enabled
0	FSCM timer disabled

Bit 11 – CSWEN Clock Switch Enable bit

Value	Description
1	Writing to NOSC and NDIV is allowed
0	The NOSC and NDIV bits cannot be changed by user software

Bit 8 – $\overline{\text{CLKOUTEN}}$ Clock Out Enable bit

Value	Condition	Description
1	If FEXTOSC = EC (high, mid or low) or Not Enabled	CLKOUT function is disabled; I/O or oscillator function on OSC2
0	If FEXTOSC = EC (high, mid or low) or Not Enabled	CLKOUT function is enabled; F_{OSC}/4 clock appears at OSC2
	Otherwise	This bit is ignored.

Bits 6:4 – RSTOSC[2:0] Power-up Default Value for COSC bits
This value is the Reset default value for COSC and selects the oscillator first used by user software. Refer to COSC operation.

Value	Description
111	EXTOSC operating per FEXTOSC bits
110	HFINTOSC (1 MHz), with OSCFRQ = '010' (4 MHz) and CDIV = '0010' (4:1)
101	LFINTOSC
100	SOSC
011	Reserved
010	EXTOSC with 4x PLL, with EXTOSC operating per FEXTOSC bits

7.8.12 STKPTR

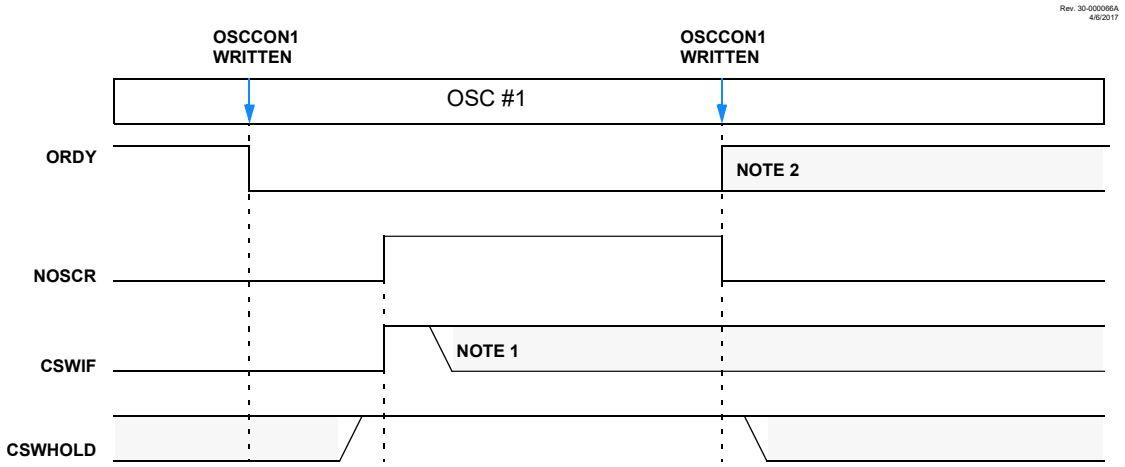
Name: STKPTR
Address: 0x1FED

Stack Pointer Register

Bit	7	6	5	4	3	2	1	0
				STKPTR[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – STKPTR[4:0] Stack Pointer Location bits

Figure 9-8. Clock Switch Abandoned



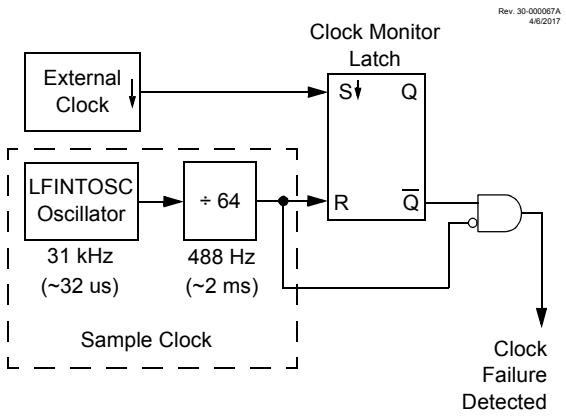
Note:

1. CSWIF may be cleared before or after rewriting OSCCON1; CSWIF is not automatically cleared.
2. ORDY = 0 if OSCCON1 does not match OSCCON2; a new switch will begin.

9.4 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator fail. The FSCM is enabled by setting the FCMEN bit in the Configuration Words. The FSCM is applicable to all external Oscillator modes (LP, XT, HS, ECL/M/H and Secondary Oscillator).

Figure 9-9. FSCM Block Diagram



9.4.1 Fail-Safe Detection

The FSCM module detects a failed oscillator by comparing the external oscillator to the FSCM sample clock. The sample clock is generated by dividing the LFINTOSC by 64. See Figure 9-9. Inside the fail detector block is a latch. The external clock sets the latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is detected when an entire half-cycle of the sample clock elapses before the external clock goes low.

10.7.13 PIR2

Name: PIR2
Address: 0x70E

Peripheral Interrupt Request (Flag) Register 2

Bit	7	6	5	4	3	2	1	0
		ZCDIF					C2IF	C1IF
Access		R/W/HS					R/W/HS	R/W/HS
Reset		0					0	0

Bit 6 – ZCDIF Zero-Cross Detect Interrupt Flag bit

Value	Description
1	An enabled rising and/or falling ZCD1 event has been detected (must be cleared in software)
0	No ZCD1 event has occurred

Bits 0, 1 – CnIF Comparator ‘n’ Interrupt Flag bit

Value	Description
1	Comparator Cn interrupt asserted (must be cleared in software)
0	Comparator Cn interrupt not asserted

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON appropriate interrupt flag bits are clear prior to enabling an interrupt.

11.1.2 Interrupts During Doze

System behavior if an interrupt occurs during DOZE can be configured using the Recover-on-Interrupt (ROI) bit and the Doze-on-Exit (DOE) bit. Refer to the table below for details about system behavior in all cases for a transition from Main to ISR back to Main.

Table 11-1. Interrupts During DOZE

DOZEN	ROI	Code Flow			
		Main	ISR(1)	Return to Main	
0	0	Normal Operation	Normal operation and DOE = DOZEN (in hardware) DOZEN = 0 (unchanged)	If DOE = 1 when return from interrupt: DOZE operation and DOZEN = 1 (in hardware)	If DOE = 0 when return from interrupt: Normal operation and DOZEN = 0 (in hardware)
0	1	Normal Operation	Normal operation and DOE = DOZEN (in hardware) DOZEN = 0 (unchanged)		
1	0	DOZE operation	DOZE operation and DOE = DOZEN (in hardware) DOZEN = 1 (unchanged)		
1	1	DOZE operation	Normal operation and DOE = DOZEN (in hardware) DOZEN = 0 (unchanged)		

Note:

1. User software can change DOE bit in the ISR.

11.2 Sleep Mode

Sleep mode is entered by executing the SLEEP instruction, while the Idle Enable (IDLEN) bit of the CPUDOZE register is clear (IDLEN = 0).

Upon entering Sleep mode, the following conditions exist:

1. WDT will be cleared but keeps running if enabled for operation during Sleep
2. The $\overline{PD}$ bit of the STATUS register is cleared
3. The $\overline{TO}$ bit of the STATUS register is set
4. The CPU clock is disabled
5. LFINTOSC, SOSC, HFINTOSC and ADCRC are unaffected and peripherals using them may continue operation in Sleep.
6. I/O ports maintain the status they had before Sleep was executed (driving high, low, or high-impedance)
7. Resets other than WDT are not affected by Sleep mode

Refer to individual chapters for more details on peripheral operation during Sleep.

12.8.2 WDTCON1

Name: WDTCON1
Address: 0x80D

Watchdog Timer Control Register 1

Bit	7	6	5	4	3	2	1	0
		WDTCS[2:0]				WINDOW[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		q	q	q		q	q	q

Bits 6:4 – WDTCS[2:0] Watchdog Timer Clock Select bits

Value	Description
111 to 010	Reserved
001	MFINTOSC 31.25 kHz
000	LFINTOSC 31 kHz

Bits 2:0 – WINDOW[2:0] Watchdog Timer Window Select bits

WINDOW	Window delay Percent of time	Window opening Percent of time
111	N/A	100
110	12.5	87.5
101	25	75
100	37.5	62.5
011	50	50
010	62.5	37.5
001	75	25
000	87.5	12.5

Note:

1. If WDTCCS in CONFIG3 = 111, the Reset value of WDTCS is '000'.
2. The Reset value (q) of WINDOW is determined by the value of WDTCWS in the CONFIG3 register.
3. If WDTCCS in CONFIG3 ≠ 111, these bits are read-only.
4. If WDTCWS in CONFIG3 ≠ 111, these bits are read-only.

14.7.11 ANSELA

Name: ANSELA
Address: 0x1F38

Analog Select Register

Bit	7	6	5	4	3	2	1	0
	ANSELA7	ANSELA6	ANSELA5	ANSELA4	ANSELA3	ANSELA2	ANSELA1	ANSELA0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 0, 1, 2, 3, 4, 5, 6, 7 – ANSELAn Analog Select on Pins RA<7:0>

Value	Description
1	Digital Input buffers are disabled
0	ST and TTL input buffers are enabled

17.6.5 IOCAN

Name: IOCAN
Address: 0x1F3E

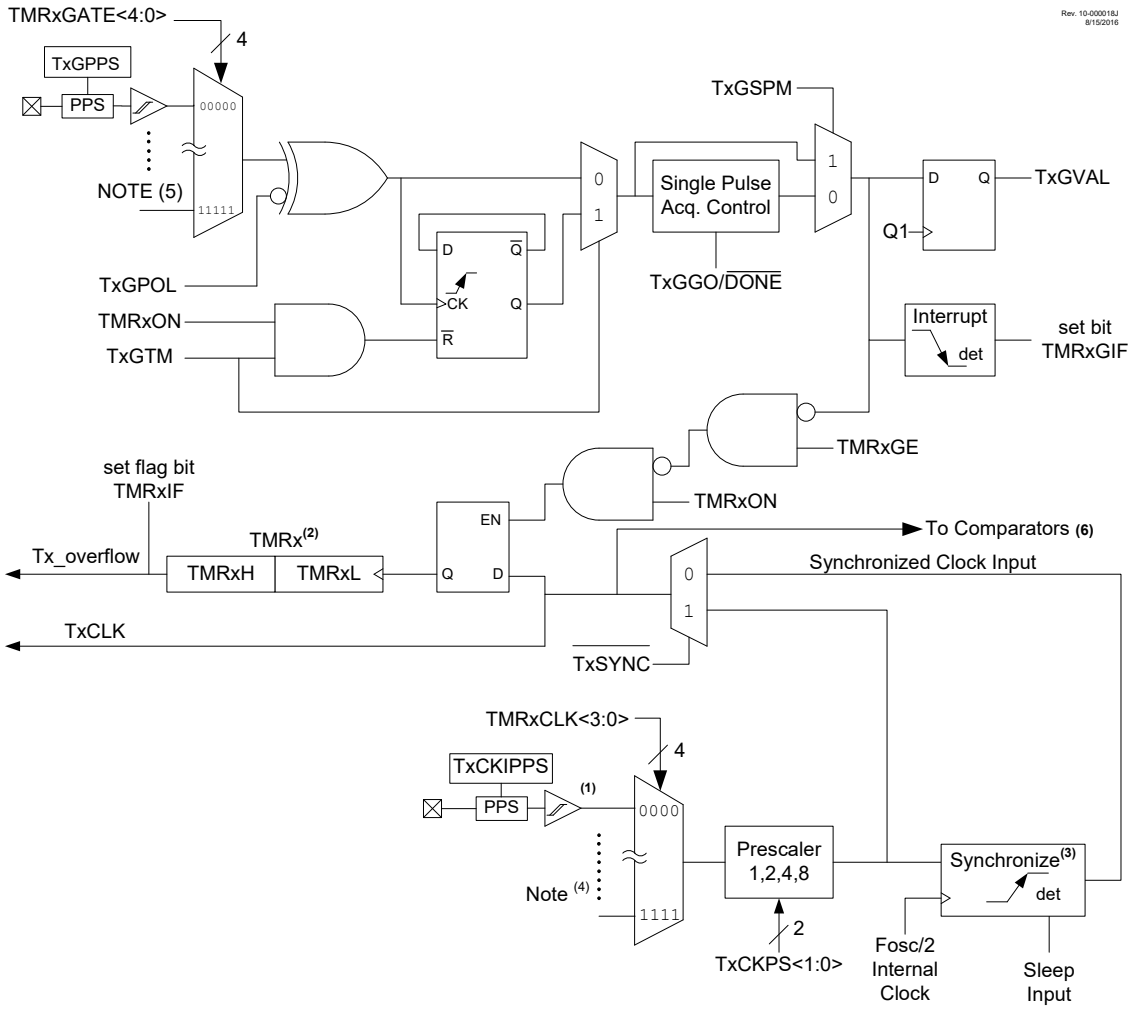
Interrupt-on-Change Negative Edge Register Example

Bit	7	6	5	4	3	2	1	0
	IOCAN7	IOCAN6	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 – IOCANn Interrupt-on-Change Negative Edge Enable bits

Value	Description
1	Interrupt-on-Change enabled on the IOCA pin for a negative-going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0	Interrupt-on-Change disabled for the associated pin

Figure 26-1. Timer1 Block Diagram



Note:

1. This signal comes from the pin seleted by TxCKIPPS.
2. TMRx register increments on rising edge.
3. Synchronize does not operate while in Sleep.
4. See TMRxCLK for clock source selections.
5. See TMRxGATE for gate source selection.
6. Synchronized comparator output should not be used in conjunction with synchronized input clock.

26.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter that is accessed through the TMRxH:TMRxL register pair. Writes to TMRxH or TMRxL directly update the counter.

When used with an internal clock source, the module is a timer and increments on every instruction cycle. When used with an external clock source, the module can be used as either a timer or counter and increments on every selected edge of the external source.

Timer1 is enabled by configuring the ON and GE bits in the TxCON and TxGCON registers, respectively. The table below displays the Timer1 enable selections.

26.13 Register Summary - Timer1

Address	Name	Bit Pos.								
0x020C	TMR1	7:0	TMRxL[7:0]							
		15:8	TMRxH[7:0]							
0x020E	T1CON	7:0			CKPS[1:0]			$\overline{\text{SYNC}}$	RD16	ON
0x020F	T1GCON	7:0	GE	GPOL	GTM	GSPM	GGO/DONE	GVAL		
0x0210	TMR1GATE	7:0				GSS[4:0]				
0x0211	TMR1CLK	7:0				CS[4:0]				
0x0212	TMR3	7:0	TMRxL[7:0]							
		15:8	TMRxH[7:0]							
0x0214	T3CON	7:0			CKPS[1:0]			$\overline{\text{SYNC}}$	RD16	ON
0x0215	T3GCON	7:0	GE	GPOL	GTM	GSPM	GGO/DONE	GVAL		
0x0216	TMR3GATE	7:0				GSS[4:0]				
0x0217	TMR3CLK	7:0				CS[4:0]				
0x0218	TMR5	7:0	TMRxL[7:0]							
		15:8	TMRxH[7:0]							
0x021A	T5CON	7:0			CKPS[1:0]			$\overline{\text{SYNC}}$	RD16	ON
0x021B	T5GCON	7:0	GE	GPOL	GTM	GSPM	GGO/DONE	GVAL		
0x021C	TMR5GATE	7:0				GSS[4:0]				
0x021D	TMR5CLK	7:0				CS[4:0]				

26.14 Register Definitions: Timer1

Long bit name prefixes for the odd numbered timers is shown in the following table. Refer to the *"Long Bit Names"* section for more information.

Table 26-5. Timer1 prefixes

Peripheral	Bit Name Prefix
Timer1	T1
Timer3	T3
Timer5	T5

Related Links

1.4.2.2 Long Bit Names

- External Input

31.11.1.1 Software Generated Shutdown

Setting the SHUTDOWN bit will force the CWG into the shutdown state.

When the auto-restart is disabled, the shutdown state will persist as long as the SHUTDOWN bit is set.

When auto-restart is enabled, the SHUTDOWN bit will clear automatically and resume operation on the next rising edge event. The SHUTDOWN bit indicates when a shutdown condition exists. The bit may be set or cleared in software or by hardware.

31.11.1.2 External Input Source

External shutdown inputs provide the fastest way to safely suspend CWG operation in the event of a Fault condition. When any of the selected shutdown inputs goes active, the CWG outputs will immediately go to the selected override levels without software delay. The override levels are selected by the LSBD and LSAC bits. Several input sources can be selected to cause a shutdown condition. All input sources are active-low. The shutdown input sources are individually enabled by the ASyE bits as shown in the following table:

Table 31-2. Shutdown Sources

ASyE	Source
AS6E	CLC2_out/CLC3_out (low causes shutdown)
AS5E	CMP2_out (low causes shutdown)
AS4E	CMP1_out (low causes shutdown)
AS3E	TMR6_postscaled (high causes shutdown)
AS2E	TMR4_postscaled (high causes shutdown)
AS1E	TMR2_postscaled (high causes shutdown)
AS0E	Pin selected by CWGxPPS (low causes shutdown)

Important: Shutdown inputs are level sensitive, not edge sensitive. The shutdown state cannot be cleared, except by disabling auto-shutdown, as long as the shutdown input level persists.

31.11.1.3 Pin Override Levels

The levels driven to the CWG outputs during an auto-shutdown event are controlled by the LSBD and LSAC bits. The LSBD bits control CWGxB/D output levels, while the LSAC bits control the CWGxA/C output levels.

31.11.1.4 Auto-Shutdown Interrupts

When an auto-shutdown event occurs, either by software or hardware setting SHUTDOWN, the CWGxIF flag bit of the PIRx register is set.

31.11.2 Auto-Shutdown Restart

After an auto-shutdown event has occurred, there are two ways to resume operation:

- Software controlled
- Auto-restart

MDCARL	
CLS<3:0>	Connection
0010	HFINTOSC
0001	F_{OSC} (system clock)
0000	Pin selected by MDCARLPPS

32.4 Carrier Synchronization

During the time when the DSM switches between carrier high and carrier low signal sources, the carrier data in the modulated output signal can become truncated. To prevent this, the carrier signal can be synchronized to the modulator signal. When synchronization is enabled, the carrier pulse that is being mixed at the time of the transition is allowed to transition low before the DSM switches over to the next carrier source.

Synchronization is enabled separately for the carrier high and carrier low signal sources. Synchronization for the carrier high signal is enabled by setting the CHSYNC bit. Synchronization for the carrier low signal is enabled by setting the CLSYNC bit.

The figures below show the timing diagrams of using various synchronization methods.

Figure 32-2. On Off Keying (OOK) Synchronization

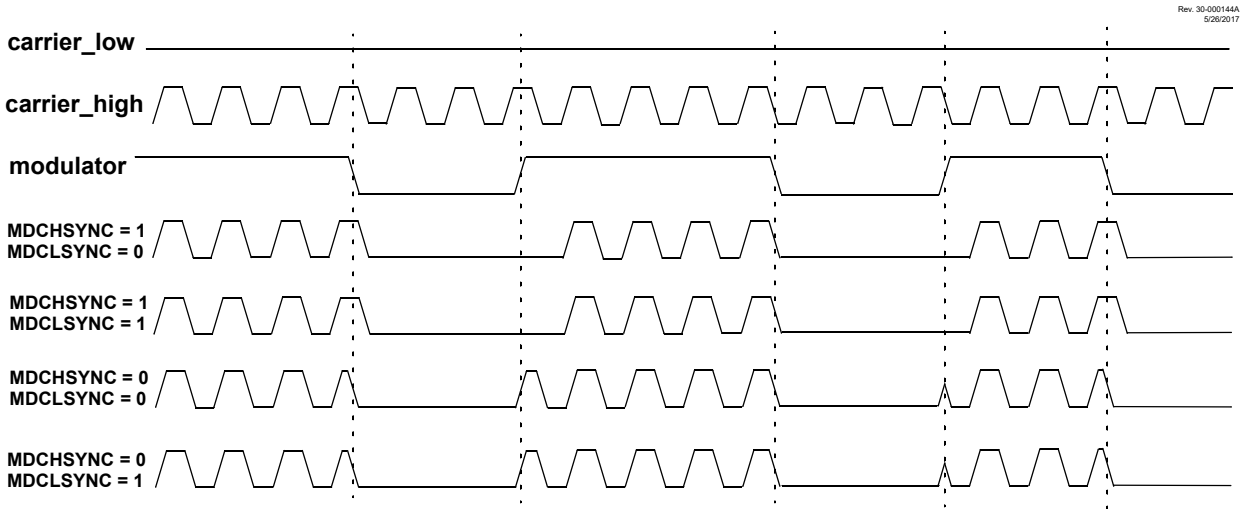
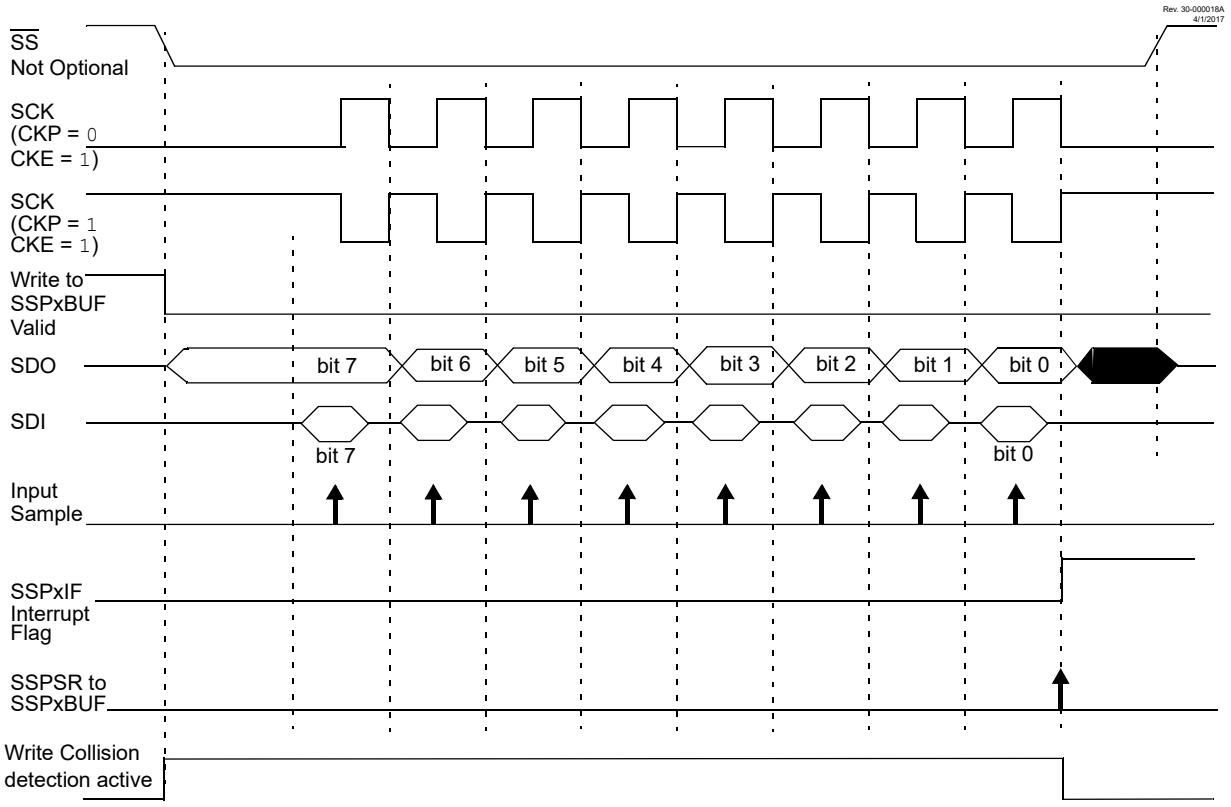


Figure 35-8. SPI Mode Waveform (Slave Mode with CKE = 1)



35.2.5 SPI Operation in Sleep Mode

In SPI Master mode, module clocks may be operating at a different speed than when in Full-Power mode; in the case of the Sleep mode, all clocks are halted.

Special care must be taken by the user when the MSSP clock is much faster than the system clock.

In Slave mode, when MSSP interrupts are enabled, after the master completes sending data, an MSSP interrupt will wake the controller from Sleep.

If an exit from Sleep mode is not desired, MSSP interrupts should be disabled.

In SPI Master mode, when the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all eight bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device.

35.3 I²C Mode Overview

The Inter-Integrated Circuit (I^2C) bus is a multi-master serial data communication bus. Devices communicate in a master/slave environment where the master devices initiate the communication. A

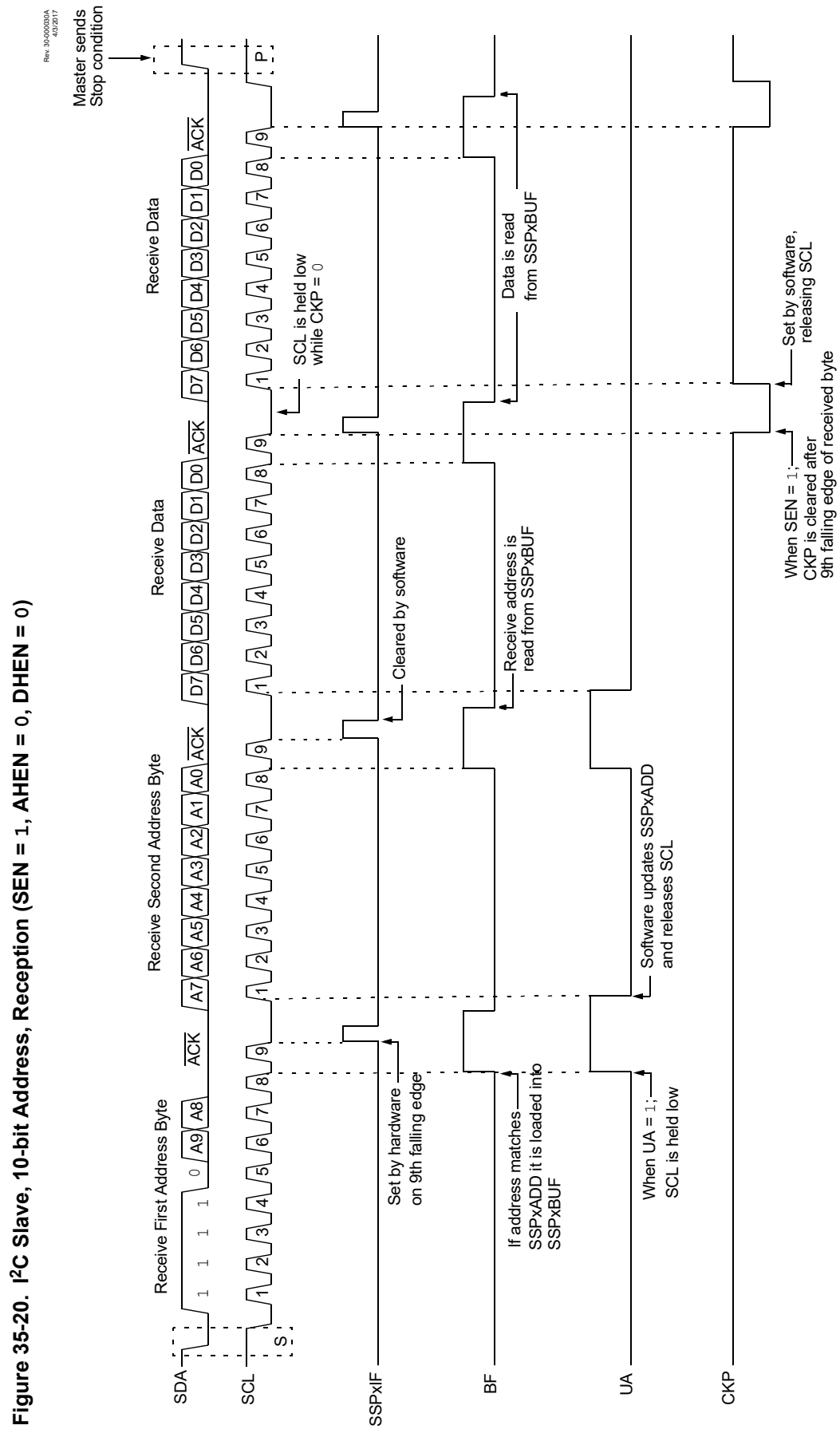


Figure 35-20. I²C Slave, 10-bit Address, Reception (SEN = 1, AHEN = 0, DHEN = 0)

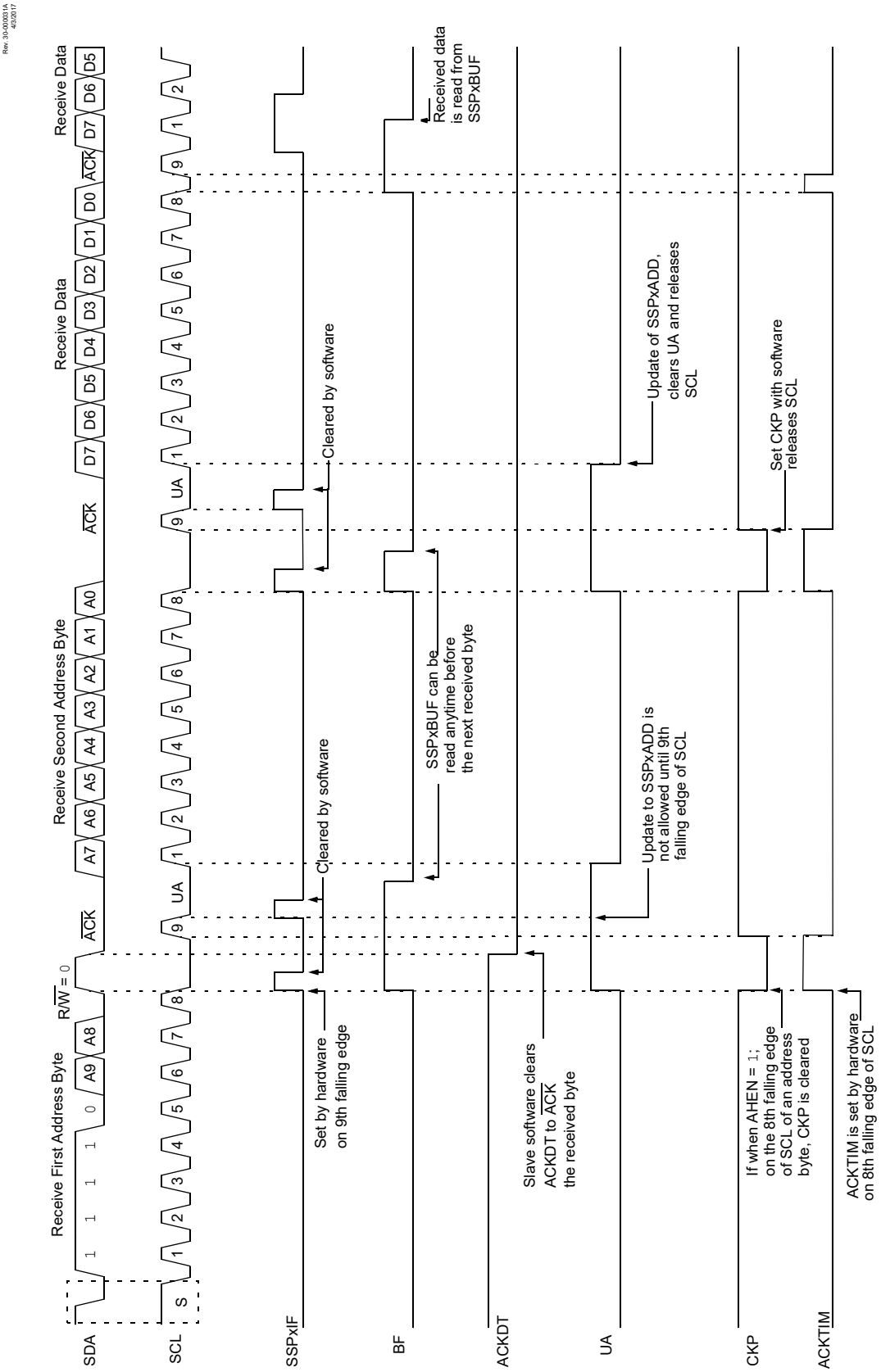


Figure 35-21. I²C Slave, 10-bit Address, Reception (SEN = 0, AHEN = 1, DHEN = 0)

Important: Because queuing of events is not allowed, writing to the lower five bits of SSPxCON2 is disabled until the Start condition is complete.

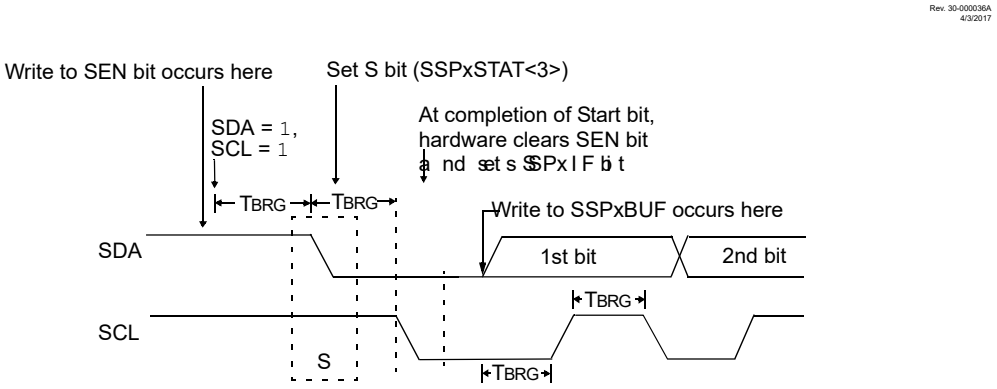
35.6.4 I²C Master Mode Start Condition Timing

To initiate a Start condition (Figure 35-26), the user sets the SEN Start Enable bit. If the SDA and SCL pins are sampled high, the Baud Rate Generator is reloaded with the contents of SSPxADD and starts its count. If SCL and SDA are both sampled high when the Baud Rate Generator times out (T_{BRG}), the SDA pin is driven low. The action of the SDA being driven low while SCL is high is the Start condition and causes the S bit to be set. Following this, the Baud Rate Generator is reloaded with the contents of SSPxADD and resumes its count. When the Baud Rate Generator times out (T_{BRG}), the SEN bit will be automatically cleared by hardware; the Baud Rate Generator is suspended, leaving the SDA line held low and the Start condition is complete.

Important:

1. If at the beginning of the Start condition, the SDA and SCL pins are already sampled low, or if during the Start condition, the SCL line is sampled low before the SDA line is driven low, a bus collision occurs, the Bus Collision Interrupt Flag, BCLxIF, is set, the Start condition is aborted and the I²C module is reset into its Idle state.
2. The Philips I²C specification states that a bus collision cannot occur on a Start.

Figure 35-26. First Start Bit Timing

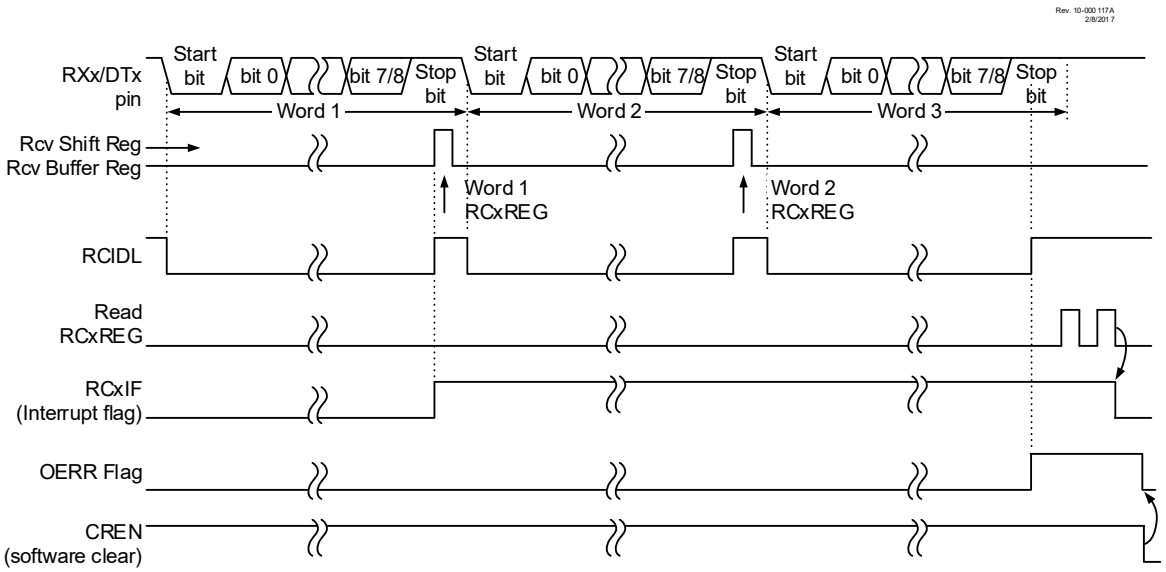


35.6.5 I²C Master Mode Repeated Start Condition Timing

A Repeated Start condition (Figure 35-27) occurs when the RSEN bit is programmed high and the master state machine is no longer active. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (T_{BRG}). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded and begins counting. SDA and SCL must be sampled high for one T_{BRG}. This action is then followed by assertion of the SDA pin (SDA = 0) for one T_{BRG} while SCL is high. SCL is asserted low. Following this, the RSEN bit will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on

5. If interrupts are desired, set the RCxIE bit of the PIEx register and the GIE and PEIE bits of the INTCON register.
6. Enable 9-bit reception by setting the RX9 bit.
7. Enable address detection by setting the ADDEN bit.
8. Enable reception by setting the CREN bit.
9. The RCxIF interrupt flag bit will be set when a character with the ninth bit set is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCxIE interrupt enable bit is also set.
10. Read the RCxSTA register to get the error flags. The ninth data bit will always be set.
11. Get the received eight Least Significant data bits from the receive buffer by reading the RCxREG register. Software determines if this is the device's address.
12. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.
13. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and generate interrupts.

Figure 36-5. Asynchronous Reception



Note: This timing diagram shows three bytes appearing on the RXx input. The OERR flag is set because the RCxREG is not read before the third word is received.

36.1.3 Clock Accuracy with Asynchronous Operation

The factory calibrates the internal oscillator block output (INTOSC). However, the INTOSC frequency may drift as V_{DD} or temperature changes, and this directly affects the asynchronous baud rate. Two methods may be used to adjust the baud rate clock, but both require a reference clock source of some kind.

The first (preferred) method uses the OSCTUNE register to adjust the INTOSC output. Adjusting the value in the OSCTUNE register allows for fine resolution changes to the system clock source.

The other method adjusts the value in the Baud Rate Generator. This can be done automatically with the Auto-Baud Detect feature (see 36.2.1 Auto-Baud Detect). There may not be fine enough resolution when adjusting the Baud Rate Generator to compensate for a gradual change in the peripheral clock frequency.

MOVIW	Move INDFn to W		
Status Affected:	Z		
	MODE	**SYNTAX**	**mm**
	Preincrement	++FSRn	00
	Predecrement	--FSRn	01
	Postincrement	FSRn++	10
	Postdecrement	FSRn--	11
Description:	This instruction is used to move data between W and one of the indirect registers (INDFn). Before/after this move, the pointer (FSRn) is updated by pre/post incrementing/ decrementing it. The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn. FSRn is limited to the range 0000h - FFFFh. Incrementing/decrementing it beyond these bounds will cause it to wrap-around.		

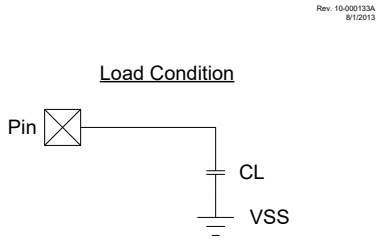
MOVLB	Move literal to BSR
Syntax:	[*label*] MOVLB k
Operands:	0 ≤ k ≤ 127
Operation:	k → BSR
Status Affected:	None
Description:	The 6-bit literal ‘k’ is loaded into the Bank Select Register (BSR).

MOVLP	Move literal to PCLATH
Syntax:	[*label*] MOVLP k
Operands:	0 ≤ k ≤ 127
Operation:	k → PCLATH
Status Affected:	None
Description:	The 7-bit literal ‘k’ is loaded into the PCLATH register.

MOVLW	Move literal to W
Syntax:	[*label*] MOVLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W)
Status Affected:	None

42.4 AC Characteristics

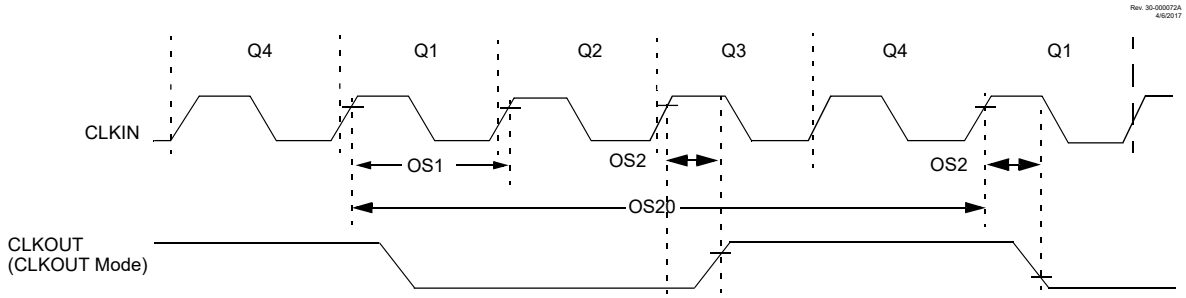
Figure 42-4. Load Conditions



Legend: CL=50 pF for all pins

42.4.1 External Clock/Oscillator Timing Requirements

Figure 42-5. Clock Timing



Note: See table below.

Table 42-7.

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ. †**	**Max.**	**Units**	**Conditions**
ECL Oscillator							
OS1	F_{ECL}	Clock Frequency	—	—	500	kHz	
OS2	T_{ECL_DC}	Clock Duty Cycle	40	—	60	%	
ECM Oscillator							
OS3	F_{ECM}	Clock Frequency	—	—	4	MHz	
OS4	T_{ECM_DC}	Clock Duty Cycle	40	—	60	%	
ECH Oscillator							
OS5	F_{ECH}	Clock Frequency	—	—	32	MHz	
OS6	T_{ECH_DC}	Clock Duty Cycle	40	—	60	%	
LP Oscillator							
OS7	F_{LP}	Clock Frequency	—	—	100	kHz	**Note 4**

45. Revision History

Date	Revision	Comment
5/2018	A	Initial release of this document.
6/2018	B	Minor corrections to electrical specs and removed EOL packages QFN and UQFN.