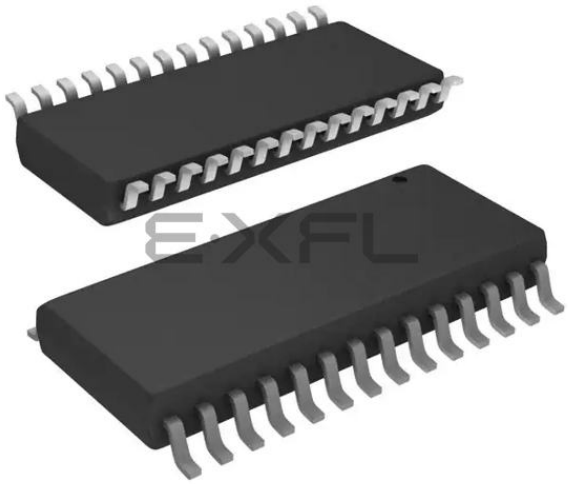

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18456-i-so

4.7.5 CONFIG5

Name: CONFIG5
Address: 0x800B

Configuration Word 5

Code Protection

Bit	15	14	13	12	11	10	9	8
Access			U	U	U	U	U	U
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
								$\overline{CP}$
Access	U	U	U	U	U	U	U	R/P
Reset	1	1	1	1	1	1	1	1

Bit 0 – $\overline{CP}$ Program Flash Memory Code Protection bit

Value	Description
1	Program Flash Memory code protection disabled
0	Program Flash Memory code protection enabled

4.8 Register Summary - Device and Revision

Offset	Name	Bit Pos.								
0x8005	REVISION ID	7:0	MJRREV[1:0]		MNRREV[5:0]					
		13:8			1	0	MJRREV[5:2]			
0x8006	DEVICE ID	7:0	DEV[7:0]							
		13:8			1	1	DEV[11:8]			

4.9 Register Definitions: Device and Revision

7.8.8 WREG

Name: WREG
Address: 0x09 + n*0x80 [n=0..63]

Working Data Register

Bit	7	6	5	4	3	2	1	0
	WREG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – WREG[7:0]

Related Links

7.3.2 Core Registers

Value	Description
1	The PLL is ready to be used
0	The PLL is not enabled, the required input source is not ready, or the PLL is not locked.

14.6 Register Summary - Input/Output

Address	Name	Bit Pos.								
0x0C	PORTA	7:0	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
0x0D	PORTB	7:0	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
0x0E	PORTC	7:0	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
0x0F	Reserved									
0x10	PORTE	7:0					RE3			
0x11	Reserved									
0x12	TRISA	7:0	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
0x13	TRISB	7:0	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0
0x14	TRISC	7:0	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
0x15 ... 0x17	Reserved									
0x18	LATA	7:0	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0
0x19	LATB	7:0	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0
0x1A	LATC	7:0	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0
0x1B ... 0x1F37	Reserved									
0x1F38	ANSELA	7:0	ANSELA7	ANSELA6	ANSELA5	ANSELA4	ANSELA3	ANSELA2	ANSELA1	ANSELA0
0x1F39	WPUA	7:0	WPUA7	WPUA6	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0
0x1F3A	ODCONA	7:0	ODCA7	ODCA6	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0
0x1F3B	SLRCONA	7:0	SLRA7	SLRA6	SLRA5	SLRA4	SLRA3	SLRA2	SLRA1	SLRA0
0x1F3C	INLVLA	7:0	INLVLA7	INLVLA6	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0
0x1F3D ... 0x1F42	Reserved									
0x1F43	ANSELB	7:0	ANSELB7	ANSELB6	ANSELB5	ANSELB4	ANSELB3	ANSELB2	ANSELB1	ANSELB0
0x1F44	WPUB	7:0	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0
0x1F45	ODCONB	7:0	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0
0x1F46	SLRCONB	7:0	SLRB7	SLRB6	SLRB5	SLRB4	SLRB3	SLRB2	SLRB1	SLRB0
0x1F47	INLVLB	7:0	INLVLB7	INLVLB6	INLVLB5	INLVLB4	INLVLB3	INLVLB2	INLVLB1	INLVLB0
0x1F48 ... 0x1F4D	Reserved									
0x1F4E	ANSELC	7:0	ANSELC7	ANSELC6	ANSELC5	ANSELC4	ANSELC3	ANSELC2	ANSELC1	ANSELC0
0x1F4F	WPUC	7:0	WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0
0x1F50	ODCONC	7:0	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0
0x1F51	SLRCONC	7:0	SLRC7	SLRC6	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0
0x1F52	INLVLC	7:0	INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0
0x1F53 ... 0x1F64	Reserved									
0x1F65	WPUE	7:0					WPUE3			
0x1F66	Reserved									

20.8.11 ADCAP

Name: ADCAP
Address: 0x10E

ADC Additional Sample Capacitor Selection Register

Bit	7	6	5	4	3	2	1	0
				CAP[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – CAP[4:0] ADC Additional Sample Capacitor Selection bits

Value	Description
1 to 31	Number of pF in the additional capacitance
0	No additional capacitance

20.8.16 ADPREV

Name: ADPREV
Address: 0x09B

ADC Previous Result Register

Bit	15	14	13	12	11	10	9	8
	PREVH[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	x	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	PREVL[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	x	x	x	x	x	x	x	x

Bits 15:8 – PREVH[7:0] Previous ADC Result Most Significant bits

Value	Condition	Description
0 to 0xFF	PSIS = 1	Upper byte of ADFLTR at the start of current ADC conversion
varies	PSIS = 0	Upper bits of ADRES at the start of current ADC conversion(1)

Bits 7:0 – PREVL[7:0] Previous ADC Result Least Significant bits

Value	Condition	Description
0 to 0xFF	PSIS = 1	Lower byte of ADFLTR at the start of current ADC conversion
varies	PSIS = 0	Lower bits of ADRES at the start of current ADC conversion(1)

Note: If PSIS = 0, PREVH and PREVL are formatted the same way as ADRES is, depending on the FRM bit.

20.8.17 ADACC

Name: ADACC
Address: 0x096

ADC Accumulator Register
See Computation Modes for more details.

Bit	23	22	21	20	19	18	17	16
							ACCU[1:0]	
Access							R/W	R/W
Reset							x	x

Bit	15	14	13	12	11	10	9	8
	ACCH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	ACCL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 17:16 – ACCU[1:0]
ADC Accumulator MSB. Upper two bits of accumulator value.

Bits 15:8 – ACCH[7:0]
ADC Accumulator middle bits. Higher eight bits of accumulator value.

Bits 7:0 – ACCL[7:0]
ADC Accumulator LSB. Lower eight bits of accumulator value.

21.2 Ratiometric Output Level

The DAC output value is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage reference input source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.

The value of the individual resistors within the ladder can be found in the *"5-Bit DAC Specifications"* table from the *"Electrical Specifications"* chapter.

Related Links

42.4.10 5-Bit DAC Specifications

21.3 DAC Voltage Reference Output

The unbuffered DAC voltage can be output to the DACxOUTn pin(s) by setting the respective OEn bit(s). Selecting the DAC reference voltage for output on either DACxOUTn pin automatically overrides the digital output buffer, the weak pull-up and digital input threshold detector functions of that pin.

Reading the DACxOUTn pin when it has been configured for DAC reference voltage output will always return a '0'.

Important: The unbuffered DAC output (DACxOUTn) is not intended to drive an external load.

21.4 Operation During Sleep

When the device wakes up from Sleep through an interrupt or a Windowed Watchdog Timer Time-out, the contents of the DACxCON0 register are not affected. To minimize current consumption in Sleep mode, the voltage reference should be disabled.

21.5 Effects of a Reset

A device Reset affects the following:

- DACx is disabled.
- DACx output voltage is removed from the DACxOUTn pin(s).
- The DAC1R range select bits are cleared.

7. When TxTMR = TxPR, the next clock clears TxTMR, regardless of the operating mode.

- T2TMR is cleared
- The PWM output is active. (Exception: When the PWM duty cycle = 0%, the PWM output will remain inactive.)
- The PWMxDCH and PWMxDCL register values are latched into the buffers.

Important: The Timer2 postscaler has no effect on the PWM operation.

30.4 PWM Duty Cycle

The PWM duty cycle is specified by writing a 10-bit value to the PWMxDCH and PWMxDCL register pair. The PWMxDCH register contains the eight MSbs and the PWMxDCL<7:6>, the two LSbs. The PWMxDCH and PWMxDCL registers can be written to at any time.

The formulas below are used to calculate the PWM pulse width and the PWM duty cycle ratio.

Equation 30-2. Pulse Width

$$PulseWidth = (PWMxDCH{:}PWMxDCL<7{:}6>) \bullet Tosc \bullet (TMR2\mathrm{P}rescaleValue)$$

Note: $T_{OSC} = 1/F_{OSC}$

Equation 30-3. Duty Cycle Ratio

$$DutyCycleRatio = \frac{(PWMxDCH{:}PWMxDCL<7{:}6>)}{4(T2PR+1)}$$

The 8-bit timer T2TMR register is concatenated with the two Least Significant bits of $1/F_{OSC}$, adjusted by the Timer2 prescaler to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

30.5 PWM Resolution

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is ten bits when T2PR is 255. The resolution is a function of the T2PR register value as shown below.

Equation 30-4. PWM Resolution

$$\mathrm{R}esolution = \frac{\log[4(T2PR+1)]}{\log(2)} bits$$

Important: If the pulse-width value is greater than the period, the assigned PWM pin(s) will remain unchanged.

32.12.2 MDxCON1

Name: MDxCON1
Address: 0x0898

Modulation Control Register 1

Bit	7	6	5	4	3	2	1	0
			CHPOL	CHSYNC			CLPOL	CLSYNC
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit 5 – CHPOL Modulator High Carrier Polarity Select bit

Value	Description
1	Selected high carrier signal is inverted
0	Selected high carrier signal is not inverted

Bit 4 – CHSYNC Modulator High Carrier Synchronization Enable bit

Value	Description
1	Modulator waits for a falling edge on the high time carrier signal before allowing a switch to the low time carrier
0	Modulator output is not synchronized to the high time carrier signal

Bit 1 – CLPOL Modulator Low Carrier Polarity Select bit

Value	Description
1	Selected low carrier signal is inverted
0	Selected low carrier signal is not inverted

Bit 0 – CLSYNC Modulator Low Carrier Synchronization Enable bit

Value	Description
1	Modulator waits for a falling edge on the low time carrier signal before allowing a switch to the high time carrier
0	Modulator output is not synchronized to the low time carrier signal

Note:

1. Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

32.12.3 MDxCARH

Name: MDxCARH
Address: 0x089B

Modulation High Carrier Control Register

Bit	7	6	5	4	3	2	1	0
					CHS[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – CHS[3:0] Modulator Carrier High Selection bits

Table 32-5. MDCARH Source Selections

MDCARH	
CHS<3:0>	**Connection**
1111	CCP5 OUT
1110	CLC4 OUT
1101	CLC3 OUT
1100	CLC2 OUT
1011	CLC1 OUT
1010	NCO1 OUT
1001	PWM7 OUT
1000	PWM6 OUT
0111	CCP4 OUT
0110	CCP3 OUT
0101	CCP2 OUT
0100	CCP1 OUT
0011	CLKREF output
0010	HFINTOSC
0001	F_{OSC} (system clock)
0000	Pin selected by MDCARHPPS

33.8.11 CLCDATA

Name: CLCDATA
Address: 0x1E0F

CLC Data Ouput Register

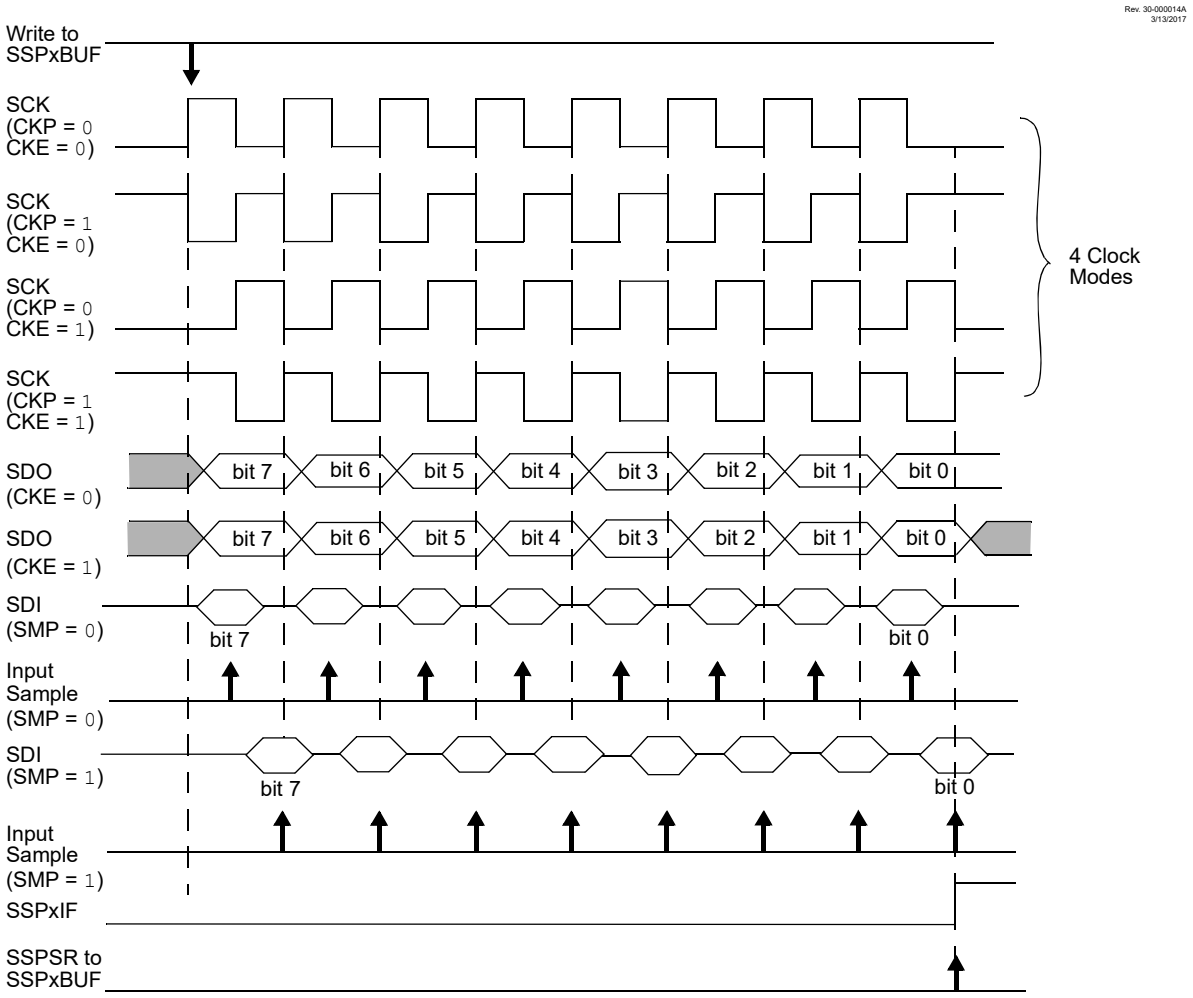
Mirror copy of

Bit	7	6	5	4	3	2	1	0
					MLC4OUT	MLC3OUT	MLC2OUT	MLC1OUT
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 0, 1, 2, 3 – MLCxOUT
Mirror copy of CLCx_out bit

Value	Description
1	CLCx_out is 1
0	CLCx_out is 0

Figure 35-4. SPI Mode Waveform (Master Mode)



35.2.2 SPI Slave Mode

In Slave mode, the data is transmitted and received as external clock pulses appear on SCK. When the last bit is latched, the SSPxIF interrupt flag bit is set.

Before enabling the module in SPI Slave mode, the clock line must match the proper Idle state. The clock line can be observed by reading the SCK pin. The Idle state is determined by the CKP bit.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in Sleep mode, the slave can transmit/receive data. The shift register is clocked from the SCK pin input and when a byte is received, the device will generate an interrupt. If enabled, the device will wake-up from Sleep.

35.2.3 Daisy-Chain Configuration

The SPI bus can sometimes be connected in a daisy-chain configuration. The first slave output is connected to the second slave input, the second slave output is connected to the third slave input, and so on. The final slave output is connected to the master input. Each slave sends out, during a second group of clock pulses, an exact copy of what was received during the first group of clock pulses. The whole

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the Global Interrupt Enable (GIE) bit is also set then the Interrupt Service Routine at address 0004h will be called.

Value	Condition	Description
1	SYNC= 0	High speed, if BRG16 = 1, baud rate is baudclk/4; else baudclk/16
0	SYNC= 0	Low speed
X	SYNC= 1	Don't care

Bit 1 – TRMT Transmit Shift Register (TSR) Status bit

Value	Description
1	TSR is empty
0	TSR is not empty

Bit 0 – TX9D Ninth bit of Transmit Data
Can be address/data bit or a parity bit.

Note:

1. SREN and CREN bits override TXEN in Sync mode.

37.3.3 SMTxSTAT

Name: SMTxSTAT
Address: 0x49A,0x51A

SMT Status Register

Bit	7	6	5	4	3	2	1	0
	CPRUP	CPWUP		RST		TS	WS	AS
Access	R/W/HC	R/W/HC		R/W		RO	RO	RO
Reset	0	0		0		0	0	0

Bit 7 – CPRUP SMT Manual Period Buffer Update bit

Value	Description
1	Request update to SMTxCPR registers
0	SMTxCPR registers update is complete

Bit 6 – CPWUP SMT Manual Pulse Width Buffer Update bit

Value	Description
1	Request update to SMTxCPW registers
0	SMTxCPW registers update is complete

Bit 4 – RST SMT Manual Timer Reset bit

Value	Description
1	Request Reset to SMTxTMR registers
0	SMTxTMR registers update is complete

Bit 2 – TS SMT GO Value Status bit

Value	Description
1	SMTxTMR is incrementing
0	SMTxTMR is not incrementing

Bit 1 – WS SMT Window Status bit

Value	Description
1	SMT window is open
0	SMT window is closed

Bit 0 – AS SMT Signal Value Status bit

Value	Description
1	SMT acquisition is in progress
0	SMT acquisition is not in progress

Note:

1. If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.
2. If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.
3. Details on `MOVIW` and `MOVWI` instruction descriptions are available in the next section.

40.2.1 Standard Instruction Set

ADDFSR	Add Literal to FSRn
Syntax:	[*label*] ADDFSR FSRn, k
Operands:	-32 ≤ k ≤ 31; n ∈ [0, 1]
Operation:	FSR(n) + k → FSR(n)
Status Affected:	None
Description:	The signed 6-bit literal ‘k’ is added to the contents of the FSRnH:FSRnL register pair. FSRn is limited to the range 0000h-FFFFh. Moving beyond these bounds will cause the FSR to wrap-around.

ADDLW	ADD literal to W
Syntax:	[*label*] ADDLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) + k → (W)
Status Affected:	C, DC, Z
Description:	The contents of W are added to the 8-bit literal ‘k’ and the result is placed in W.

ADDWF	ADD W to f
Syntax:	[*label*] ADDWF f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) + (f) → dest
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register ‘f’. If ‘d’ is ‘`0`’, the result is stored in the W register. If ‘d’ is ‘`1`’, the result is stored back in register ‘f’.

Example:	NOP
None.	

RESET	Software Reset
Syntax:	[*label*] RESET
Operands:	None
Operation:	Execute a device Reset. Resets the $\overline{RI}$ flag of the PCON register.
Status Affected:	None
Description:	This instruction provides a way to execute a hardware Reset by software.

RETFIE	Return from Interrupt			
Syntax:	[*label*] RETFIE k			
Operands:	None			
Operation:	(TOS) → PC, 1 → GIE			
Status Affected:	None			
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction.			
Words:	1			
Cycles:	2			

Example:	RETFIE
After Interrupt PC = TOS GIE = 1	

RETLW	Return literal to W
Syntax:	[*label*] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W), (TOS) → PC,
Status Affected:	None

42.4.9 Comparator Specifications

Table 42-15.

Standard Operating Conditions (unless otherwise stated) V_{DD} = 3.0V, T_A = 25°C							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ. †**	**Max.**	**Units**	**Conditions**
CM01	V_{IOFF}	Input Offset Voltage	—	±30	—	mV	$V_{ICM} = V_{DD}/2$
CM02	V_{ICM}	Input Common Mode Range	GND	—	V_{DD}	V	
CM03	CMRR	Common Mode Input Rejection Ratio	—	50	—	dB	
CM04	V_{HYST}	Comparator Hysteresis	15	25	35	mV	
CM05	T_{RESP}(1)	Response Time, Rising Edge	—	300	600	ns	
		Response Time, Falling Edge	—	220	500	ns	
CM06*	T_{MCV2VO}(2)	Mode Change to Valid Output	—	—	10	ns	

* - These parameters are characterized but not tested.

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:

1. Response time measured with one comparator input at $V_{DD}/2$, while the other input transitions from V_{SS} to V_{DD}.
2. A mode change includes changing any of the control register values, including module enable.

42.4.10 5-Bit DAC Specifications

Table 42-16.

Standard Operating Conditions (unless otherwise stated) V_{DD} = 3.0V, T_A = 25°C							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ. †**	**Max.**	**Units**	**Conditions**
DSB01	V_{LSB}	Step Size	—	($V_{DACREF+}$ - $V_{DACREF-}$)/32	—	V	
DSB02	V_{ACC}	Absolute Accuracy	—	—	±0.5	LSb	