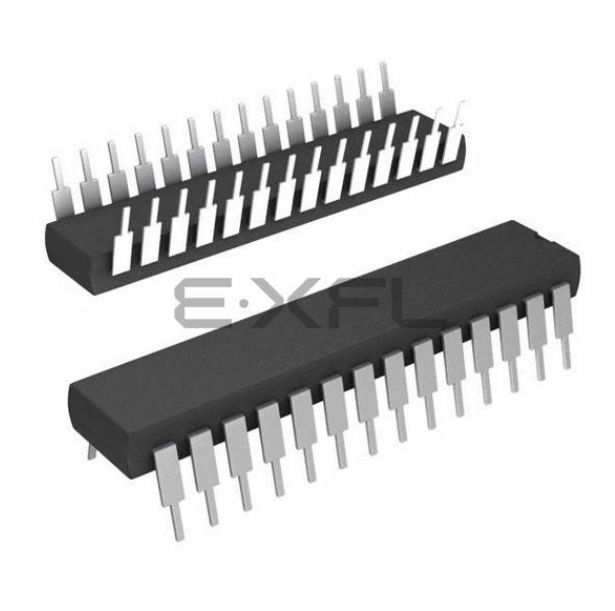

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18456-i-sp

- 256B Data EEPROM
- Direct, Indirect and Relative Addressing modes
- Memory Access Partition (MAP):
  - Write-protect
  - Customizable partition
- Device Information Area (DIA)
- Device Configuration Information (DCI)

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF184XX)
  - 2.3V to 5.5V (PIC16F184XX)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Operation Modes

- Doze: CPU and Peripherals Running at Different Cycle Rates (typically CPU is lower)
- Idle: CPU Halted While Peripherals Operate
- Sleep: Lowest Power Consumption
- Peripheral Module Disable (PMD):
  - Ability to selectively disable hardware module to minimize active power consumption of unused peripherals
- Extreme Low-Power mode (XLP)
  - Sleep: 500 nA typical @ 1.8V
  - Sleep and Watchdog Timer: 900 nA typical @ 1.8V

eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

Digital Peripherals

- Configurable Logic Cell (CLC):
  - 4 CLCs
  - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
  - 3 CWGs

4.7.1 CONFIG1

Name: CONFIG1
Address: 0x8007

Configuration word 1

Oscillators

Bit	15	14	13	12	11	10	9	8
			FCMEN		CSWEN			$\overline{\text{CLKOUTEN}}$
Access			R/P	U	R/P	U	U	R/P
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
		RSTOSC[2:0]				FEXTOSC[2:0]		
Access	U	R/P	R/P	R/P	U	R/P	R/P	R/P
Reset	1	1	1	1	1	1	1	1

Bit 13 – FCMEN Fail-Safe Clock Monitor Enable bit

Value	Description
1	FSCM timer enabled
0	FSCM timer disabled

Bit 11 – CSWEN Clock Switch Enable bit

Value	Description
1	Writing to NOSC and NDIV is allowed
0	The NOSC and NDIV bits cannot be changed by user software

Bit 8 – $\overline{\text{CLKOUTEN}}$ Clock Out Enable bit

Value	Condition	Description
1	If FEXTOSC = EC (high, mid or low) or Not Enabled	CLKOUT function is disabled; I/O or oscillator function on OSC2
0	If FEXTOSC = EC (high, mid or low) or Not Enabled	CLKOUT function is enabled; F_{OSC}/4 clock appears at OSC2
	Otherwise	This bit is ignored.

Bits 6:4 – RSTOSC[2:0] Power-up Default Value for COSC bits
This value is the Reset default value for COSC and selects the oscillator first used by user software. Refer to COSC operation.

Value	Description
111	EXTOSC operating per FEXTOSC bits
110	HFINTOSC (1 MHz), with OSCFRQ = '010' (4 MHz) and CDIV = '0010' (4:1)
101	LFINTOSC
100	SOSC
011	Reserved
010	EXTOSC with 4x PLL, with EXTOSC operating per FEXTOSC bits

9.6.6 OSCTUNE

Name: OSCTUNE
Address: 0x892

HFINTOSC Tuning Register

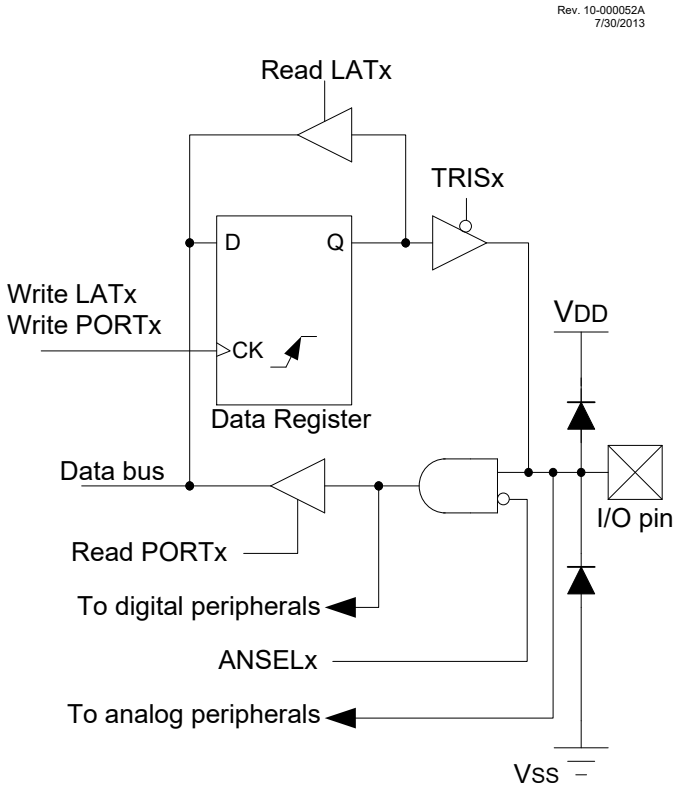
Bit	7	6	5	4	3	2	1	0
			HFTUN[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:0 – HFTUN[5:0] HFINTOSC Frequency Tuning bits

Value	Description
01 1111	Maximum frequency
00 0000	Center frequency. Oscillator module is running at the calibrated frequency (default value).
10 0000	Minimum frequency

Disabling the input buffer prevents analog signal levels on the pin between a logic high and low from causing excessive current in the logic input circuitry. A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in the following figure:

Figure 14-1. Generic I/O Port Operation



14.3 I/O Priorities

Each pin defaults to the PORT data latch after Reset. Other functions are selected with the peripheral pin select logic. See *"Peripheral Pin Select (PPS) Module"* for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELx register. Digital output functions may continue to control the pin when it is in Analog mode.

Analog outputs, when enabled, take priority over digital outputs and force the digital output driver into a high-impedance state.

The pin function priorities are as follows:

1. Configuration bits
2. Analog outputs (disable the input buffers)
3. Analog inputs
4. Port inputs and outputs from PPS

Related Links

15. (PPS) Peripheral Pin Select Module

14.7.1 PORTA

Name: PORTA
Address: 0x00C

PORTA Register
Note: Writes to PORTA are actually written to the corresponding LATA register.
Reads from PORTA register return actual I/O pin values.

Bit	7	6	5	4	3	2	1	0
	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 0, 1, 2, 3, 4, 5, 6, 7 – RAn Port I/O Value bits
Reset States: POR/BOR = xxxxxxxx
All Other Resets = uuuuuuuu

Value	Description
1	Port pin is ≥ V_{IH}
0	Port pin is ≤ V_{IL}

14.7.7 TRISC

Name: TRISC
Address: 0x014

Tri-State Control Register

Bit	7	6	5	4	3	2	1	0
	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 0, 1, 2, 3, 4, 5, 6, 7 – TRISCn TRISC Port I/O Tri-state Control bits

Value	Description
1	Port output driver is disabled
0	Port output driver is enabled

Address	Name	Bit Pos.								
0x1EBD	CLCIN2PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBE	CLCIN3PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBF ... 0x1EC2	Reserved									
0x1EC3	ADACTPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC4	Reserved									
0x1EC5	SSP1CLKPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC6	SSP1DATPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC7	SSP1SSPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC8	SSP2CLKPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC9	SSP2DATPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECA	SSP2SSPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECB	RX1PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECC	CK1PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECD	RX2PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECE	CK2PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECF ... 0x1F0F	Reserved									
0x1F10	RA0PPS	7:0			PPS[5:0]					
0x1F11	RA1PPS	7:0			PPS[5:0]					
0x1F12	RA2PPS	7:0			PPS[5:0]					
0x1F13	RA3PPS	7:0			PPS[5:0]					
0x1F14	RA4PPS	7:0			PPS[5:0]					
0x1F15	RA5PPS	7:0			PPS[5:0]					
0x1F16	RA6PPS	7:0			PPS[5:0]					
0x1F17	RA7PPS	7:0			PPS[5:0]					
0x1F18	RB0PPS	7:0			PPS[5:0]					
0x1F19	RB1PPS	7:0			PPS[5:0]					
0x1F1A	RB2PPS	7:0			PPS[5:0]					
0x1F1B	RB3PPS	7:0			PPS[5:0]					
0x1F1C	RB4PPS	7:0			PPS[5:0]					
0x1F1D	RB5PPS	7:0			PPS[5:0]					
0x1F1E	RB6PPS	7:0			PPS[5:0]					
0x1F1F	RB7PPS	7:0			PPS[5:0]					
0x1F20	RC0PPS	7:0			PPS[5:0]					
0x1F21	RC1PPS	7:0			PPS[5:0]					
0x1F22	RC2PPS	7:0			PPS[5:0]					
0x1F23	RC3PPS	7:0			PPS[5:0]					
0x1F24	RC4PPS	7:0			PPS[5:0]					
0x1F25	RC5PPS	7:0			PPS[5:0]					
0x1F26	RC6PPS	7:0			PPS[5:0]					
0x1F27	RC7PPS	7:0			PPS[5:0]					

16.5.5 PMD4

Name: PMD4
Address: 0x79A

PMD Control Register 4

Bit	7	6	5	4	3	2	1	0
		PWM7MD	PWM6MD	CCP5MD	CCP4MD	CCP3MD	CCP2MD	CCP1MD
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit 6 – PWM7MD Disable Pulse-Width Modulator PWM7 bit

Value	Description
1	PWM7 module disabled
0	PWM7 module enabled

Bit 5 – PWM6MD Disable Pulse-Width Modulator PWM6 bit

Value	Description
1	PWM6 module disabled
0	PWM6 module enabled

Bit 4 – CCP5MD Disable Pulse-Width Modulator CCP5 bit

Value	Description
1	CCP5 module disabled
0	CCP5 module enabled

Bit 3 – CCP4MD Disable Pulse-Width Modulator CCP4 bit

Value	Description
1	CCP4 module disabled
0	CCP4 module enabled

Bit 2 – CCP3MD Disable Pulse-Width Modulator CCP3 bit

Value	Description
1	CCP3 module disabled
0	CCP3 module enabled

Bit 1 – CCP2MD Disable Pulse-Width Modulator CCP2 bit

Value	Description
1	CCP2 module disabled
0	CCP2 module enabled

Bit 0 – CCP1MD Disable Pulse-Width Modulator CCP1 bit

17.6.9 IOCAP

Name: IOCAP
Address: 0x1F3D

Interrupt-on-Change Positive Edge Register

Bit	7	6	5	4	3	2	1	0
	IOCAP7	IOCAP6	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 – IOCAPn Interrupt-on-Change Positive Edge Enable bits

Value	Description
1	Interrupt-on-Change enabled on the IOCA pin for a positive-going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0	Interrupt-on-Change disabled for the associated pin.

ADC Clock Period (T_{AD})		Device Frequency (F_{OSC})						
ADC Clock Source	ADCLK	64 MHz	32 MHz	20 MHz	16 MHz	8 MHz	4 MHz	1 MHz
F_{OSC}/6	000010	93.75 ns(2)	187.5 ns(2)	300 ns(2)	375 ns(2)	750 ns(2)	1.5 µs	6.0 µs
F_{OSC}/8	000011	125 ns(2)	250 ns(2)	400 ns(2)	500 ns(2)	1.0 µs	2.0 µs	8.0 µs
...	...	...	...	...	...	...	...	...
F_{OSC}/16	000100	250 ns(2)	500 ns(2)	800 ns(2)	1.0 µs	2.0 µs	4.0 µs	16.0 µs(3)
...	...	...	...	...	...	...	...	...
F_{OSC}/128	111111	2.0 µs	4.0 µs	6.4 µs	8.0 µs	16.0 µs(3)	32.0 µs(2)	128.0 µs(2)
FRC	CS(ADCON0<4>) = 1	1.0-6.0 µs	1.0-6.0 µs	1.0-6.0 µs	1.0-6.0 µs	1.0-6.0 µs	1.0-6.0 µs	1.0-6.0 µs

Note:

1. See T_{AD} parameter in the *"Electrical Specifications"* section for FRC source typical T_{AD} value.
2. These values violate the required T_{AD} time.
3. Outside the recommended T_{AD} time.
4. The ADC clock period (T_{AD}) and total ADC conversion time can be minimized when the ADC clock is derived from the system clock F_{OSC}. However, the FRC oscillator source must be used when conversions are to be performed with the device in Sleep mode.

Related Links

20.8.1 ADCON0

42.4.8 Analog-to-Digital Converter (ADC) Conversion Timing Specifications

20.1.5 Interrupts

The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital Conversion. The ADC Interrupt Flag is the ADIF bit in the PIRx register. The ADC Interrupt Enable is the ADIE bit in the PIEx register. The ADIF bit must be cleared in software.

Important:

1. The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.
2. The ADC operates during Sleep only when the FRC oscillator is selected.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the ADIE bit and the PEIE bit of the INTCON register must both be set and the GIE bit of the

20.8.21 ADUTH

Name: ADUTH
Address: 0x08E

ADC Upper Threshold Register

ADLTH and ADUTH are compared with ADERR to set the UTHR and LTHR bits. Depending on the setting of TMD, an interrupt may be triggered by the results of this comparison.

Bit	15	14	13	12	11	10	9	8
	UTHH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	UTHL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – UTHH[7:0] ADC Upper Threshold MSB.

Bits 7:0 – UTHL[7:0] ADC Upper Threshold LSB.

22.9.4 NCOxINC

Name: NCOxINC
Address: 0x058F

NCO Increment Register

Bit	23	22	21	20	19	18	17	16
					INCU[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	INCH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INCL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 19:16 – INCU[3:0] NCO Increment – Upper Byte(1)

Bits 15:8 – INCH[7:0] NCO Increment – High Byte(1)

Bits 7:0 – INCL[7:0] NCO Increment – Low Byte(1,2)

Note:

1. The logical increment spans NCOxINCU:NCOxINCH:NCOxINCL.
2. NCOxINC is double-buffered as INCBUF; INCBUF is updated on the next falling edge of NCOxCLK after writing to NCOxINCL; NCOxINCU and NCOxINCH should be written prior to writing NCOxINCL.

- TMRxON bit of the TxCON register
- TMRxIE bits of the PIEx register
- PEIE/GIEL bit of the INTCON register
- GIE/GIEH bit of the INTCON register

The interrupt is cleared by clearing the TMRxIF bit in the Interrupt Service Routine.

For more information on selecting high or low priority status for the Timer1 overflow interrupt, see the Interrupts chapter.

Important: The TMRxH:TMRxL register pair and the TMRxIF bit should be cleared before enabling interrupts.

26.9 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when set up in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMRxON bit of the TxCON register must be set
- TMRxIE bit of the PIEx register must be set
- PEIE/GIEL bit of the INTCON register must be set
- $\overline{\text{TxSYNC}}$ bit of the TxCON register must be set
- Configure the TMRxCLK register for using secondary oscillator as the clock source
- Enable the SOSCEN bit of the OSCEN register

The device will wake-up on an overflow and execute the next instruction. If the GIE/GIEH bit of the INTCON register is set, the device will call the Interrupt Service Routine.

The secondary oscillator will continue to operate in Sleep regardless of the $\overline{\text{TxSYNC}}$ bit setting.

26.10 CCP Capture/Compare Time Base

The CCP modules use the TMRxH:TMRxL register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMRxH:TMRxL register pair is copied into the CCPRxH:CCPRxL register pair on a configured event.

In Compare mode, an event is triggered when the value in the CCPRxH:CCPRxL register pair matches the value in the TMRxH:TMRxL register pair. This event can be a Special Event Trigger.

For more information, see Capture/Compare/PWM Module(CCP) chapter.

Related Links

29. Capture/Compare/PWM Module

Related Links

20.2.6 Auto-Conversion Trigger

29.3.4 Compare During Sleep

Since F_{OSC} is shut down during Sleep mode, the Compare mode will not function properly during Sleep, unless the timer is running. The device will wake on interrupt (if enabled).

29.4 PWM Overview

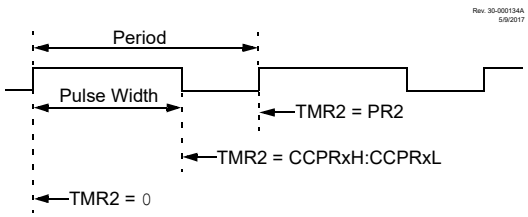
Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully ON and fully OFF states. The PWM signal resembles a square wave where the high portion of the signal is considered the ON state and the low portion of the signal is considered the OFF state. The high portion, also known as the pulse width, can vary in time and is defined in steps. A larger number of steps applied, which lengthens the pulse width, also supplies more power to the load. Lowering the number of steps applied, which shortens the pulse width, supplies less power. The PWM period is defined as the duration of one complete cycle or the total amount of ON and OFF time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse-width time and in turn the power that is applied to the load.

The term duty cycle describes the proportion of the ON time to the OFF time and is expressed in percentages, where 0% is fully OFF and 100% is fully ON. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied.

The shows a typical waveform of the PWM signal.

Figure 29-3. CCP PWM Output Signal



29.4.1 Standard PWM Operation

The standard PWM function described in this section is available and identical for all CCP modules.

The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the CCPx pin with up to ten bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- Even numbered TxPR registers (T2PR, T4PR, etc)
- Even numbered TxCON registers (T2CON, T4CON, etc)
- 16-bit CCPRx registers
- CCPxCON registers

It is required to have $F_{OSC}/4$ as the clock input to TxTMR for correct PWM operation. The following figure shows a simplified block diagram of PWM operation.

In other words, if the HFINTOSC is simultaneously selected as the system clock and as a CLC input source, when the CLC is enabled, the CPU will go idle during Sleep, but the CLC will continue to operate and the HFINTOSC will remain active.

This will have a direct effect on the Sleep mode current.

33.6 CLC Setup Steps

The following steps should be followed when setting up the CLC:

- Disable CLC by clearing the EN bit.
- Select desired inputs using the CLCxSEL0 through CLCxSEL3 registers (See CLC Data Input Table).
- Clear any associated ANSEL bits.
- Set all TRIS bits associated with inputs.
- Enable the chosen inputs through the four gates using the CLCxGLS0 through CLCxGLS3 registers.
- Select the gate output polarities with the GyPOL bits
- Select the desired logic function with the MODE bits
- Select the desired polarity of the logic output with the POL bit. (This step may be combined with the previous gate output polarity step).
- If driving a device pin, set the desired pin PPS control register and also clear the TRIS bit corresponding to that output.
- Configure the interrupts (optional). See 33.2 CLC Interrupts
- Enable the CLC by setting the EN bit.

35.9.7 SSPxMSK

Name: SSPxMSK
Address: 0x18E,0x198

MSSP Address Mask Register

Bit	7	6	5	4	3	2	1	0
	MSK[6:0]							MSK0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 7:1 – MSK[6:0] Mask bits

Value	Mode	Description
1	I²C Slave	The received address bit n is compared to SSPxADD bit n to detect I²C address match
0	I²C Slave	The received address bit n is not used to detect I²C address match

Bit 0 – MSK0
Mask bit for I²C 10-bit Slave mode

Value	Mode	Description
1	I²C 10-bit Slave	The received address bit 0 is compared to SSPxADD bit 0 to detect I²C address match
0	I²C 10-bit Slave	The received address bit 0 is not used to detect I²C address match
x	SPI or I²C 7-bit	Don't care

Address	Name	Bit Pos.								
0x071D	PIE7	7:0			NVMIE	NCO1IE		CWG3IE	CWG2IE	CWG1IE
0x071E	PIE8	7:0			SMT2PWAIE	SMT2PRAIE	SMT2IE	SMT1PWAIE	SMT1PRAIE	SMT1IE
0x071F ... 0x077F	Reserved									
0x0780	INDF0	7:0	INDF0[7:0]							
0x0781	INDF1	7:0	INDF1[7:0]							
0x0782	PCL	7:0	PCL[7:0]							
0x0783	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x0784	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0786	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0788	BSR	7:0			BSR[5:0]					
0x0789	WREG	7:0	WREG[7:0]							
0x078A	PCLATH	7:0	PCLATH[6:0]							
0x078B	INTCON	7:0	GIE	PEIE						INTEDG
0x078C ... 0x0795	Reserved									
0x0796	PMD0	7:0	SYSCMD	FVRMD				NVMMD	CLKRMD	IOCMD
0x0797	PMD1	7:0		TMR6MD	TMR5MD	TMR4MD	TMR3MD	TMR2MD	TMR1MD	TMR0MD
0x0798	PMD2	7:0	NCO1MD							
0x0799	PMD3	7:0		DAC1MD	ADCMD			C2MD	C1MD	ZCDMD
0x079A	PMD4	7:0		PWM7MD	PWM6MD	CCP5MD	CCP4MD	CCP3MD	CCP2MD	CCP1MD
0x079B	PMD5	7:0	CWG3MD	CWG2MD	CWG1MD					
0x079C	PMD6	7:0			UART2MD	UART1MD			MSSP2MD	MSSP1MD
0x079D	PMD7	7:0		SMT2MD	SMT1MD	CLC4MD	CLC3MD	CLC2MD	CLC1MD	DSM1MD
0x079E ... 0x07FF	Reserved									
0x0800	INDF0	7:0	INDF0[7:0]							
0x0801	INDF1	7:0	INDF1[7:0]							
0x0802	PCL	7:0	PCL[7:0]							
0x0803	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x0804	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0806	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0808	BSR	7:0			BSR[5:0]					
0x0809	WREG	7:0	WREG[7:0]							
0x080A	PCLATH	7:0	PCLATH[6:0]							
0x080B	INTCON	7:0	GIE	PEIE						INTEDG
0x080C	WDTCON0	7:0			WDTPS[4:0]					SEN
0x080D	WDTCON1	7:0		WDTCS[2:0]				WINDOW[2:0]		
0x080E	WDTPSL	7:0	PSCNTL[7:0]							

Address	Name	Bit Pos.								
0x1E1B	CLC2POL	7:0	POL				G4POL	G3POL	G2POL	G1POL
0x1E1C	CLC2SEL0	7:0			D1S[5:0]					
0x1E1D	CLC2SEL1	7:0			D2S[5:0]					
0x1E1E	CLC2SEL2	7:0			D3S[5:0]					
0x1E1F	CLC2SEL3	7:0			D4S[5:0]					
0x1E20	CLC2GLS0	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0x1E21	CLC2GLS1	7:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x1E22	CLC2GLS2	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0x1E23	CLC2GLS3	7:0	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
0x1E24	CLC3CON	7:0	EN		OUT	INTP	INTN	MODE[2:0]		
0x1E25	CLC3POL	7:0	POL				G4POL	G3POL	G2POL	G1POL
0x1E26	CLC3SEL0	7:0			D1S[5:0]					
0x1E27	CLC3SEL1	7:0			D2S[5:0]					
0x1E28	CLC3SEL2	7:0			D3S[5:0]					
0x1E29	CLC3SEL3	7:0			D4S[5:0]					
0x1E2A	CLC3GLS0	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0x1E2B	CLC3GLS1	7:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x1E2C	CLC3GLS2	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0x1E2D	CLC3GLS3	7:0	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
0x1E2E	CLC4CON	7:0	EN		OUT	INTP	INTN	MODE[2:0]		
0x1E2F	CLC4POL	7:0	POL				G4POL	G3POL	G2POL	G1POL
0x1E30	CLC4SEL0	7:0			D1S[5:0]					
0x1E31	CLC4SEL1	7:0			D2S[5:0]					
0x1E32	CLC4SEL2	7:0			D3S[5:0]					
0x1E33	CLC4SEL3	7:0			D4S[5:0]					
0x1E34	CLC4GLS0	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0x1E35	CLC4GLS1	7:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x1E36	CLC4GLS2	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0x1E37	CLC4GLS3	7:0	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
0x1E38 ... 0x1E7F	Reserved									
0x1E80	INDF0	7:0	INDF0[7:0]							
0x1E81	INDF1	7:0	INDF1[7:0]							
0x1E82	PCL	7:0	PCL[7:0]							
0x1E83	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1E84	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1E86	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1E88	BSR	7:0			BSR[5:0]					
0x1E89	WREG	7:0	WREG[7:0]							
0x1E8A	PCLATH	7:0		PCLATH[6:0]						
0x1E8B	INTCON	7:0	GIE	PEIE						INTEDG
0x1E8C ...	Reserved									

ADDWFC	ADD W and CARRY bit to f
Syntax:	[*label*] ADDWFC f {,d}
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) + (f) + (C) → dest
Status Affected:	C, DC, Z
Description:	Add W, the Carry flag and data memory location ‘f’. If ‘d’ is ‘0’, the result is placed in W. If ‘d’ is ‘1’, the result is placed in data memory location ‘f’.

ANDLW	AND literal with W
Syntax:	[*label*] ANDLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) .AND. k → (W)
Status Affected:	Z
Description:	The contents of W are AND’ed with the 8-bit literal ‘k’. The result is placed in W.

ANDWF	AND W with f
Syntax:	[*label*] ANDWF f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) .AND. (f) → dest
Status Affected:	Z
Description:	AND the W register with register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.

ASRF	Arithmetic Right Shift
Syntax:	[*label*] ASRF f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f<7>) → dest<7> (f<7:1>) → dest<6:0> (f<0>) → C

Standard Operating Conditions (unless otherwise stated)							
Param No.	Sym.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions
MEM11	I_{DDPGM}	Supply Current during Programming operation	—	—	10	mA	
Data EEPROM Memory Specifications							
MEM20	E_D	DataEE Byte Endurance	100k	—	—	E/W	-40°C≤T_A≤ +85°C
MEM21	T_{D_RET}	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
MEM22	N_{D_REF}	Total Erase/Write Cycles before Refresh	—	—	100k	E/W	
MEM23	V_{D_RW}	V_{DD} for Read or Erase/Write operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM24	T_{D_BEW}	Byte Erase and Write Cycle Time	—	4.0	5.0	ms	
Program Flash Memory Specifications							
MEM30	E_P	Flash Memory Cell Endurance	10k	—	—	E/W	-40°C≤Ta≤ +85°C (**Note 1**)
MEM32	T_{P_RET}	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
MEM33	V_{P_RD}	V_{DD} for Read operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM34	V_{P_REW}	V_{DD} for Row Erase or Write operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM35	T_{P_REW}	Self-Timed Row Erase or Self-Timed Write	—	2.0	2.5	ms	

† - Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note: