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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18456-i-ss

4.7.4 CONFIG4

Name: CONFIG4
Address: 0x800A

Configuration Word 4

Memory Write Protection

Bit	15	14	13	12	11	10	9	8
			LVP		$\overline{\text{WRTSAF}}$	$\overline{\text{WRTD}}$	$\overline{\text{WRTC}}$	$\overline{\text{WRTB}}$
Access			R/P	U	R/P	R/P	R/P	R/P
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	$\overline{\text{WRTAPP}}$			$\overline{\text{SAFEN}}$	$\overline{\text{BBEN}}$	BBSIZE[2:0]		
Access	R/P	U	U	R/P	R/P	R/P	R/P	R/P
Reset	1	1	1	1	1	1	1	1

Bit 13 – LVP Low-Voltage Programming Enable bit
The LVP bit cannot be written (to zero) while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode, or accidentally eliminating LVP mode from the Configuration state.

The preconditioned (erased) state for this bit is critical.

Value	Description
1	Low-voltage programming enabled. $\overline{\text{MCLR}}/V_{PP}$ pin function is $\overline{\text{MCLR}}$. MCLRE Configuration bit is ignored.
0	HV on $\overline{\text{MCLR}}/V_{PP}$ must be used for programming

Bit 11 – $\overline{\text{WRTSAF}}$ Storage Area Flash Write Protection bit(1)

Value	Description
1	SAF NOT write-protected
0	SAF write-protected

Bit 10 – $\overline{\text{WRTD}}$ Data EEPROM Write Protection bit(1)

Value	Description
1	Data EEPROM NOT write-protected
0	Data EEPROM write-protected

Bit 9 – $\overline{\text{WRTC}}$ Configuration Register Write Protection bit(1)

Value	Description
1	Configuration Registers NOT write-protected
0	Configuration Registers write-protected

Bit 8 – $\overline{\text{WRTB}}$ Boot Block Write Protection bit(1)

The CALLW instruction enables computed calls by combining PCLATH and W to form the destination address. A computed CALLW is accomplished by loading the W register with the desired address and executing CALLW. The PCL register is loaded with the value of W and PCH is loaded with PCLATH.

7.4.4 Branching

The branching instructions add an offset to the PC. This allows relocatable code and code that crosses page boundaries. There are two forms of branching, BRW and BRA. The PC will have incremented to fetch the next instruction in both cases. When using either branching instruction, a PCL memory boundary may be crossed.

If using BRW, load the W register with the desired unsigned address and execute BRW. The entire PC will be loaded with the address PC + 1 + W.

If using BRA, the entire PC will be loaded with PC + 1 + the signed value of the operand of the BRA instruction.

7.5 Stack

All devices have a 16-level by 15-bit wide hardware stack. The stack space is not part of either program or data space. The PC is PUSHed onto the stack when CALL or CALLW instructions are executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer if the STVREN Configuration bit is programmed to '0'. This means that after the stack has been PUSHed sixteen times, the seventeenth PUSH overwrites the value that was stored from the first PUSH. The eighteenth PUSH overwrites the second PUSH (and so on). The STKOVF and STKUNF flag bits will be set on an Overflow/Underflow, regardless of whether the Reset is enabled.

Important: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, CALLW, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

7.5.1 Accessing the Stack

The stack is accessible through the TOSH, TOSL and STKPTR registers. STKPTR is the current value of the Stack Pointer. TOSH:TOSL register pair points to the TOP of the stack. Both registers are read/writable. TOS is split into TOSH and TOSL due to the 15-bit size of the PC. To access the stack, adjust the value of STKPTR, which will position TOSH:TOSL, then read/write to TOSH:TOSL. STKPTR is five bits to allow detection of overflow and underflow.

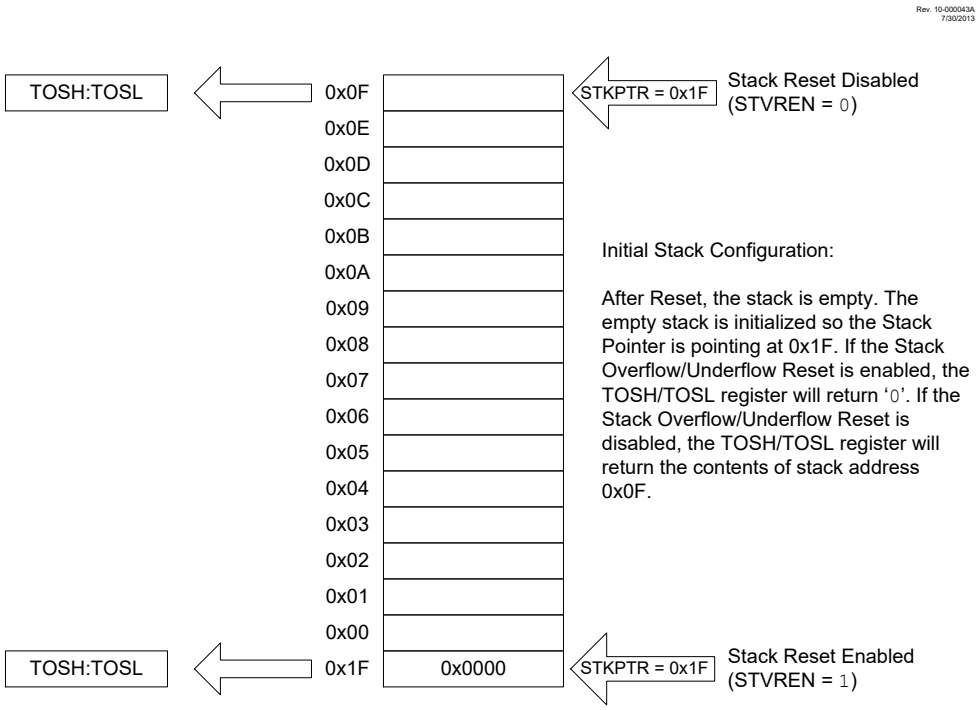
Important: Care should be taken when modifying the STKPTR while interrupts are enabled.

During normal program operation, CALL, CALLW and interrupts will increment STKPTR while RETLW, RETURN, and RETFIE will decrement STKPTR. STKPTR can be monitored to obtain to value of stack

memory left at any given time. The STKPTR always points at the currently used place on the stack. Therefore, a CALL or CALLW will increment the STKPTR and then write the PC, and a return will unload the PC value from the stack and then decrement the STKPTR.

Reference the following figures for examples of accessing the stack.

Figure 7-4. Accessing the Stack Example 1



7.8.7 BSR

Name: BSR
Address: 0x08 + n*0x80 [n=0..63]

Bank Select Register
The BSR indicates the data memory bank by writing the bank number into the register. All data memory can be accessed directly via instructions, or indirectly via FSRs.

Bit	7	6	5	4	3	2	1	0
			BSR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:0 – BSR[5:0]
Six Most Significant bits of the data memory address

Related Links
7.3.2 Core Registers

8.14 Register Summary - BOR Control and Power Control

Address	Name	Bit Pos.								
0x0811	BORCON	7:0	SBOREN							BORRDY
0x0812	Reserved									
0x0813	PCON0	7:0	STKOVF	STKUNF	$\overline{\text{WDTWV}}$	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
0x0814	PCON1	7:0							$\overline{\text{MEMV}}$	

8.15 Register Definitions: Power Control

Related Links

9.6.4 OSCSTAT

9.6.5 OSCEN

9.2.2.8 HFOR and MFOR Bits

The HFOR and MFOR bits indicate that the HFINTOSC and MFINTOSC is ready. These clocks are always valid for use at all times, but only accurate after they are ready.

When a new value is loaded into the OSCFRQ register, the HFOR and MFOR bits will clear, and set again when the oscillator is ready. During pending OSCFRQ changes the MFINTOSC clock will stall at a high or a low state, until the HFINTOSC resumes operation.

9.3 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the New Oscillator Source (NOSC) and New Divider selection request (NDIV) bits. The following clock sources can be selected:

- External Oscillator (EXTOSC)
- High-Frequency Internal Oscillator (HFINTOSC)
- Low-Frequency Internal Oscillator (LFINTOSC)
- Secondary Oscillator (SOSC)
- EXTOSC with 4x PLL
- HFINTOSC with 2x PLL

9.3.1 New Oscillator Source (NOSC) and New Divider Selection Request (NDIV) Bits

The New Oscillator Source (NOSC) and New Divider Selection Request (NDIV) bits select the system clock source and frequency that are used for the CPU and peripherals.

When new values of NOSC and NDIV are written to OSCCON1, the current oscillator selection will continue to operate while waiting for the new clock source to indicate that it is stable and ready. In some cases, the newly requested source may already be in use, and is ready immediately. In the case of a divider-only change, the new and old sources are the same, so the old source will be ready immediately. The device may enter Sleep while waiting for the switch.

When the new oscillator is ready, the New Oscillator Ready (NOSCR) bit is set and also the Clock Switch Interrupt Flag (CSWIF) bit of PIR1 sets. If Clock Switch Interrupts are enabled (CSWIE = 1), an interrupt will be generated at that time. The Oscillator Ready (ORDY) bit of OSCCON3 can also be polled to determine when the oscillator is ready in lieu of an interrupt.

If the Clock Switch Hold (CSWHOLD) bit is clear, the oscillator switch will occur when the New Oscillator is READY bit (NOSCR) is set, and the interrupt (if enabled) will be serviced at the new oscillator setting.

If CSWHOLD is set, the oscillator switch is suspended, while execution continues using the current (old) clock source. When the NOSCR bit is set, software should:

- Set CSWHOLD = 0 so the switch can complete, or
- Copy COSC into NOSC to abandon the switch.

If DOZE is in effect, the switch occurs on the next clock cycle, whether or not the CPU is operating during that cycle.

Changing the clock post-divider without changing the clock source (i.e., changing F_{OSC} from 1 MHz to 2 MHz) is handled in the same manner as a clock source change, as described previously. The clock

14.7.11 ANSELA

Name: ANSELA
Address: 0x1F38

Analog Select Register

Bit	7	6	5	4	3	2	1	0
	ANSELA7	ANSELA6	ANSELA5	ANSELA4	ANSELA3	ANSELA2	ANSELA1	ANSELA0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 0, 1, 2, 3, 4, 5, 6, 7 – ANSELAn Analog Select on Pins RA<7:0>

Value	Description
1	Digital Input buffers are disabled
0	ST and TTL input buffers are enabled

16.5.3 PMD2

Name: PMD2
Address: 0x798

PMD Control Register 2

Bit	7	6	5	4	3	2	1	0
	NCO1MD							
Access	R/W							
Reset	0							

Bit 7 – NCO1MD Disable Numerically Control Oscillator bit

Value	Description
1	NCO1 module disabled
0	NCO1 module enabled

18.4.1 FVRCON

Name: FVRCON
Address: 0x90C

Fixed Voltage Reference Control Register

Bit	7	6	5	4	3	2	1	0
	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR[1:0]		ADFVR[1:0]	
Access	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	q	0	0	0	0	0	0

Bit 7 – FVREN Fixed Voltage Reference Enable bit

Value	Description
1	Fixed Voltage Reference is enabled
0	Fixed Voltage Reference is disabled

Bit 6 – FVRRDY Fixed Voltage Reference Ready Flag bit

Value	Description
1	Fixed Voltage Reference output is ready for use
0	Fixed Voltage Reference output is not ready or not enabled

Bit 5 – TSEN
Temperature Indicator Enable bit(2)

Value	Description
1	Temperature Indicator is enabled
0	Temperature Indicator is disabled

Bit 4 – TSRNG
Temperature Indicator Range Selection bit(2)

Value	Description
1	$V_{OUT} = V_{DD}$ - 4Vt (High Range)
0	$V_{OUT} = V_{DD}$ - 2Vt (Low Range)

Bits 3:2 – CDAFVR[1:0] Comparator FVR Buffer Gain Selection bits

Value	Description
11	Comparator FVR Buffer Gain is 4x, (4.096V)(1)
10	Comparator FVR Buffer Gain is 2x, (2.048V)(1)
01	Comparator FVR Buffer Gain is 1x, (1.024V)
00	Comparator FVR Buffer is off

Bits 1:0 – ADFVR[1:0] ADC FVR Buffer Gain Selection bit

Value	Description
11	ADC FVR Buffer Gain is 4x, (4.096V)(1)
10	ADC FVR Buffer Gain is 2x, (2.048V)(1)

Equation 24-6. Series R for V range

$$R_{SERIES} = \frac{V_{MAX\_PEAK} + V_{MIN\_PEAK}}{7 \times 10^{-4}}$$

24.7 Operation During Sleep

The ZCD current sources and interrupts are unaffected by Sleep.

24.8 Effects of a Reset

The ZCD circuit can be configured to default to the active or inactive state on Power-on Reset (POR). When the $\overline{ZCD}$ Configuration bit is cleared, the ZCD circuit will be active at POR. When the $\overline{ZCD}$ Configuration bit is set, the SEN bit must be set to enable the ZCD module.

24.9 Disabling the ZCD Module

The ZCD module can be disabled in two ways:

1. The $\overline{ZCD}$ Configuration bit disables the ZCD module when set. When this is the case then the ZCD module will be enabled by setting the SEN bit. When the $\overline{ZCD}$ bit is clear, the ZCD is always enabled and the SEN bit has no effect.
2. The ZCD can also be disabled using the ZCDMD bit of the PMDx register. This is subject to the status of the $\overline{ZCD}$ bit.

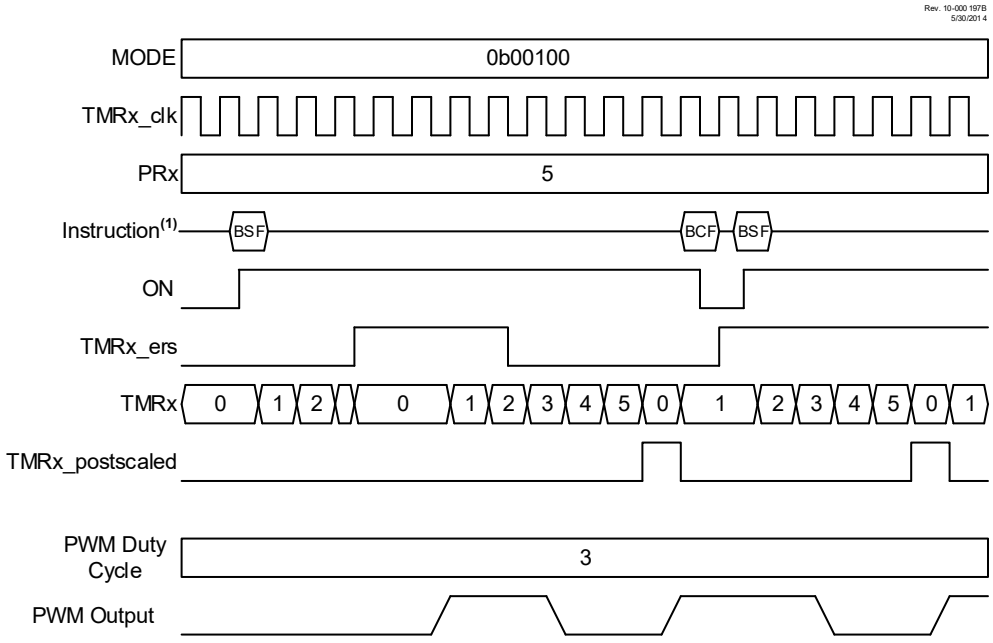
26. Timer1 Module with Gate Control

Timer1 module is a 16-bit timer/counter with the following features:

- 16-Bit Timer/Counter Register Pair (TMRxH:TMRxL)
- Programmable Internal or External Clock Source
- 2-Bit Prescaler
- Optionally Synchronized Comparator Out
- Multiple Timer1 Gate (count enable) Sources
- Interrupt-on-Overflow
- Wake-Up on Overflow (external clock, Asynchronous mode only)
- 16-Bit Read/Write Operation
- Time Base for the Capture/Compare Function with the CCP modules
- Special Event Trigger (with CCP)
- Selectable Gate Source Polarity
- Gate Toggle mode
- Gate Single-Pulse mode
- Gate Value Status
- Gate Event Interrupt

Important: References to module Timer1 apply to all the odd numbered timers on this device.

Figure 27-5. Edge-Triggered Hardware Limit Mode Timing Diagram (MODE = 00100)



Note:

1. BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

Related Links

29.4 PWM Overview

30. (PWM) Pulse-Width Modulation

27.6.4 Level-Triggered Hardware Limit Mode

In the Level-Triggered Hardware Limit Timer modes the counter is reset by high or low levels of the external signal TMRx_ers, as shown in Figure 27-6. Selecting MODE<4:0> = 00110 will cause the timer to reset on a low level external signal. Selecting MODE<4:0> = 00111 will cause the timer to reset on a high level external signal. In the example, the counter is reset while TMRx_ers = 1. ON is controlled by BSF and BCF instructions. When ON = 0 the external signal is ignored.

When the CCP uses the timer as the PWM time base then the PWM output will be set high when the timer starts counting and then set low only when the timer count matches the CCPRx value. The timer is reset when either the timer count matches the PRx value or two clock periods after the external Reset signal goes true and stays true.

The timer starts counting, and the PWM output is set high, on either the clock following the PRx match or two clocks after the external Reset signal relinquishes the Reset. The PWM output will remain high until the timer counts up to match the CCPRx pulse width value. If the external Reset signal goes true while the PWM output is high then the PWM output will remain high until the Reset signal is released allowing the timer to count up to match the CCPRx value.

29.1.2 Open-Drain Output Option

When operating in Output mode (the Compare or PWM modes), the drivers for the CCPx pins can be optionally configured as open-drain outputs. This feature allows the voltage level on the pin to be pulled to a higher level through an external pull-up resistor and allows the output to communicate with external circuits without the need for additional level shifters.

29.2 Capture Mode

Capture mode makes use of the 16-bit odd numbered timer resources (Timer1, Timer3, etc.). When an event occurs on the capture source, the 16-bit CCPRx register captures and stores the 16-bit value of the TMRx register. An event is defined as one of the following and is configured by the MODE bits:

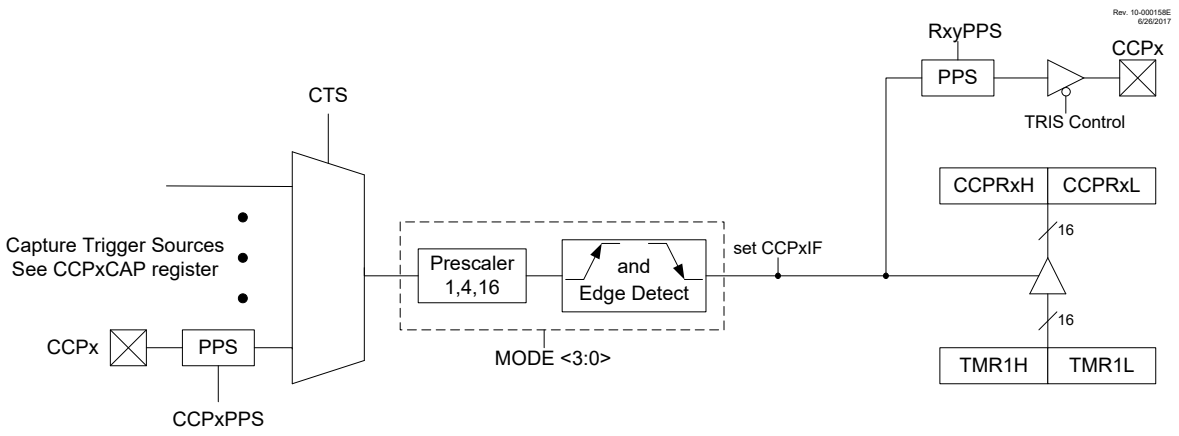
- Every falling edge of CCPx input
- Every rising edge of CCPx input
- Every 4th rising edge of CCPx input
- Every 16th rising edge of CCPx input
- Every edge of CCPx input (rising or falling)

When a capture is made, the Interrupt Request Flag bit CCPxIF of the PIRx register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRx register is read, the old captured value is overwritten by the new captured value.

Important: If an event occurs during a 2-byte read, the high and low-byte data will be from different events. It is recommended while reading the CCPRxH:CCPRxL register pair to either disable the module or read the register pair twice for data integrity.

The following figure shows a simplified diagram of the capture operation.

Figure 29-1. Capture Mode Operation Block Diagram



29.2.1 Capture Sources

In Capture mode, the CCPx pin should be configured as an input by setting the associated TRIS control bit.

29.5 Register Summary - CCP Control

Address	Name	Bit Pos.								
0x030C	CCPR1	7:0	CCPRL[7:0]							
		15:8	CCPRH[7:0]							
0x030E	CCP1CON	7:0	EN		OUT	FMT	MODE[3:0]			
0x030F	CCP1CAP	7:0						CTS[2:0]		
0x0310	CCPR2	7:0	CCPRL[7:0]							
		15:8	CCPRH[7:0]							
0x0312	CCP2CON	7:0	EN		OUT	FMT	MODE[3:0]			
0x0313	CCP2CAP	7:0						CTS[2:0]		
0x0314	CCPR3	7:0	CCPRL[7:0]							
		15:8	CCPRH[7:0]							
0x0316	CCP3CON	7:0	EN		OUT	FMT	MODE[3:0]			
0x0317	CCP3CAP	7:0						CTS[2:0]		
0x0318	CCPR4	7:0	CCPRL[7:0]							
		15:8	CCPRH[7:0]							
0x031A	CCP4CON	7:0	EN		OUT	FMT	MODE[3:0]			
0x031B	CCP4CAP	7:0						CTS[2:0]		
0x031C	CCPR5	7:0	CCPRL[7:0]							
		15:8	CCPRH[7:0]							
0x031E	CCP5CON	7:0	EN		OUT	FMT	MODE[3:0]			
0x031F	CCP5CAP	7:0						CTS[2:0]		

29.6 Register Definitions: CCP Control

Long bit name prefixes for the CCP peripherals are shown in the following table. Refer to the *"Long Bit Names"* section for more information.

Table 29-5. CCP Long bit name prefixes

Peripheral	Bit Name Prefix
CCP1	CCP1
CCP2	CCP2
CCP3	CCP3
CCP4	CCP4
CCP5	CCP5

Related Links

1.4.2.2 Long Bit Names

34.6.2 CLKRCLK

Name: CLKRCLK
Address: 0x896

Clock Reference Clock Selection MUX

Bit	7	6	5	4	3	2	1	0
					CLK[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – CLK[3:0] CLKR Clock Selection bits
See the Clock Sources table.

Figure 37-7. High and Low Measurement Mode, Repeat Acquisition Timing Diagram

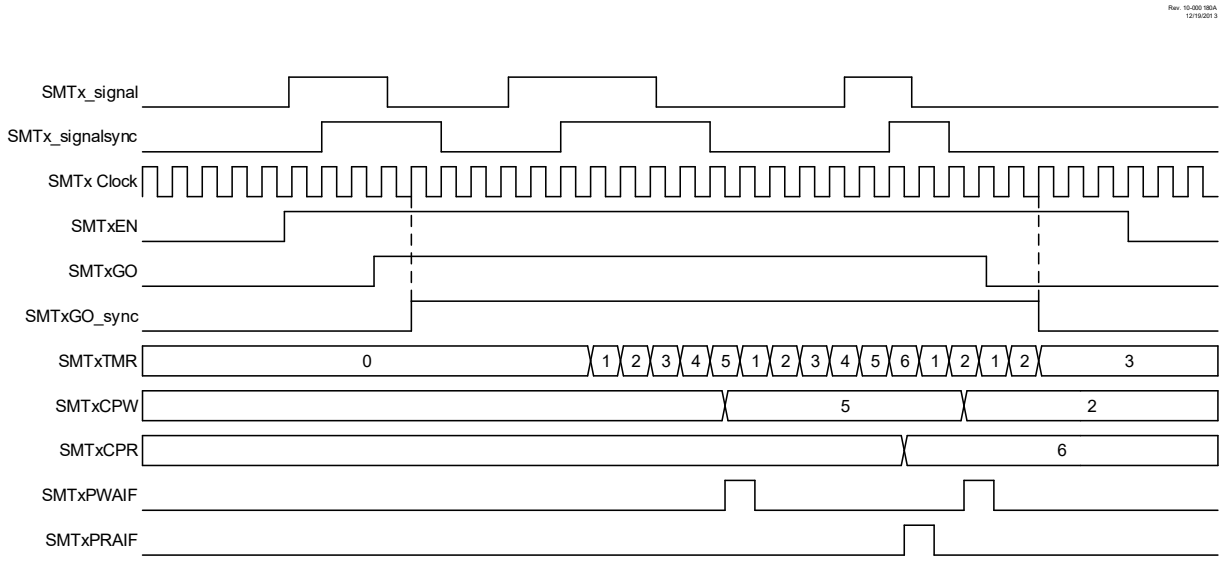
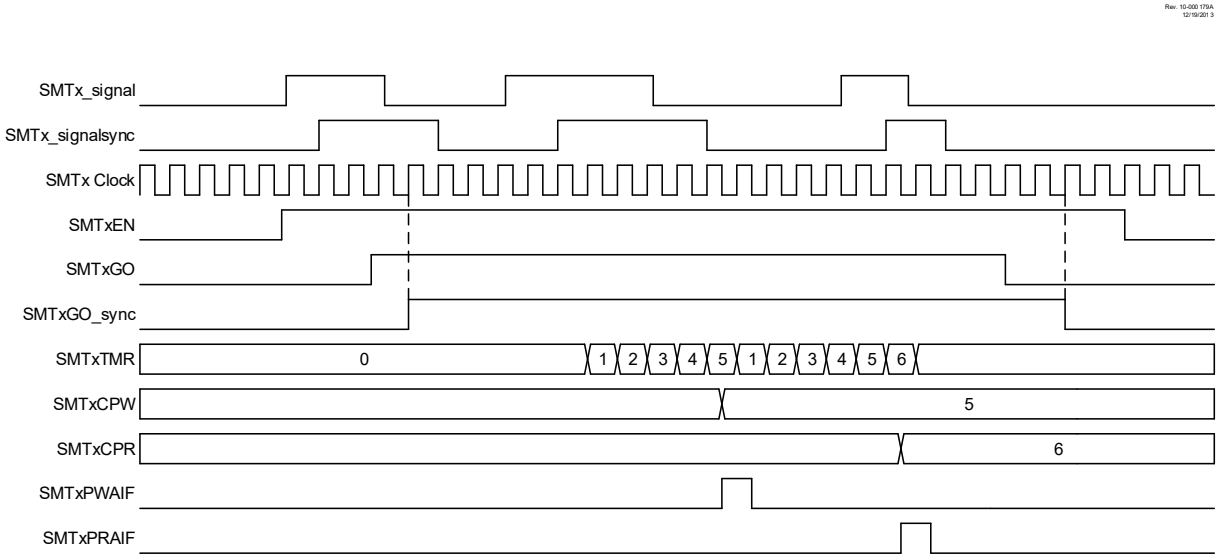


Figure 37-8. High and Low Measurement Mode, Single Acquisition Timing Diagram



37.1.6.5 Windowed Measurement Mode

This mode measures the duration of the window input (WSEL) to the SMT. It begins incrementing the timer on a rising edge of the window input and updates the SMTxCPR register with the value of the timer and resets the timer on a second rising edge. See figures below.

WSEL<4:0>	SMT1 Window Source	SMT2 Window Source
00011	SOSC	SOSC
00010	MFINTOSC (31.25kHz)	MFINTOSC (31.25kHz)
00001	LFINTOSC (31.25kHz)	LFINTOSC (31.25kHz)
00000	Pin Selected by SMT1WINPPS	Pin Selected by SMT1WINPPS

Address	Name	Bit Pos.								
0x1103	STATUS	7:0				TO	PD	Z	DC	C
0x1104	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1106	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1108	BSR	7:0			BSR[5:0]					
0x1109	WREG	7:0	WREG[7:0]							
0x110A	PCLATH	7:0		PCLATH[6:0]						
0x110B	INTCON	7:0	GIE	PEIE						INTEDG
0x110C ... 0x117F	Reserved									
0x1180	INDF0	7:0	INDF0[7:0]							
0x1181	INDF1	7:0	INDF1[7:0]							
0x1182	PCL	7:0	PCL[7:0]							
0x1183	STATUS	7:0				TO	PD	Z	DC	C
0x1184	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1186	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1188	BSR	7:0			BSR[5:0]					
0x1189	WREG	7:0	WREG[7:0]							
0x118A	PCLATH	7:0		PCLATH[6:0]						
0x118B	INTCON	7:0	GIE	PEIE						INTEDG
0x118C ... 0x11FF	Reserved									
0x1200	INDF0	7:0	INDF0[7:0]							
0x1201	INDF1	7:0	INDF1[7:0]							
0x1202	PCL	7:0	PCL[7:0]							
0x1203	STATUS	7:0				TO	PD	Z	DC	C
0x1204	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1206	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1208	BSR	7:0			BSR[5:0]					
0x1209	WREG	7:0	WREG[7:0]							
0x120A	PCLATH	7:0		PCLATH[6:0]						
0x120B	INTCON	7:0	GIE	PEIE						INTEDG
0x120C ... 0x127F	Reserved									
0x1280	INDF0	7:0	INDF0[7:0]							
0x1281	INDF1	7:0	INDF1[7:0]							
0x1282	PCL	7:0	PCL[7:0]							
0x1283	STATUS	7:0				TO	PD	Z	DC	C

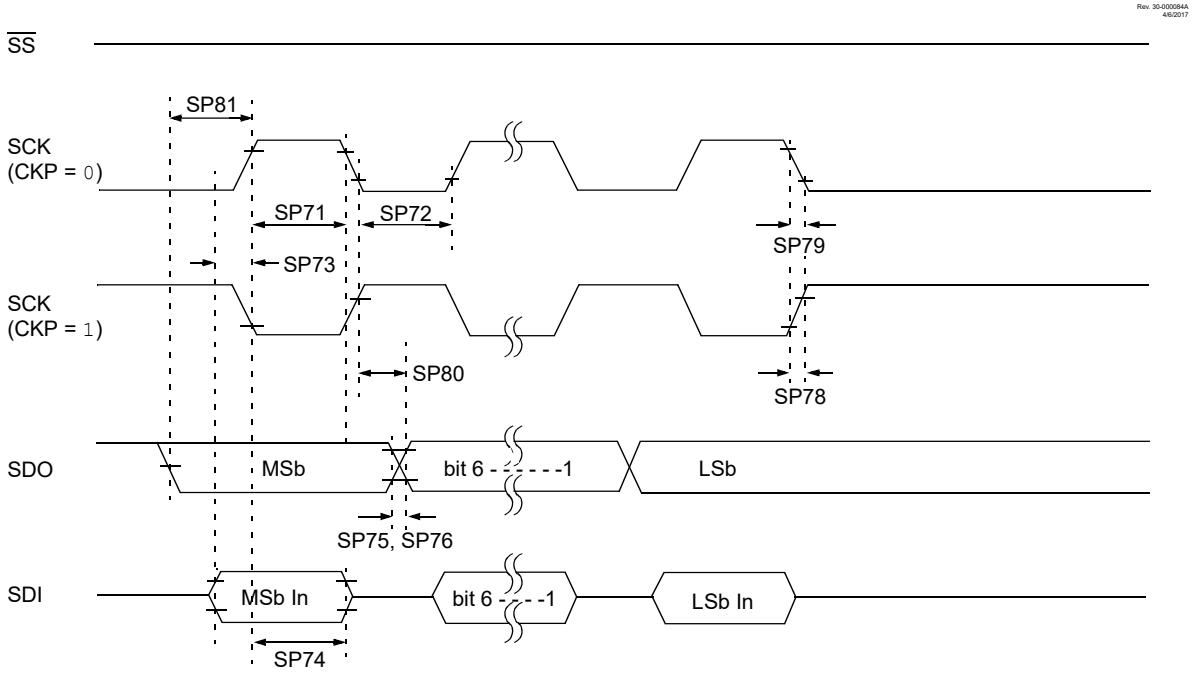
CLRW	Clear W
Syntax:	[*label*] CLRW
Operands:	None
Operation:	00h → (W) 1 → Z
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

CLRWDT	Clear Watchdog Timer
Syntax:	[*label*] CLRWDT
Operands:	None
Operation:	00h → WDT, 00h → WDT prescaler, 1 → $\overline{TO}$, 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	`CLRWDT` instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits, $\overline{TO}$ and $\overline{PD}$, are set.

COMF	Complement f
Syntax:	[*label*] COMF f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	($\bar{f}$) → dest
Status Affected:	Z
Description:	The contents of register ‘f’ are complemented. If ‘d’ is ‘`0`’, the result is stored in W. If ‘d’ is ‘`1`’, the result is stored back in register ‘f’.

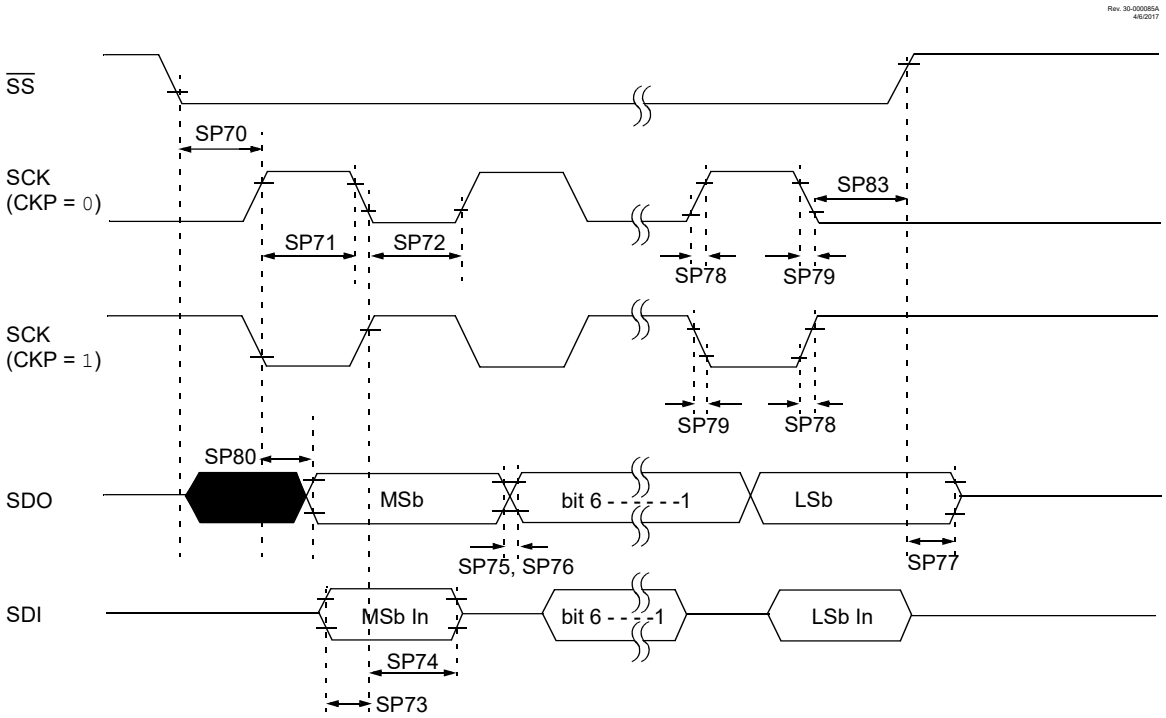
DECF	Decrement f
Syntax:	[*label*] DECF f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) – 1 → dest

Figure 42-18. SPI Master Mode Timing (CKE = 1, SMP = 1)



Note: Refer to Figure 42-4 for load conditions.

Figure 42-19. SPI Slave Mode Timing (CKE = 0)



Note: Refer to Figure 42-4 for load conditions.