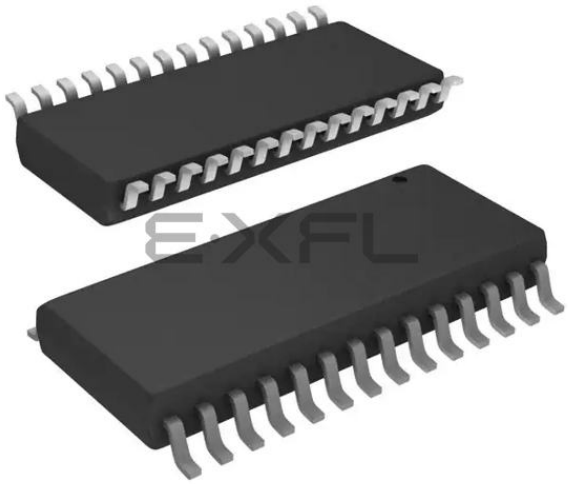

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18455-i-so

4.7.3 CONFIG3

Name: CONFIG3
Address: 0x8009

Configuration Word 3

Windowed Watchdog Timer

Bit	15	14	13	12	11	10	9	8
			WDTCCS[2:0]			WDTCWS[2:0]		
Access			R/P	R/P	R/P	R/P	R/P	R/P
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
		WDTE[1:0]		WDTCPS[4:0]				
Access	U	R/P	R/P	R/P	R/P	R/P	R/P	R/P
Reset	1	1	1	1	1	1	1	1

Bits 13:11 – WDTCCS[2:0] WDT Input Clock Selector bits

Value	Description
111	Software Control
110 to 011	Reserved
010	32 kHz SOSC
001	WDT reference clock is the 31.25 kHz HFINTOSC (MFINTOSC) output
000	WDT reference clock is the 31.0 kHz LFINTOSC

Bits 10:8 – WDTCWS[2:0] WDT Window Select bits

WDTCWS	WDTCON1 [WINDOW] at POR			Software control of WINDOW?	Keyed access required?
	Value	Window delay Percent of time	Window opening Percent of time		
111	111	n/a	100	Yes	No
110	110	n/a	100	No	Yes
101	101	25	75		
100	100	37.5	62.5		
011	011	50	50		
010	010	62.5	37.5		
001	001	75	25		
000	000	87.5	12.5		

Bits 6:5 – WDTE[1:0] WDT Operating Mode bits

7.8.3 PCL

Name: PCL
Address: 0x02 + n*0x80 [n=0..63]

Low byte of the Program Counter

Bit	7	6	5	4	3	2	1	0
	PCL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – PCL[7:0]
Provides direct read and write access to the Program Counter

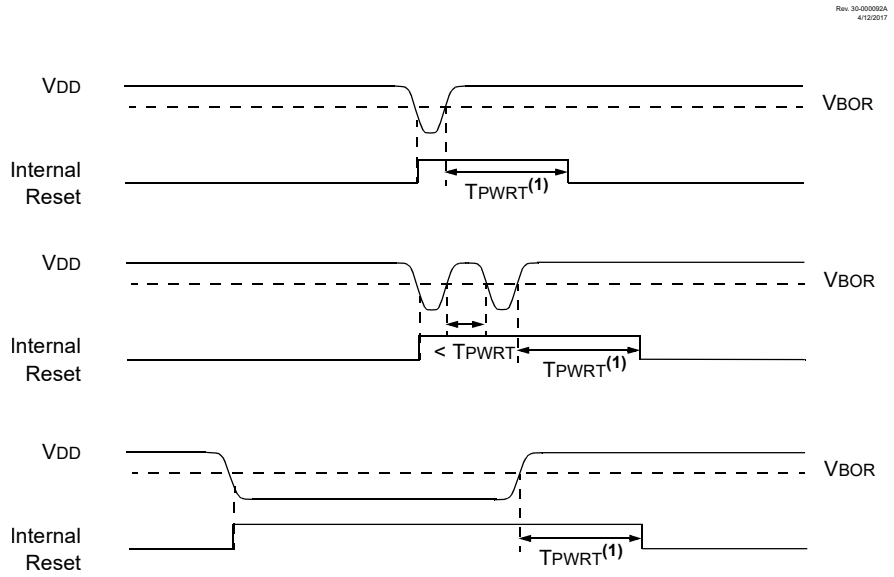
Table 8-1. BOR Operating Conditions

BOREN<1:0>	SBOREN	Device Mode	BOR Mode	Instruction Execution upon: Release of POR or Wake-up from Sleep
11	X	X	Active	Waits for release of BOR(1) (BORRDY = 1)
10	X	Awake	Active	Waits for release of BOR (BORRDY = 1) Waits for BOR Reset release
		Sleep	Disabled	
01	1	X	Active	Waits for BOR Reset release (BORRDY = 1)
	0	X	Disabled	Begins immediately (BORRDY = x)
00	X	X	Disabled	

Note:

1. In this specific case, “Release of POR” and “Wake-up from Sleep”, there is no delay in start-up. The BOR ready flag, (BORRDY = 1), will be set before the CPU is ready to execute instructions because the BOR circuit is forced on by the BOREN<1:0> bits

Figure 8-2. Brown-out Situations



Note: T_{PWRT} delay only if PWRTS bit field is programmed to a value different from ‘11’.

8.2.4 BOR is Always OFF

When the BOREN bits of the Configuration Words are programmed to ‘00’, the BOR is off at all times. The device start-up is not delayed by the BOR ready condition or the V_{DD} level.

8.3 Low-Power Brown-out Reset (LPBOR)

The Low-Power Brown-out Reset (LPBOR) provides an additional BOR circuit for low-power operation. Refer to the figure below to see how the BOR interacts with other modules.

8.4.1 MCLR Enabled

When MCLR is enabled and the pin is held low, the device is held in Reset. The MCLR pin is connected to V_{DD} through an internal weak pull-up.

The device has a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

Important: An internal Reset event (RESET instruction, BOR, WWDT, POR, STKOVF, STKUNF) does not drive the MCLR pin low.

Related Links

2.3 Master Clear (MCLR) Pin

8.4.2 MCLR Disabled

When MCLR is disabled, the MCLR becomes input-only and pin functions such as internal weak pull-ups are under software control.

Related Links

14.3 I/O Priorities

8.5 Windowed Watchdog Timer (WWDT) Reset

The Windowed Watchdog Timer generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period or window set. The TO and PD bits in the STATUS register and the RWDT bit are changed to indicate a WDT Reset. The WDTWV bit indicates if the WDT Reset has occurred due to a timeout or a window violation.

Related Links

7.8.4 STATUS

12. (WWDT) Windowed Watchdog Timer

8.6 RESET Instruction

A RESET instruction will cause a device Reset. The RI bit will be set to '0'. See *"Reset Condition for Special Registers"* table for default conditions after a RESET instruction has occurred.

8.7 Stack Overflow/Underflow Reset

The device can reset when the Stack Overflows or Underflows. The STKOVF or STKUNF bits register indicate the Reset condition. These Resets are enabled by setting the STVREN bit in Configuration Words.

Related Links

4.7.2 CONFIG2

7.5.2 Overflow/Underflow Reset

8.8 Programming Mode Exit

Upon exit of Programming mode, the device will behave as if a POR had just occurred.

10.7.9 PIE7

Name: PIE7
Address: 0x71D

Peripheral Interrupt Enable Register 7

Bit	7	6	5	4	3	2	1	0
			NVMIE	NCO1IE		CWG3IE	CWG2IE	CWG1IE
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bit 5 – NVMIE NVM Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 4 – NCO1IE NCO Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 2 – CWG3IE CWG3 Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 1 – CWG2IE CWG2 Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 0 – CWG1IE CWG1 Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by registers PIE1-PIE8.

12.8.5 WDTTMR

Name: WDTTMR
Address: 0x810

WDT Timer Register (Read-Only)

Bit	7	6	5	4	3	2	1	0
	WDTTMR[4:0]					STATE	PSCNT[1:0]	
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 7:3 – WDTTMR[4:0] Watchdog Window Value bits

WINDOW	WDT Window State		Open Percent
	Closed	Open	
111	**N/A**	00000-11111	100
110	00000-00011	00100-11111	87.5
101	00000-00111	01000-11111	75
100	00000-01011	01100-11111	62.5
011	00000-01111	10000-11111	50
010	00000-10011	10100-11111	37.5
001	00000-10111	11000-11111	25
000	00000-11011	11100-11111	12.5

Bit 2 – STATE WDT Armed Status bit

Value	Description
1	WDT is armed
0	WDT is not armed

Bits 1:0 – PSCNT[1:0] Prescale Select Upper Byte bits(1)

Note:

1. The 18-bit WDT prescale value, PSCNT<17:0> includes the WDTPSL, WDTPSH and the lower bits of the WDTTMR registers. PSCNT<17:0> is intended for debug operations and should be read during normal operation.

13.4.9 WRERR Bit

The WRERR bit can be used to determine if a write error occurred. WRERR will be set if one of the following conditions occurs:

- If WR is set while the NVMADRH:NMVADRL points to a write-protected address
- A Reset occurs while a self-write operation was in progress
- An unlock sequence was interrupted

The WRERR bit is normally set by hardware, but can be set by the user for test purposes. Once set, WRERR must be cleared in software.

Table 13-3. Actions for PFM When WR = 1

Free	LWLO	Actions for PFM when WR = 1	Comments
1	x	Erase the 32-word row of NVMADRH:NVMADRL location.	• If WP is enabled, WR is cleared and WRERR is set • All 32 words are erased • NVMDATH:NVMDATL is ignored
0	1	Copy NVMDATH:NVMDATL to the write latch corresponding to NVMADR LSBs.	• Write protection is ignored • No memory access occurs
0	0	Write the write-latch data to PFM row.	• If WP is enabled, WR is cleared and WRERR is set • Write latches are reset to 3FFh • NVMDATH:NVMDATL is ignored

Related Links

13.4.4 NVMREG Erase of Program Memory

14.4.4 Slew Rate Control

The SLRCONx register controls the slew rate option for each port pin. Slew rate for each port pin can be controlled independently. When an SLRCONx bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONx bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

14.4.5 Input Threshold Control

The INLVLx register controls the input voltage threshold for each of the available PORTx input pins. A selection between the Schmitt Trigger CMOS or the TTL compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTx register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See link below for more information on threshold levels.

Important: Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

14.4.6 Analog Control

The ANSELx register is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELx bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELx bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing `READ-MODIFY-WRITE` instructions on the affected port.

Important: The ANSELx bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

14.4.7 Weak Pull-up Control

The WPUx register controls the individual weak pull-ups for each port pin.

14.4.8 PORTx Functions and Output Priorities

Each PORTx pin is multiplexed with other functions.

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic, or by enabling an analog output, such as the DAC. See the link below for more information.

Analog input functions, such as ADC and comparator inputs are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

Related Links

15. (PPS) Peripheral Pin Select Module

Output Signal Name	RxyPPS Register Value
NCO1OUT	0x18
PWM6OUT	0x0D
PWM7OUT	0x0E
SCK1	0x13
SCL1	0x13
SDA1	0x14
SDO1	0x14
SCK2	0x15
SCL2	0x15
SDA2	0x16
SDO2	0x16
TMR0OUT	0x17

Note:
1. CK1/CK2 and DT1/DT2 are bidirectional signals used in EUSART Synchronous mode.

15.3 Bidirectional Pins

PPS selections for peripherals with bidirectional signals on a single pin must be made so that the PPS input and PPS output select the same pin. Peripherals that have bidirectional signals include:

- EUSART (DT/RXxPPS and TX/CKxPPS pins for synchronous operation)
- MSSP (I^2C SDA/SSPxDATPPS and SCL/SSPxCLKPPS)

Important: The I^2C default inputs, and a limited number of other alternate pins, are I^2C and SMBus compatible. Clock and data signals can be routed to any pin, however pins without I^2C compatibility will operate at standard TTL/ST logic levels as selected by the INLVL register. See the INLVL register for each port to determine which pins are I^2C and SMBus compatible.

15.4 PPS Lock

The PPS includes a mode in which all input and output selections can be locked to prevent inadvertent changes. PPS selections are locked by setting the PPSLOCKED bit of the PPSLOCK register. Setting and clearing this bit requires a special sequence as an extra precaution against inadvertent changes. Examples of setting and clearing the PPSLOCKED bit are shown in the following examples.

Example 15-1. PPS Lock Sequence

```
; suspend interrupts
   BCF      INTCON,GIE
   BANKSEL  PPSLOCK ; set bank
```

Table 20-3. ADC Auto-Conversion Trigger Sources

ACT	Auto-conversion Trigger Source
11111	Software write to ADPCH
11110	Reserved, do not use
11101	Software read of ADRESH
11100	Software read of ADERRH
11011	Reserved, do not use
11010	Reserved, do not use
11001	SMT2_trigger
11000	CCP5_trigger
10111	CLC4_out
10110	CLC3_out
10101	CLC2_out
10100	CLC1_out
10011	Logical OR of all Interrupt-on-change Interrupt Flags
10010	C2_out
10001	C1_out
10000	NCO1_out
01111	PWM7_out
01110	PWM6_out
01101	CCP4_trigger
01100	CCP3_trigger
01011	CCP2_trigger
01010	CCP1_trigger
01001	SMT1_trigger
01000	TMR6_postscaled
00111	TMR5_overflow
00110	TMR4_postscaled
00101	TMR3_overflow
00100	TMR2_postscaled
00011	TMR1_overflow
00010	TMR0_overflow

20.8 Register Definitions: ADC Control

Long bit name prefixes for the ADC peripherals are shown in the table below. Refer to the *"Long Bit Names Section"* for more information.

Table 20-7. ADC Long Bit Name Prefixes

Peripheral	Bit Name Prefix
ADC[2]	AD

Related Links

1.4.2.2 Long Bit Names

20.8.2 ADCON1

Name: ADCON1
Address: 0x112

ADC Control Register 1

Bit	7	6	5	4	3	2	1	0
	PPOL	IPEN	GPOL					DSEN
Access	R/W	R/W	R/W					R/W
Reset	0	0	0					0

Bit 7 – PPOL Precharge Polarity bit
Action During 1st Precharge Stage

Value	Condition	Description
x	PRE=0	Bit has no effect
1	PRE>0 & ADC input is I/O pin	Pin shorted to AV_{DD}
0	PRE>0 & ADC input is I/O pin	Pin shorted to V_{SS}
1	PRE>0 & ADC input is internal	C_{HOLD} Shorted to AV_{DD}
0	PRE>0 & ADC input is internal	C_{HOLD} Shorted to V_{SS}

Bit 6 – IPEN A/D Inverted Precharge Enable bit

Value	Condition	Description
x	DSEN = 0	Bit has no effect
1	DSEN = 1	The precharge and guard signals in the second conversion cycle are the opposite polarity of the first cycle
0	DSEN = 1	Both Conversion cycles use the precharge and guards specified by PPOL and GPOL

Bit 5 – GPOL Guard Ring Polarity Selection bit

Value	Description
1	ADC guard Ring outputs start as digital high during Precharge stage
0	ADC guard Ring outputs start as digital low during Precharge stage

Bit 0 – DSEN Double-Sample Enable bit

Value	Description
1	Two conversions are performed on each trigger. Data from the first conversion appears in PREV
0	One conversion is performed for each trigger

20.8.22 ADACT

Name: ADACT
Address: 0x117

ADC AUTO Conversion Trigger Source Selection Register

Bit	7	6	5	4	3	2	1	0
				ACT[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – ACT[4:0] Auto-Conversion Trigger Select Bits

Value	Description
00000 to 11111	See ADC Auto-Conversion Trigger Sources table.

28. CCP/PWM Timer Resource Selection

Each CCP/PWM module has an independent timer selection which can be accessed using the CxTSEL or PxTSEL bits in the CCPTMRS0 and/or CCPTMRS1 registers. The default timer selection is TMR1 when using Capture/Compare mode and T2TMR when using PWM mode in the CCPx module. The default timer selection for the PWM module is always T2TMR.

ISM	Data Source
0001	CCP1_out
0000	Pin selected by CWGxINPPS

31.6 Output Control

31.6.1 CWG Outputs

Each CWG output can be routed to a Peripheral Pin Select (PPS) output via the RxyPPS register.

Related Links

15. (PPS) Peripheral Pin Select Module

31.6.2 Polarity Control

The polarity of each CWG output can be selected independently. When the output polarity bit is set, the corresponding output is active-high. Clearing the output polarity bit configures the corresponding output as active-low. However, polarity does not affect the override levels. Output polarity is selected with the POLy bits. Auto-shutdown and steering options are unaffected by polarity.

31.7 Dead-Band Control

The dead-band control provides non-overlapping PWM signals to prevent shoot-through current in PWM switches. Dead-band operation is employed for Half-Bridge and Full-Bridge modes. The CWG contains two 6-bit dead-band counters. One is used for the rising edge of the input source control in Half-Bridge mode or for reverse dead-band Full-Bridge mode. The other is used for the falling edge of the input source control in Half-Bridge mode or for forward dead band in Full-Bridge mode.

Dead band is timed by counting CWG clock periods from zero up to the value in the rising or falling dead-band counter registers.

31.7.1 Dead-Band Functionality in Half-Bridge mode

In Half-Bridge mode, the dead-band counters dictate the delay between the falling edge of the normal output and the rising edge of the inverted output. This can be seen in Figure 31-1.

31.7.2 Dead-Band Functionality in Full-Bridge mode

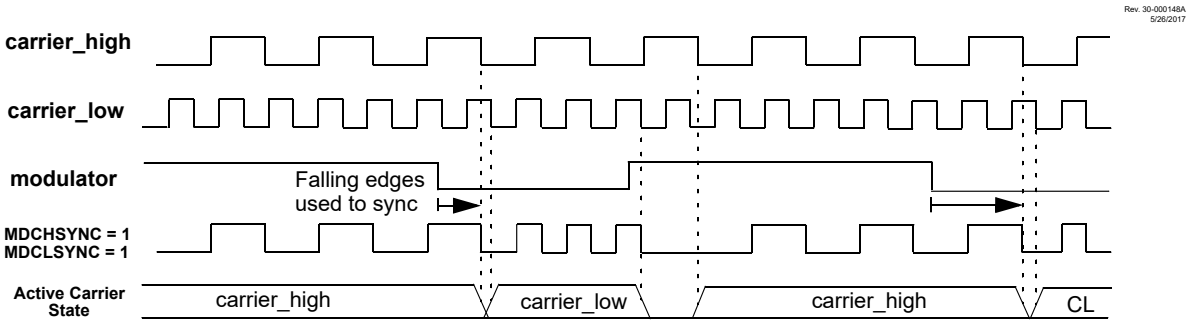
In Full-Bridge mode, the dead-band counters are used when undergoing a direction change. The MODE<0> bit can be set or cleared while the CWG is running, allowing for changes from Forward to Reverse mode. The CWGxA and CWGxC signals will change immediately upon the first rising input edge following a direction change, but the modulated signals (CWGxB or CWGxD, depending on the direction of the change) will experience a delay dictated by the dead-band counters.

31.8 Rising Edge and Reverse Dead Band

In Half-Bridge mode, the rising edge dead band delays the turn-on of the CWGxA output after the rising edge of the CWG data input. In Full-Bridge mode, the reverse dead-band delay is only inserted when changing directions from Forward mode to Reverse mode, and only the modulated output CWGxB is affected.

The 31.15.8 CWGxDBR register determines the duration of the dead-band interval on the rising edge of the input source signal. This duration is from 0 to 64 periods of the CWG clock.

Figure 32-6. Full Synchronization (MDCHSYNC = 1, MDCLSYNC = 1)



32.5 Carrier Source Polarity Select

The signal provided from any selected input source for the carrier high and carrier low signals can be inverted. Inverting the signal for the carrier high and low source is enabled by setting the CHPOL bit and the CLPOL bit, respectively.

32.6 Programmable Modulator Data

The BIT bit can be selected as the modulation source. This gives the user the ability to provide software driven modulation.

32.7 Modulated Output Polarity

The modulated output signal provided on the DSM pin can also be inverted. Inverting the modulated output signal is enabled by setting the OPOL bit.

32.8 Operation in Sleep Mode

The DSM can still operate during Sleep, if the Carrier and Modulator input sources are also still operable during Sleep. Refer to *"Power-Saving Operation Modes"* for more details.

32.9 Effects of a Reset

Upon any device Reset, the DSM module is disabled. The user's firmware is responsible for initializing the module before enabling the output. All the registers are reset to their default values.

32.10 Peripheral Module Disable

The DSM module can be completely disabled using the PMD module to achieve maximum power saving. When the DSMMD bit of PMDx register is set, the DSM module is completely disabled. This puts the module in its lowest power consumption state. When enabled again all the registers of the DSM module default to POR status.

Related Links

16.5 Register Definitions: Peripheral Module Disable

35.9.1 SSPxSTAT

Name: SSPxSTAT
Address: 0x18F,0x199

MSSP Status Register

Bit	7	6	5	4	3	2	1	0
	SMP	CKE	$\overline{D/A}$	P	S	$\overline{R/W}$	UA	BF
Access	R/W	R/W	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 7 – SMP Slew Rate Control bit

Value	Mode	Description
1	SPI Master	Input data is sampled at the end of data output time
0	SPI Master	Input data is sampled at the middle of data output time
0	SPI Slave	Keep this bit cleared in SPI Slave mode
1	I^2C	Slew rate control is disabled for Standard Speed mode (100 kHz and 1 MHz)
0	I^2C	Slew rate control is enabled for High-Speed mode (400 kHz)

Bit 6 – CKE

SPI: Clock select bit(4) I^2C: SMBus Select bit

Value	Mode	Description
1	SPI	Transmit occurs on the transition from active to Idle clock state
0	SPI	Transmit occurs on the transition from Idle to active clock state
1	I^2C	Enables SMBus-specific inputs
0	I^2C	Disables SMBus-specific inputs

Bit 5 – D/$\overline{A}$
Data/$\overline{Address}$ bit

Value	Mode	Description
x	SPI or I^2C Master	Reserved
1	I^2C Slave	Indicates that the last byte received or transmitted was data
0	I^2C Slave	Indicates that the last byte received or transmitted was address

Bit 4 – P
Stop bit(1)

Value	Mode	Description
x	SPI	Reserved
1	I^2C	Stop bit was detected last
0	I^2C	Stop bit was not detected last

Bit 3 – S
Start bit(1)

- TXEN = 1 (enables the transmitter circuitry of the EUSART)
- SYNC = 0 (configures the EUSART for asynchronous operation)
- SPEN = 1 (enables the EUSART and automatically enables the output drivers for the RxyPPS selected as the TXx/CKx output)

All other EUSART control bits are assumed to be in their default state.

If the TXx/CKx pin is shared with an analog peripheral, the analog I/O function must be disabled by clearing the corresponding ANSEL bit.

Important: The TXxIF Transmitter Interrupt flag is set when the TXEN enable bit is set and the TSR is idle.

36.1.1.2 Transmitting Data

A transmission is initiated by writing a character to the TXxREG register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXxREG is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TXxREG until the Stop bit of the previous character has been transmitted. The pending character in the TXxREG is then transferred to the TSR in one T_{CY} immediately following the Stop bit transmission. The transmission of the Start bit, data bits and Stop bit sequence commences immediately following the transfer of the data to the TSR from the TXxREG.

36.1.1.3 Transmit Data Polarity

The polarity of the transmit data can be controlled with the SCKP bit of the BAUDxCON register. The default state of this bit is '0' which selects high true transmit idle and data bits. Setting the SCKP bit to '1' will invert the transmit data resulting in low true idle and data bits. The SCKP bit controls transmit data polarity in Asynchronous mode only. In Synchronous mode, the SCKP bit has a different function. See the 36.3.1.2 Clock Polarity section for more detail.

36.1.1.4 Transmit Interrupt Flag

The TXxIF interrupt flag bit of the PIRx register is set whenever the EUSART transmitter is enabled and no character is being held for transmission in the TXxREG. In other words, the TXxIF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TXxREG. The TXxIF flag bit is not cleared immediately upon writing TXxREG. TXxIF becomes valid in the second instruction cycle following the write execution. Polling TXxIF immediately following the TXxREG write will return invalid results. The TXxIF bit is read-only, it cannot be set or cleared by software.

The TXxIF interrupt can be enabled by setting the TXxIE interrupt enable bit of the PIEx register. However, the TXxIF flag bit will be set whenever the TXxREG is empty, regardless of the state of TXxIE enable bit.

To use interrupts when transmitting data, set the TXxIE bit only when there is more data to send. Clear the TXxIE interrupt enable bit upon writing the last character of the transmission to the TXxREG.

36.1.1.5 TSR Status

The TRMT bit of the TXxSTA register indicates the status of the TSR register. This is a read-only bit. The TRMT bit is set when the TSR register is empty and is cleared when a character is transferred to the TSR register from the TXxREG. The TRMT bit remains clear until all bits have been shifted out of the TSR register. No interrupt logic is tied to this bit, so the user needs to poll this bit to determine the TSR status.

Address	Name	Bit Pos.								
0x1284	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1286	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1288	BSR	7:0			BSR[5:0]					
0x1289	WREG	7:0	WREG[7:0]							
0x128A	PCLATH	7:0		PCLATH[6:0]						
0x128B	INTCON	7:0	GIE	PEIE						INTEDG
0x128C ... 0x12FF	Reserved									
0x1300	INDF0	7:0	INDF0[7:0]							
0x1301	INDF1	7:0	INDF1[7:0]							
0x1302	PCL	7:0	PCL[7:0]							
0x1303	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1304	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1306	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1308	BSR	7:0			BSR[5:0]					
0x1309	WREG	7:0	WREG[7:0]							
0x130A	PCLATH	7:0		PCLATH[6:0]						
0x130B	INTCON	7:0	GIE	PEIE						INTEDG
0x130C ... 0x137F	Reserved									
0x1380	INDF0	7:0	INDF0[7:0]							
0x1381	INDF1	7:0	INDF1[7:0]							
0x1382	PCL	7:0	PCL[7:0]							
0x1383	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1384	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1386	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1388	BSR	7:0			BSR[5:0]					
0x1389	WREG	7:0	WREG[7:0]							
0x138A	PCLATH	7:0		PCLATH[6:0]						
0x138B	INTCON	7:0	GIE	PEIE						INTEDG
0x138C ... 0x13FF	Reserved									
0x1400	INDF0	7:0	INDF0[7:0]							
0x1401	INDF1	7:0	INDF1[7:0]							
0x1402	PCL	7:0	PCL[7:0]							
0x1403	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1404	FSR0	7:0	FSRL[7:0]							