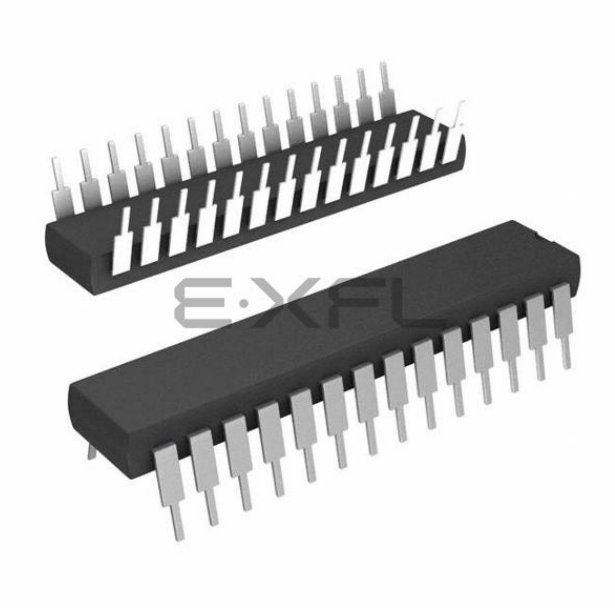

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18455-i-sp

Address Range	Name of Region	Standard Device Information
8118h	FVRA1X	ADC FVR1 Output voltage for 1x setting (in mV)
8119h	FVRA2X	ADC FVR1 Output Voltage for 2x setting (in mV)
811Ah	FVRA4X(1)	ADC FVR1 Output Voltage for 4x setting (in mV)
811Bh	FVRC1X	Comparator FVR2 output voltage for 1x setting (in mV)
811Ch	FVRC2X	Comparator FVR2 output voltage for 2x setting (in mV)
811Dh	FVRC4X(1)	Comparator FVR2 output voltage for 4x setting (in mV)
811Eh-811Fh		Unassigned (2 Words)

Note:
1. Value not present on LF devices.

5.1 Microchip Unique Identifier (MUI)

The PIC16(L)F184XX devices are individually encoded during final manufacturing with a Microchip Unique Identifier (MUI). The MUI cannot be erased by a Bulk Erase command or any other user-accessible means. This feature allows for manufacturing traceability of Microchip Technology devices in applications where this is required. It may also be used by the application manufacturer for a number of functions that require unverified unique identification, such as:

- Tracking the device
- Unique serial number

The MUI consists of nine program words and one reserved program word. When taken together, these fields form a unique identifier. The MUI is stored in read-only locations, located between 8100h to 8109h in the DIA space. The above table lists the addresses of the identifier words.

Important: For applications that require verified unique identification, contact your Microchip Technology sales office to create a serialized quick turn programming option.

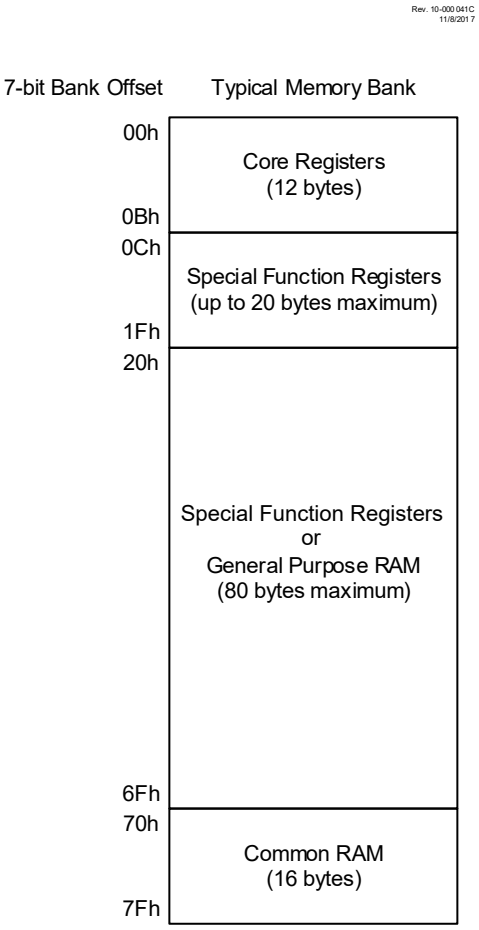
5.2 External Unique Identifier (EUI)

The EUI data is stored at locations 810Ah to 8111h in the program memory region. This region is an optional space for placing application specific information. The data is coded per customer requirements during manufacturing. The EUI cannot be erased by a Bulk Erase command.

Important: Data is stored in this address range on receiving a request from the customer. The customer may contact the local sales representative or Field Applications Engineer, and provide them the unique identifier information that is required to be stored in this region.

- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

Figure 7-2. Banked Memory Partition



7.3.1 Bank Selection

The active bank is selected by writing the bank number into the Bank Select Register (BSR). All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). Data memory uses a 13-bit address. The upper six bits of the address define the Bank address and the lower seven bits select the registers/RAM in that bank.

Related Links

7.6 Indirect Addressing

7.8.7 BSR

7.3.2 Core Registers

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses n00h/n80h through n0Bh/n8Bh). These registers are listed below.

10.7.7 PIE5

Name: PIE5
Address: 0x71B

Peripheral Interrupt Enable Register 5

Bit	7	6	5	4	3	2	1	0
	CLC4IE	CLC3IE	CLC2IE	CLC1IE		TMR5GIE	TMR3GIE	TMR1GIE
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit 7 – CLC4IE CLC4 Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 6 – CLC3IE CLC3 Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 5 – CLC2IE CLC2 Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 4 – CLC1IE CLC1 Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 2 – TMR5GIE TMR5 Gate Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 1 – TMR3GIE TMR3 Gate Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 0 – TMR1GIE TMR1 Gate Interrupt Enable bit

11.1.2 Interrupts During Doze

System behavior if an interrupt occurs during DOZE can be configured using the Recover-on-Interrupt (ROI) bit and the Doze-on-Exit (DOE) bit. Refer to the table below for details about system behavior in all cases for a transition from Main to ISR back to Main.

Table 11-1. Interrupts During DOZE

DOZEN	ROI	Code Flow			
		Main	ISR(1)	Return to Main	
0	0	Normal Operation	Normal operation and DOE = DOZEN (in hardware) DOZEN = 0 (unchanged)	If DOE = 1 when return from interrupt: DOZE operation and DOZEN = 1 (in hardware)	If DOE = 0 when return from interrupt: Normal operation and DOZEN = 0 (in hardware)
0	1	Normal Operation	Normal operation and DOE = DOZEN (in hardware) DOZEN = 0 (unchanged)		
1	0	DOZE operation	DOZE operation and DOE = DOZEN (in hardware) DOZEN = 1 (unchanged)		
1	1	DOZE operation	Normal operation and DOE = DOZEN (in hardware) DOZEN = 0 (unchanged)		

Note:

1. User software can change DOE bit in the ISR.

11.2 Sleep Mode

Sleep mode is entered by executing the SLEEP instruction, while the Idle Enable (IDLEN) bit of the CPUDOZE register is clear (IDLEN = 0).

Upon entering Sleep mode, the following conditions exist:

1. WDT will be cleared but keeps running if enabled for operation during Sleep
2. The $\overline{PD}$ bit of the STATUS register is cleared
3. The $\overline{TO}$ bit of the STATUS register is set
4. The CPU clock is disabled
5. LFINTOSC, SOSC, HFINTOSC and ADCRC are unaffected and peripherals using them may continue operation in Sleep.
6. I/O ports maintain the status they had before Sleep was executed (driving high, low, or high-impedance)
7. Resets other than WDT are not affected by Sleep mode

Refer to individual chapters for more details on peripheral operation during Sleep.

Related Links

11.1.2 Interrupts During Doze

16.4 Register Summary - PMD

Address	Name	Bit Pos.								
0x0796	PMD0	7:0	SYSCMD	FVRMD				NVMMD	CLKRMD	IOCMD
0x0797	PMD1	7:0		TMR6MD	TMR5MD	TMR4MD	TMR3MD	TMR2MD	TMR1MD	TMR0MD
0x0798	PMD2	7:0	NCO1MD							
0x0799	PMD3	7:0		DAC1MD	ADCMD			C2MD	C1MD	ZCDMD
0x079A	PMD4	7:0		PWM7MD	PWM6MD	CCP5MD	CCP4MD	CCP3MD	CCP2MD	CCP1MD
0x079B	PMD5	7:0	CWG3MD	CWG2MD	CWG1MD					
0x079C	PMD6	7:0			UART2MD	UART1MD			MSSP2MD	MSSP1MD
0x079D	PMD7	7:0		SMT2MD	SMT1MD	CLC4MD	CLC3MD	CLC2MD	CLC1MD	DSM1MD

16.5 Register Definitions: Peripheral Module Disable

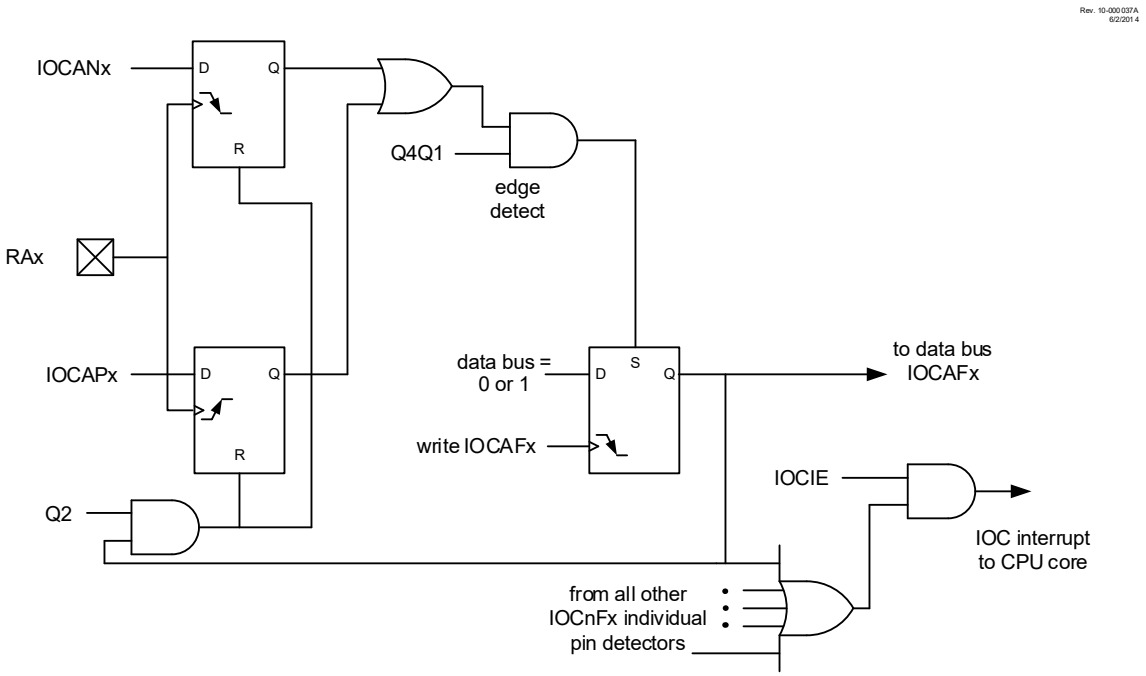
17. Interrupt-on-Change

An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual pin, or combination of pins, can be configured to generate an interrupt. The interrupt-on-change module has the following features:

- Interrupt-on-Change enable (Master Switch)
- Individual pin configuration
- Rising and falling edge detection
- Individual pin interrupt flags

The following figure is a block diagram of the IOC module.

Figure 17-1. Interrupt-on-Change Block Diagram (PORTA Example)



Note: See link below for BOR Active Conditions.

Related Links

8.2.3 BOR Controlled by Software

17.1 Enabling the Module

To allow individual port pins to generate an interrupt, the IOCIE bit of the PIE0 register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

Related Links

10.7.2 PIE0

17.5 Register Summary - Interrupt-on-Change

Address	Name	Bit Pos.								
0x1F3D	IOCAP	7:0	IOCAP7	IOCAP6	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0
0x1F3E	IOCAN	7:0	IOCAN7	IOCAN6	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0
0x1F3F	IOCAF	7:0	IOCAF7	IOCAF6	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0
0x1F40 ... 0x1F47	Reserved									
0x1F48	IOCBP	7:0	IOCBP7	IOCBP6	IOCBP5	IOCBP4	IOCBP3	IOCBP2	IOCBP1	IOCBP0
0x1F49	IOCBN	7:0	IOCBN7	IOCBN6	IOCBN5	IOCBN4	IOCBN3	IOCBN2	IOCBN1	IOCBN0
0x1F4A	IOCBF	7:0	IOCBF7	IOCBF6	IOCBF5	IOCBF4	IOCBF3	IOCBF2	IOCBF1	IOCBF0
0x1F4B ... 0x1F52	Reserved									
0x1F53	IOCCP	7:0	IOCCP7	IOCCP6	IOCCP5	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0
0x1F54	IOCCN	7:0	IOCCN7	IOCCN6	IOCCN5	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0
0x1F55	IOCCF	7:0	IOCCF7	IOCCF6	IOCCF5	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0
0x1F56 ... 0x1F68	Reserved									
0x1F69	IOCEP	7:0					IOCEP3			
0x1F6A	IOCEN	7:0					IOCEN3			
0x1F6B	IOCEF	7:0					IOCEF3			

17.6 Register Definitions: Interrupt-on-Change Control

20.8.14 ADFLTR

Name: ADFLTR
Address: 0x094

ADC Filter Register

Bit	15	14	13	12	11	10	9	8
	FLTRH[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	x	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	FLTRL[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	x	x	x	x	x	x	x	x

Bits 15:8 – FLTRH[7:0] ADC Filter Output Most Significant bits
In Accumulate, Average, and Burst Average mode, this is equal to ADACC right shifted by the CRS bits.
In LPF mode, this is the output of the low-pass filter.

Bits 7:0 – FLTRL[7:0] ADC Filter Output Least Significant bits
In Accumulate, Average, and Burst Average mode, this is equal to ADACC right shifted by the CRS bits.
In LPF mode, this is the output of the low-pass filter.

29. Capture/Compare/PWM Module

The Capture/Compare/PWM module is a peripheral that allows the user to time and control different events, and to generate Pulse-Width Modulation (PWM) signals. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate Pulse-Width Modulated signals of varying frequency and duty cycle.

This family of devices contains five standard Capture/Compare/PWM modules (CCP1, CCP2, CCP3, CCP4 and CCP5). It should be noted that the Capture/Compare mode operation is described with respect to TMR1 and the PWM mode operation is described with respect to T2TMR in the following sections.

The Capture and Compare functions are identical for all CCP modules.

Important:

1. In devices with more than one CCP module, it is very important to pay close attention to the register names used. A number placed after the module acronym is used to distinguish between separate modules. For example, the CCP1CON and CCP2CON control the same operational aspects of two completely different CCP modules.
2. Throughout this section, generic references to a CCP module in any of its operating modes may be interpreted as being equally applicable to CCPx module. Register names, module signals, I/O pins, and bit names may use the generic designator ‘x’ to indicate the use of a numeral to distinguish a particular module, when required.

29.1 CCP Module Configuration

Each Capture/Compare/PWM module is associated with a control register (CCPxCON), a capture input selection register (CCPxCAP) and a data register (CCPRx). The data register, in turn, is comprised of two 8-bit registers: CCPRxL (low byte) and CCPRxH (high byte).

29.1.1 CCP Modules and Timer Resources

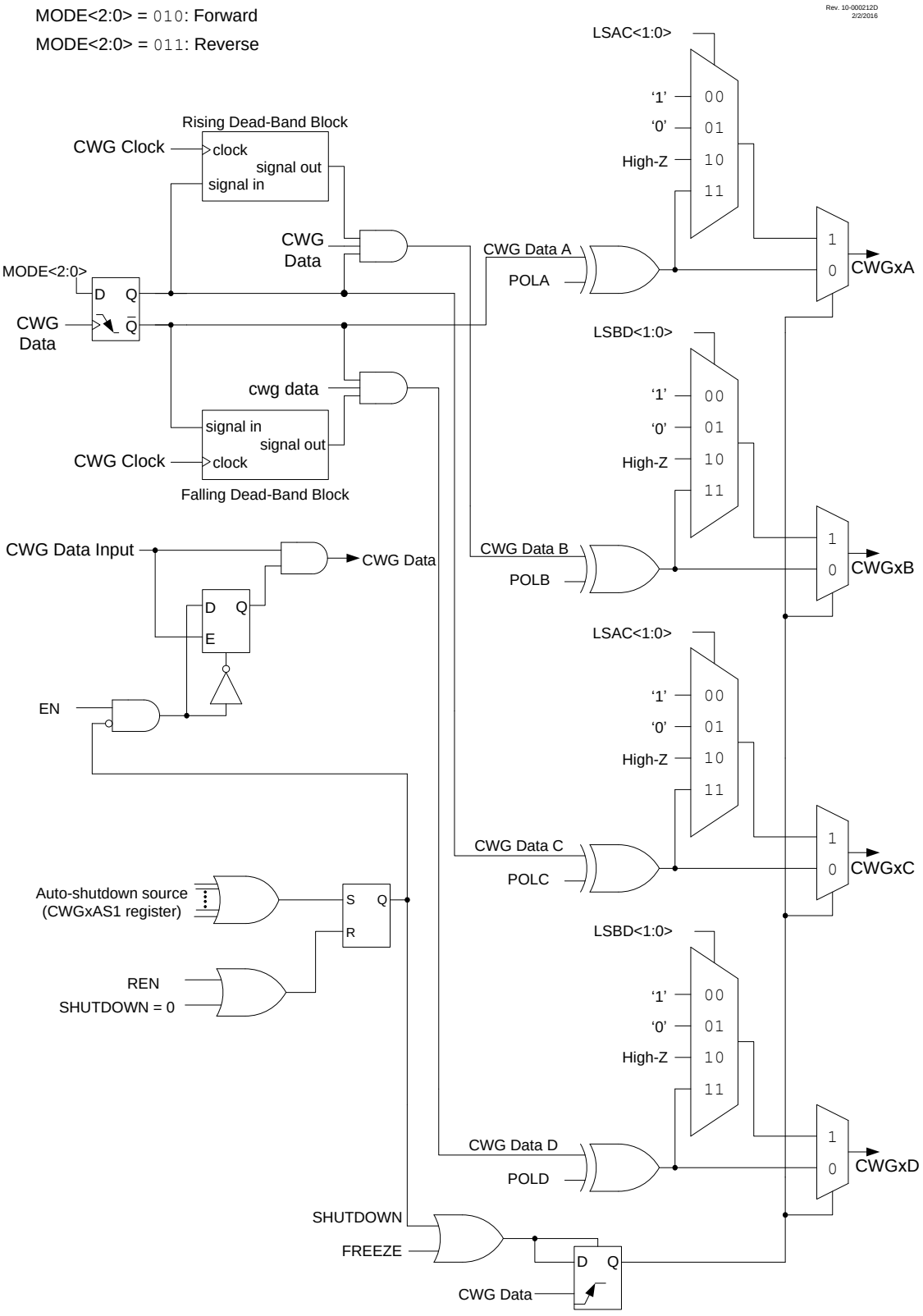
The CCP modules utilize Timers 1 through 6 that vary with the selected mode. Various timers are available to the CCP modules in Capture, Compare or PWM modes, as shown in the table below.

Table 29-1. CCP Mode - Timer Resources

CCP Mode	Timer Resource
Capture	Timer1, Timer3 or Timer5
Compare	
PWM	Timer2, Timer4 or Timer6

The assignment of a particular timer to a module is determined by the timer to CCP enable bits in the CCPTMRS0 and/or CCPTMRS1 registers. All of the modules may be active at once and may share the same timer resource if they are configured to operate in the same mode (Capture/Compare or PWM) at the same time.

Figure 31-6. Simplified CWG Block Diagram (Forward and Reverse Full-Bridge Modes)



31.10 Dead-Band Jitter

When the rising and falling edges of the input source are asynchronous to the CWG clock, it creates jitter in the dead-band time delay. The maximum jitter is equal to one CWG clock period. Refer to the equations below for more details.

Equation 31-1. Dead-Band Delay Time Calculation

$$T_{DEAD-BAND\_MIN} = \frac{1}{F_{CWG\_CLOCK}} \bullet DBx<5:0>$$

$$T_{DEAD-BAND\_MAX} = \frac{1}{F_{CWG\_CLOCK}} \bullet DBx<5:0> + 1$$

$$T_{JITTER} = T_{DEAD-BAND\_MAX} - T_{DEAD-BAND\_MIN}$$

$$T_{JITTER} = \frac{1}{F_{CWG\_CLOCK}}$$

$$T_{DEAD-BAND\_MAX} = T_{DEAD-BAND\_MIN} + T_{JITTER}$$

Equation 31-2. Dead-Band Delay Example Calculation

$$DBx<5:0> = 0x0A = 10$$

$$F_{CWG\_CLOCK} = 8\,MHz$$

$$T_{JITTER} = \frac{1}{8\,MHz} = 125ns$$

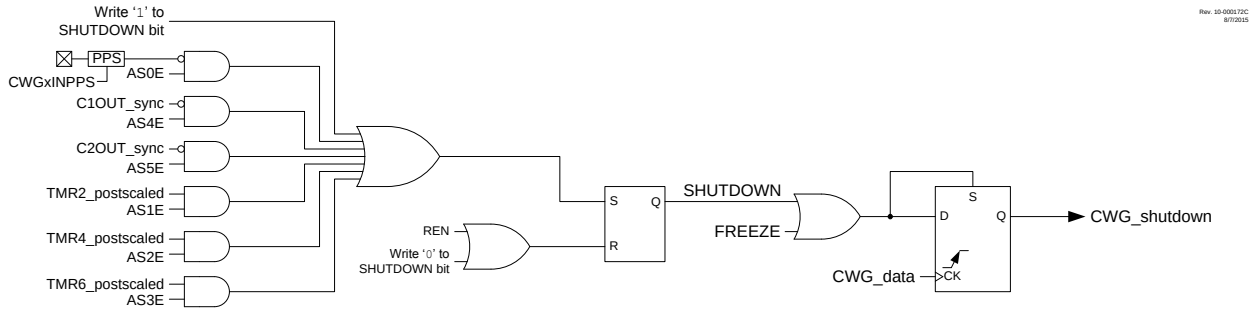
$$T_{DEAD-BAND\_MIN} = 125ns \bullet 10 = 125\mu s$$

$$T_{DEAD-BAND\_MAX} = 1.25\mu s + 0.125\,\mu s = 1.37\mu s$$

31.11 Auto-Shutdown

Auto-shutdown is a method to immediately override the CWG output levels with specific overrides that allow for safe shutdown of the circuit. The shutdown state can be either cleared automatically or held until cleared by software. The auto-shutdown circuit is illustrated in the following figure.

Figure 31-14. CWG Shutdown Block Diagram



31.11.1 Shutdown

The shutdown state can be entered by either of the following two methods:

- Software Generated

33.8.6 CLCxSEL3

Name: CLCxSEL3
Address: 0x1E15,0x1E1F,0x1E29,0x1E33

Generic CLCx Data 4 Select Register

Bit	7	6	5	4	3	2	1	0
			D4S[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			x	x	x	x	x	x

Bits 5:0 – D4S[5:0]
CLCx Data4 Input Selection bits
Reset States: POR/BOR = xxxxxx
All Other Resets = uuuuuu

Value	Description
n	Refer to CLC Input Sources for input selections

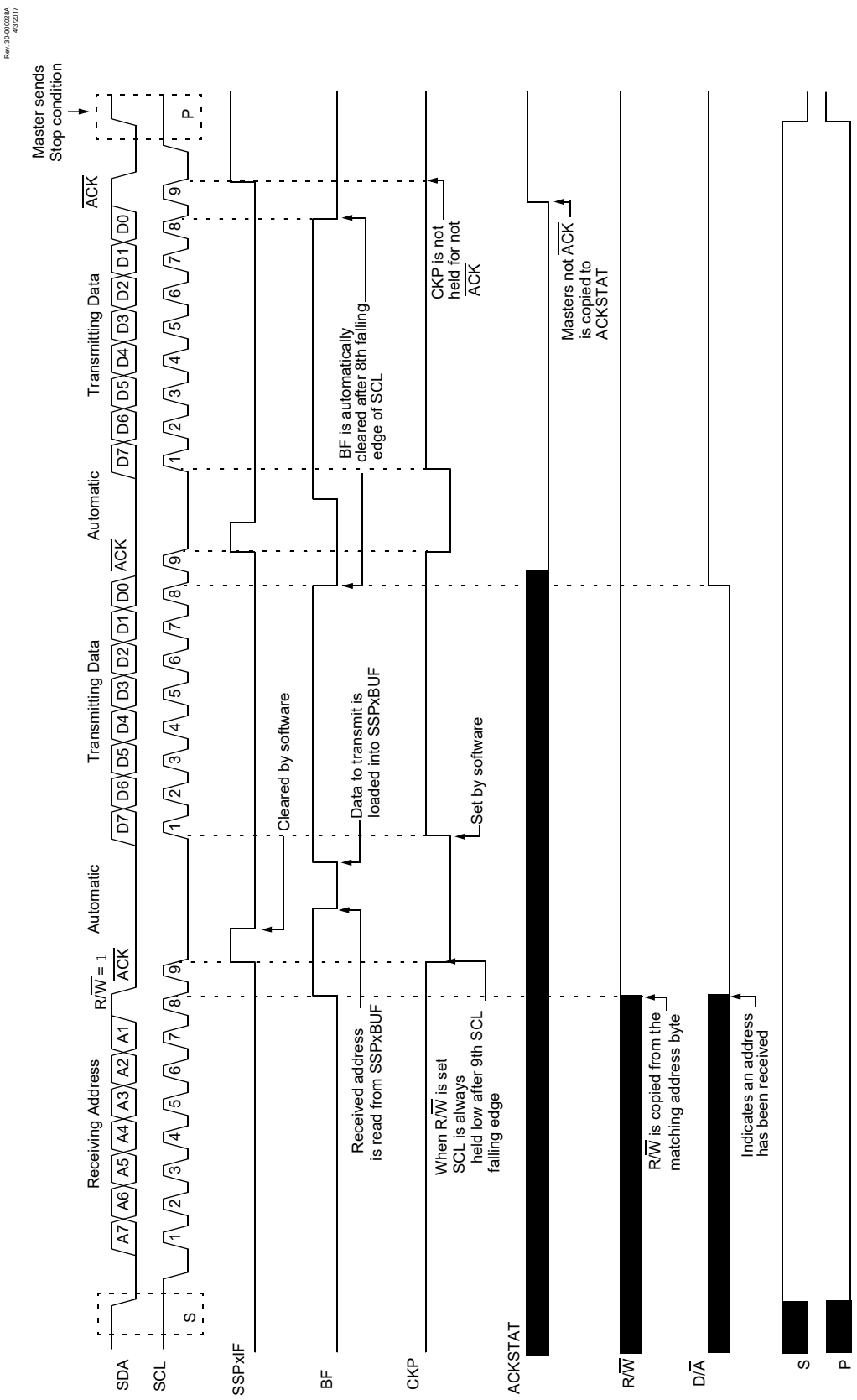


Figure 35-18. I²C Slave, 7-bit Address, Transmission (AHEN = 0)

37.2 Register Summary - SMT Control

Address	Name	Bit Pos.								
0x048C	SMT1TMR	7:0	TMRL[7:0]							
		15:8	TMRH[7:0]							
		23:16	TMRU[7:0]							
0x048F	SMT1CPR	7:0	CPRL[7:0]							
		15:8	CPRH[7:0]							
		23:16	CPRU[7:0]							
0x0492	SMT1CPW	7:0	CPWL[7:0]							
		15:8	CPWH[7:0]							
		23:16	CPWU[7:0]							
0x0495	SMT1PR	7:0	PRL[7:0]							
		15:8	PRH[7:0]							
		23:16	PRU[7:0]							
0x0498	SMT1CON0	7:0	EN		STP	WPOL	SPOL	CPOL	PS[1:0]	
0x0499	SMT1CON1	7:0	GO	REPEAT			MODE[3:0]			
0x049A	SMT1STAT	7:0	CPRUP	CPWUP		RST		TS	WS	AS
0x049B	SMT1CLK	7:0						CSEL[2:0]		
0x049C	SMT1SIG	7:0				SSEL[4:0]				
0x049D	SMT1WIN	7:0				WSEL[4:0]				
0x049E ... 0x050B	Reserved									
0x050C	SMT2TMR	7:0	TMRL[7:0]							
		15:8	TMRH[7:0]							
		23:16	TMRU[7:0]							
0x050F	SMT2CPR	7:0	CPRL[7:0]							
		15:8	CPRH[7:0]							
		23:16	CPRU[7:0]							
0x0512	SMT2CPW	7:0	CPWL[7:0]							
		15:8	CPWH[7:0]							
		23:16	CPWU[7:0]							
0x0515	SMT2PR	7:0	PRL[7:0]							
		15:8	PRH[7:0]							
		23:16	PRU[7:0]							
0x0518	SMT2CON0	7:0	EN		STP	WPOL	SPOL	CPOL	PS[1:0]	
0x0519	SMT2CON1	7:0	GO	REPEAT			MODE[3:0]			
0x051A	SMT2STAT	7:0	CPRUP	CPWUP		RST		TS	WS	AS
0x051B	SMT2CLK	7:0						CSEL[2:0]		
0x051C	SMT2SIG	7:0				SSEL[4:0]				
0x051D	SMT2WIN	7:0				WSEL[4:0]				

37.3 Register Definitions: SMT Control

Address	Name	Bit Pos.								
0x1EBE	CLCIN3PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBF ... 0x1EC2	Reserved									
0x1EC3	ADACTPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC4	Reserved									
0x1EC5	SSP1CLKPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC6	SSP1DATPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC7	SSP1SSPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC8	SSP2CLKPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC9	SSP2DATPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECA	SSP2SSPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECB	RX1PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECC	CK1PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECD	RX2PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECE	CK2PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECF ... 0x1EFF	Reserved									
0x1F00	INDF0	7:0	INDF0[7:0]							
0x1F01	INDF1	7:0	INDF1[7:0]							
0x1F02	PCL	7:0	PCL[7:0]							
0x1F03	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1F04	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1F06	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1F08	BSR	7:0			BSR[5:0]					
0x1F09	WREG	7:0	WREG[7:0]							
0x1F0A	PCLATH	7:0		PCLATH[6:0]						
0x1F0B	INTCON	7:0	GIE	PEIE						INTEDG
0x1F0C ... 0x1F0F	Reserved									
0x1F10	RA0PPS	7:0			PPS[5:0]					
0x1F11	RA1PPS	7:0			PPS[5:0]					
0x1F12	RA2PPS	7:0			PPS[5:0]					
0x1F13	RA3PPS	7:0			PPS[5:0]					
0x1F14	RA4PPS	7:0			PPS[5:0]					
0x1F15	RA5PPS	7:0			PPS[5:0]					
0x1F16	RA6PPS	7:0			PPS[5:0]					
0x1F17	RA7PPS	7:0			PPS[5:0]					
0x1F18	RB0PPS	7:0			PPS[5:0]					
0x1F19	RB1PPS	7:0			PPS[5:0]					
0x1F1A	RB2PPS	7:0			PPS[5:0]					
0x1F1B	RB3PPS	7:0			PPS[5:0]					

Address	Name	Bit Pos.								
0x1F1C	RB4PPS	7:0			PPS[5:0]					
0x1F1D	RB5PPS	7:0			PPS[5:0]					
0x1F1E	RB6PPS	7:0			PPS[5:0]					
0x1F1F	RB7PPS	7:0			PPS[5:0]					
0x1F20	RC0PPS	7:0			PPS[5:0]					
0x1F21	RC1PPS	7:0			PPS[5:0]					
0x1F22	RC2PPS	7:0			PPS[5:0]					
0x1F23	RC3PPS	7:0			PPS[5:0]					
0x1F24	RC4PPS	7:0			PPS[5:0]					
0x1F25	RC5PPS	7:0			PPS[5:0]					
0x1F26	RC6PPS	7:0			PPS[5:0]					
0x1F27	RC7PPS	7:0			PPS[5:0]					
0x1F28 ... 0x1F37	Reserved									
0x1F38	ANSELA	7:0	ANSELA7	ANSELA6	ANSELA5	ANSELA4	ANSELA3	ANSELA2	ANSELA1	ANSELA0
0x1F39	WPUA	7:0	WPUA7	WPUA6	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0
0x1F3A	ODCONA	7:0	ODCA7	ODCA6	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0
0x1F3B	SLRCONA	7:0	SLRA7	SLRA6	SLRA5	SLRA4	SLRA3	SLRA2	SLRA1	SLRA0
0x1F3C	INLVLA	7:0	INLVLA7	INLVLA6	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0
0x1F3D	IOCAP	7:0	IOCAP7	IOCAP6	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0
0x1F3E	IOCAN	7:0	IOCAN7	IOCAN6	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0
0x1F3F	IOCAF	7:0	IOCAF7	IOCAF6	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0
0x1F40 ... 0x1F42	Reserved									
0x1F43	ANSELB	7:0	ANSELB7	ANSELB6	ANSELB5	ANSELB4	ANSELB3	ANSELB2	ANSELB1	ANSELB0
0x1F44	WPUB	7:0	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0
0x1F45	ODCONB	7:0	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0
0x1F46	SLRCONB	7:0	SLRB7	SLRB6	SLRB5	SLRB4	SLRB3	SLRB2	SLRB1	SLRB0
0x1F47	INLVLB	7:0	INLVLB7	INLVLB6	INLVLB5	INLVLB4	INLVLB3	INLVLB2	INLVLB1	INLVLB0
0x1F48	IOCBP	7:0	IOCBP7	IOCBP6	IOCBP5	IOCBP4	IOCBP3	IOCBP2	IOCBP1	IOCBP0
0x1F49	IOCBN	7:0	IOCBN7	IOCBN6	IOCBN5	IOCBN4	IOCBN3	IOCBN2	IOCBN1	IOCBN0
0x1F4A	IOCBF	7:0	IOCBF7	IOCBF6	IOCBF5	IOCBF4	IOCBF3	IOCBF2	IOCBF1	IOCBF0
0x1F4B ... 0x1F4D	Reserved									
0x1F4E	ANSELC	7:0	ANSELC7	ANSELC6	ANSELC5	ANSELC4	ANSELC3	ANSELC2	ANSELC1	ANSELC0
0x1F4F	WPUC	7:0	WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0
0x1F50	ODCONC	7:0	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0
0x1F51	SLRCONC	7:0	SLRC7	SLRC6	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0
0x1F52	INLVLC	7:0	INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0
0x1F53	IOCCP	7:0	IOCCP7	IOCCP6	IOCCP5	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0
0x1F54	IOCCN	7:0	IOCCN7	IOCCN6	IOCCN5	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0
0x1F55	IOCCF	7:0	IOCCF7	IOCCF6	IOCCF5	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0
0x1F56	Reserved									

42.4.9 Comparator Specifications

Table 42-15.

Standard Operating Conditions (unless otherwise stated) V_{DD} = 3.0V, T_A = 25°C							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ. †**	**Max.**	**Units**	**Conditions**
CM01	V_{IOFF}	Input Offset Voltage	—	±30	—	mV	$V_{ICM} = V_{DD}/2$
CM02	V_{ICM}	Input Common Mode Range	GND	—	V_{DD}	V	
CM03	CMRR	Common Mode Input Rejection Ratio	—	50	—	dB	
CM04	V_{HYST}	Comparator Hysteresis	15	25	35	mV	
CM05	T_{RESP}(1)	Response Time, Rising Edge	—	300	600	ns	
		Response Time, Falling Edge	—	220	500	ns	
CM06*	T_{MCV2VO}(2)	Mode Change to Valid Output	—	—	10	ns	

* - These parameters are characterized but not tested.

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:

1. Response time measured with one comparator input at $V_{DD}/2$, while the other input transitions from V_{SS} to V_{DD}.
2. A mode change includes changing any of the control register values, including module enable.

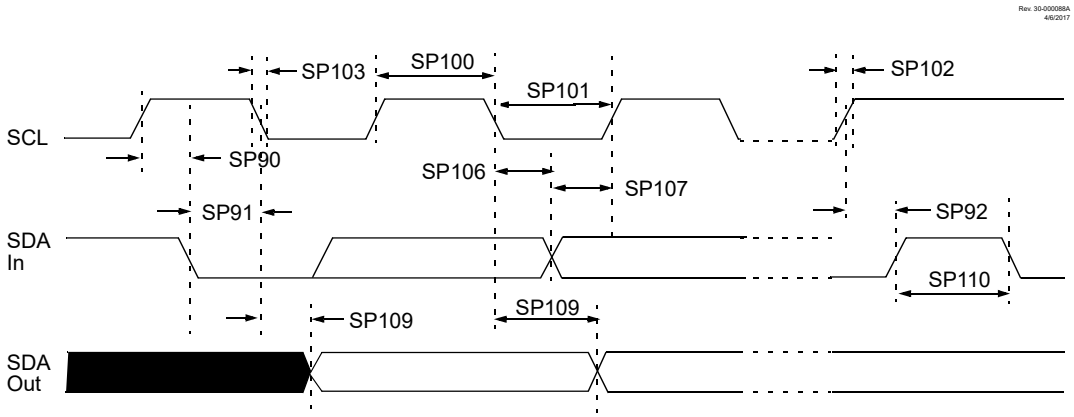
42.4.10 5-Bit DAC Specifications

Table 42-16.

Standard Operating Conditions (unless otherwise stated) V_{DD} = 3.0V, T_A = 25°C							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ. †**	**Max.**	**Units**	**Conditions**
DSB01	V_{LSB}	Step Size	—	($V_{DACREF+}$ - $V_{DACREF-}$)/32	—	V	
DSB02	V_{ACC}	Absolute Accuracy	—	—	±0.5	LSb	

Standard Operating Conditions (unless otherwise stated)						
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Conditions
		if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line TR max. + $T_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification), before the SCL line is released.				

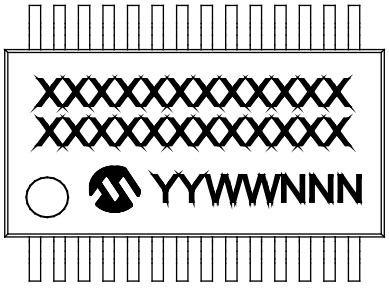
Figure 42-22. I^2C Bus Data Timing



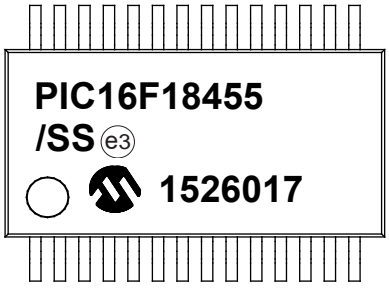
Note: Refer to Figure 42-4 for load conditions.

Rev. 30-009028C
5/17/2017

28-Lead SSOP (5.30 mm)

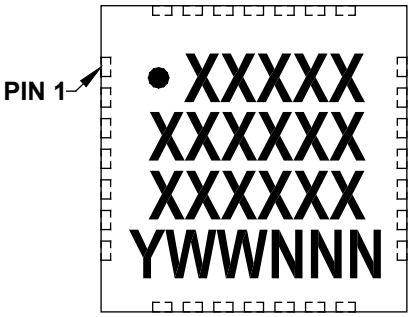


Example

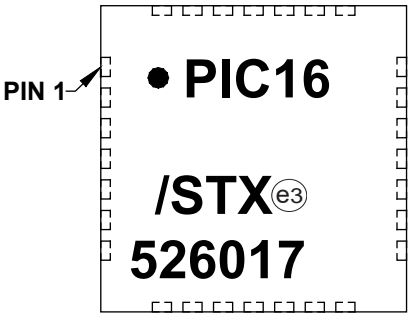


Rev. 30-009028F
4/2/2018

28-Lead VQFN (4x4x1 mm)



Example



44.1 Package Details

The following sections give the technical details of the packages.