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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18455t-i-ss

7.8.3 PCL

Name: PCL
Address: 0x02 + n*0x80 [n=0..63]

Low byte of the Program Counter

Bit	7	6	5	4	3	2	1	0
	PCL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – PCL[7:0]
Provides direct read and write access to the Program Counter

10.7.18 PIR7

Name: PIR7
Address: 0x713

Peripheral Interrupt Request (Flag) Register 7

Bit	7	6	5	4	3	2	1	0
			NVMIF	NCO1IF		CWG3IF	CWG2IF	CWG1IF
Access			R/W/HS	R/W/HS		R/W/HS	R/W/HS	R/W/HS
Reset			0	0		0	0	0

Bit 5 – NVMIF NVM Interrupt Flag bit

Value	Description
1	The requested NVM operation has completed
0	NVM interrupt not asserted

Bit 4 – NCO1IF Numerically Controlled Oscillator (NCO) Interrupt Flag bit

Value	Description
1	The NCO has rolled over
0	No NCO interrupt event has occurred

Bit 2 – CWG3IF CWG3 Interrupt Flag bit

Value	Description
1	CWG3 has gone into shutdown
0	CWG3 is operating normally, or interrupt cleared

Bit 1 – CWG2IF CWG2 Interrupt Flag bit

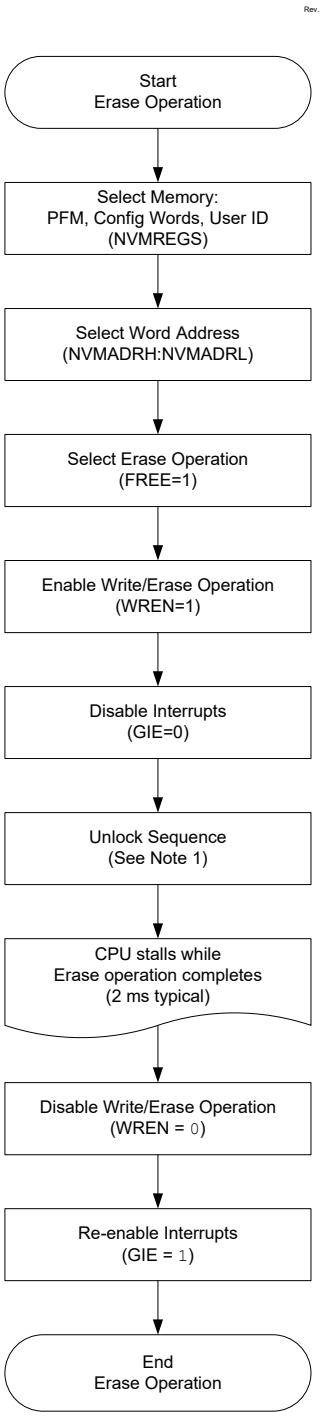
Value	Description
1	CWG2 has gone into shutdown
0	CWG2 is operating normally, or interrupt cleared

Bit 0 – CWG1IF CWG1 Interrupt Flag bit

Value	Description
1	CWG1 has gone into shutdown
0	CWG1 is operating normally, or interrupt cleared

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON appropriate interrupt flag bits are clear prior to enabling an interrupt.

Figure 13-3. NVM Erase Flowchart



Note: See previous figure.

Example 13-3. Erasing One Row of Program Flash Memory

```
; This sample row erase routine assumes the following:
; 1.A valid address within the erase row is loaded in variables ADDRH:ADDRL
; 2.ADDRH and ADDRL are located in common RAM (locations 0x70 - 0x7F)
```

14.7.26 INLVLC

Name: INLVLC
Address: 0x1F52

Input Level Control Register

Bit	7	6	5	4	3	2	1	0
	INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 0, 1, 2, 3, 4, 5, 6, 7 – INLVLCn Input Level Select on Pins Rx<7:0>, respectively
Note: INLVLC4 / INLVLC3: Pins read the I^2C ST inputs when MSSP inputs select these pins, and I^2C mode is enabled.

Value	Description
1	ST input used for port reads and interrupt-on-change
0	TTL input used for port reads and interrupt-on-change

PCH	ADC Positive Channel Input
001110	RB6/ANB6
001101	RB5/ANB5
001100	RB4/ ANB4
001011	RB3/ANB3
001010	RB2/ ANB2
001001	RB1/ ANB1
001000	RB0/ANB0
000111	RA7/ANA7
000110	RA6/ANA6
000101	RA5/ANA5
000100	RA4/ANA4
000011	RA3/ANA3
000010	RA2/ ANA2
000001	RA1/ ANA1
000000	RA0/ANA0

Related Links

20.2 ADC Operation

18. (FVR) Fixed Voltage Reference

19. Temperature Indicator Module

21. (DAC) 5-Bit Digital-to-Analog Converter Module

20.1.3 ADC Voltage Reference

The PREF bits provide control of the positive voltage reference. The positive voltage reference can be:

- V_{REF}+ pin
- V_{DD}
- FVR 1.024V
- FVR 2.048V
- FVR 4.096V

The NREF bit provides control of the negative voltage reference. The negative voltage reference can be:

- V_{REF}- pin
- V_{SS}

Related Links

18. (FVR) Fixed Voltage Reference

20.8.7 ADREF

If SOI = 1, a threshold interrupt condition will clear GO and the conversions will stop.

20.6.9 Double Sample Conversion

Double sampling is enabled by setting the DSEN bit. When this bit is set, two conversions are required before the module will calculate threshold error (each conversion must still be triggered separately). The first conversion will set the MATH bit and update ADACC, but will not calculate ADERR or trigger ADTIF. When the second conversion completes, the first value is transferred to ADPREV (depending on the setting of PSIS) and the value of the second conversion is placed into ADRES. Only upon the completion of the second conversion is ADERR calculated and ADTIF triggered (depending on the value of CALC).

20.8.14 ADFLTR

Name: ADFLTR
Address: 0x094

ADC Filter Register

Bit	15	14	13	12	11	10	9	8
	FLTRH[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	x	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	FLTRL[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	x	x	x	x	x	x	x	x

Bits 15:8 – FLTRH[7:0] ADC Filter Output Most Significant bits
In Accumulate, Average, and Burst Average mode, this is equal to ADACC right shifted by the CRS bits.
In LPF mode, this is the output of the low-pass filter.

Bits 7:0 – FLTRL[7:0] ADC Filter Output Least Significant bits
In Accumulate, Average, and Burst Average mode, this is equal to ADACC right shifted by the CRS bits.
In LPF mode, this is the output of the low-pass filter.

23.2.1 Comparator Enable

Setting the EN bit enables the comparator for operation. Clearing the CxEN bit disables the comparator, resulting in minimum current consumption.

23.2.2 Comparator Output

The output of the comparator can be monitored by reading either the CxOUT bit or the MCxOUT bit.

The comparator output can also be routed to an external pin through the RxyPPS register. The corresponding TRIS bit must be clear to enable the pin as an output.

Note:

1. The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

Related Links

15.9.2 RxyPPS

23.2.3 Comparator Output Polarity

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit. Clearing the CxPOL bit results in a non-inverted output.

Table 23-1 shows the output state versus input conditions, including polarity control.

Table 23-1. Comparator Output State vs. Input Conditions

Input Condition	CxPOL	CxOUT
CxVn > CxVp	0	0
CxVn < CxVp	0	1
CxVn > CxVp	1	1
CxVn < CxVp	1	0

23.3 Comparator Hysteresis

A selectable amount of separation voltage can be added to the input pins of each comparator to provide a hysteresis function to the overall operation. Hysteresis is enabled by setting the CxHYS bit.

See Comparator Specifications for more information.

Related Links

42.4.9 Comparator Specifications

23.4 Operation With Timer1 Gate

The output resulting from a comparator operation can be used as a source for gate control of the odd numbered timers (Timer1, Timer3, etc.). See the timer gate section for more information. This feature is useful for timing the duration or interval of an analog event.

It is recommended that the comparator output be synchronized to the timer by setting the SYNC bit. This ensures that the timer does not increment while a change in the comparator is occurring. However,

24.10 Register Summary: ZCD Control

Address	Name	Bit Pos.								
0x091F	ZCDCON	7:0	SEN		OUT	POL			INTP	INTN

24.11 Register Definitions: ZCD Control

Long bit name prefixes for the ZCD peripherals are shown in the table below. Refer to the *"Long Bit Names Section"* for more information.

Table 24-1. ZCD Long Bit Name Prefixes

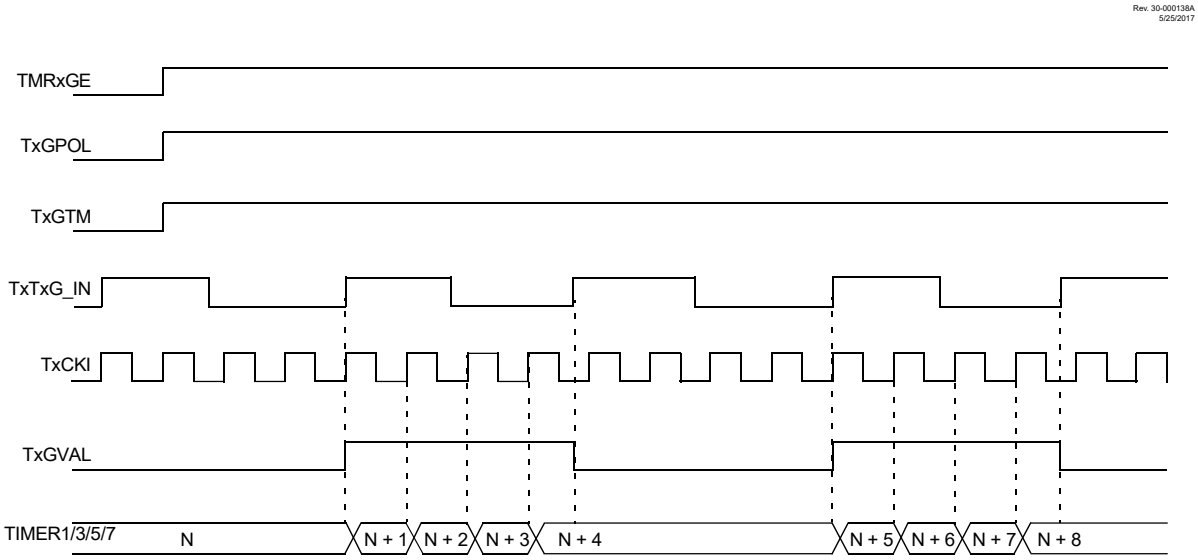
Peripheral	Bit Name Prefix
ZCD	ZCD

Related Links

1.4.2.2 Long Bit Names

1.4.2.2 Long Bit Names

Figure 26-5. TIMER1 GATE TOGGLE MODE



26.7.4 Timer1 Gate Single-Pulse Mode

When Timer1 Gate Single-Pulse mode is enabled, it is possible to capture a single-pulse gate event. Timer1 Gate Single-Pulse mode is first enabled by setting the GSPM bit. Next, the GGO/DONE must be set. The Timer1 will be fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the GGO/$\overline{\text{DONE}}$ bit will automatically be cleared. No other gate events will be allowed to increment Timer1 until the GGO/$\overline{\text{DONE}}$ bit is once again set in software.

Clearing the GSPM bit will also clear the GGO/$\overline{\text{DONE}}$ bit. See figure below for timing details.

Enabling the Toggle mode and the Single-Pulse mode simultaneously will permit both sections to work together. This allows the cycle times on the Timer1 gate source to be measured. See figure below for timing details.

31.3 Start-up Considerations

The application hardware must use the proper external pull-up and/or pull-down resistors on the CWG output pins. This is required because all I/O pins are forced to high-impedance at Reset.

The polarity control bits (POLy) allow the user to choose whether the output signals are active-high or active-low.

31.4 Clock Source

The clock source is used to drive the dead-band timing circuits. The CWG module allows the following clock sources to be selected:

- F_{OSC} (system clock)
- HFINTOSC

When the HFINTOSC is selected, the HFINTOSC will be kept running during Sleep. Therefore, CWG modes requiring dead band can operate in Sleep, provided that the CWG data input is also active during Sleep. The clock sources are selected using the CS bit. The system clock F_{OSC}, is disabled in Sleep and thus dead-band control cannot be used.

31.5 Selectable Input Sources

The CWG generates the output waveforms from the input sources which are selected with the ISM bits as shown below.

Table 31-1. CWG Data Input Sources

ISM	Data Source
1111	CCP5_out
1110	CLC4_out
1101	CLC3_out
1100	CLC2_out
1011	CLC1_out
1010	DSM1_out
1001	C2_out
1000	C1_out
0111	NCO1_out
0110	PWM7_out
0101	PWM6_out
0100	CCP4_out
0011	CCP3_out
0010	CCP2_out

33.8 Register Definitions: Configurable Logic Cell

Long bit name prefixes for the CLC peripherals are shown in the table below. Refer to the *"Long Bit Names Section"* for more information.

Table 33-2. CLC Bit Name Prefixes

Peripheral	Bit Name Prefix
CLC1	LC1
CLC2	LC2
CLC3	LC3
CLC4	LC4

Related Links

1.4.2.2 Long Bit Names

35.5.3.3 7-bit Transmission with Address Hold Enabled

Setting the AHEN bit enables additional clock stretching and interrupt generation after the eighth falling edge of a received matching address. Once a matching address has been clocked in, CKP is cleared and the SSPxIF interrupt is set.

Figure 35-19 displays a standard waveform of a 7-bit address slave transmission with AHEN enabled.

1. Bus starts Idle.
2. Master sends Start condition; the S bit is set; SSPxIF is set if interrupt on Start detect is enabled.
3. Master sends matching address with R/W bit set. After the eighth falling edge of the SCL line the CKP bit is cleared and SSPxIF interrupt is generated.
4. Slave software clears SSPxIF.
5. Slave software reads the ACKTIM, R/W and D/A bits to determine the source of the interrupt.
6. Slave reads the address value from the SSPxBUF register clearing the BF bit.
7. Slave software decides from this information if it wishes to $\overline{ACK}$ or not $\overline{ACK}$ and sets the ACKDT bit accordingly.
8. Slave sets the CKP bit releasing SCL.
9. Master clocks in the $\overline{ACK}$ value from the slave.
10. Slave hardware automatically clears the CKP bit and sets SSPxIF after the $\overline{ACK}$ if the R/W bit is set.
11. Slave software clears SSPxIF.
12. Slave loads value to transmit to the master into SSPxBUF setting the BF bit.

Important: SSPxBUF cannot be loaded until after the $\overline{ACK}$.

13. Slave sets the CKP bit releasing the clock.
14. Master clocks out the data from the slave and sends an $\overline{ACK}$ value on the ninth SCL pulse.
15. Slave hardware copies the $\overline{ACK}$ value into the ACKSTAT bit.
16. Steps 10-15 are repeated for each byte transmitted to the master from the slave.
17. If the master sends a not $\overline{ACK}$ the slave releases the bus allowing the master to send a Stop and end the communication.

Important: Master must send a not $\overline{ACK}$ on the last byte to ensure that the slave releases the SCL line to receive a Stop.

36.1.2.6 Receiving 9-Bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCxSTA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCxSTA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCxREG.

36.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCxSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RCxIF interrupt bit. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.

36.1.2.8 Asynchronous Reception Setup

1. Initialize the SPxBRGH:SPxBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see the 36.2 EUSART Baud Rate Generator (BRG) section).
2. Set the RXxPPS register to select the RXx/DTx input pin.
3. Clear the ANSEL bit for the RXx pin (if applicable).
4. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
5. If interrupts are desired, set the RCxIE bit of the PIEx register and the GIE and PEIE bits of the INTCON register.
6. If 9-bit reception is desired, set the RX9 bit.
7. Enable reception by setting the CREN bit.
8. The RCxIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCxIE interrupt enable bit was also set.
9. Read the RCxSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
10. Get the received eight Least Significant data bits from the receive buffer by reading the RCxREG register.
11. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

36.1.2.9 9-Bit Address Detection Mode Setup

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable follow these steps:

1. Initialize the SPxBRGH:SPxBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see the 36.2 EUSART Baud Rate Generator (BRG) section).
2. Set the RXxPPS register to select the RXx input pin.
3. Clear the ANSEL bit for the RXx pin (if applicable).
4. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.

Table 36-1. Baud Rate Formulas

Configuration Bits			BRG/EUSART Mode	Baud Rate Formula
SYNC	BRG16	BRGH		
0	0	0	8-bit/Asynchronous	$F_{OSC}/[64\ (n+1)]$
0	0	1	8-bit/Asynchronous	$F_{OSC}/[16\ (n+1)]$
0	1	0	16-bit/Asynchronous	
0	1	1	16-bit/Asynchronous	$F_{OSC}/[4\ (n+1)]$
1	0	x	8-bit/Synchronous	
1	1	x	16-bit/Synchronous	

Note: x = Don't care, n = value of SPxBRGH:SPxBRGL register pair.

Table 36-2. Sample Baud Rates for Asynchronous Modes

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 0											
	F_{OSC} = 32.000 MHz			F_{OSC} = 20.000 MHz			F_{OSC} = 18.432 MHz			F_{OSC} = 11.0592 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	—	—	—	—	—	—	—	—	—	—	—	—
1200	—	—	—	1221	1.73	255	1200	0.00	239	1200	0.00	143
2400	2404	0.16	207	2404	0.16	129	2400	0.00	119	2400	0.00	71
9600	9615	0.16	51	9470	-1.36	32	9600	0.00	29	9600	0.00	17
10417	10417	0.00	47	10417	0.00	29	10286	-1.26	27	10165	-2.42	16
19.2k	19.23k	0.16	25	19.53k	1.73	15	19.20k	0.00	14	19.20k	0.00	8
57.6k	55.55k	-3.55	3	—	—	—	57.60k	0.00	7	57.60k	0.00	2
115.2k	—	—	—	—	—	—	—	—	—	—	—	—

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 0											
	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	—	—	—	300	0.16	207	300	0.00	191	300	0.16	51
1200	1202	0.16	103	1202	0.16	51	1200	0.00	47	1202	0.16	12
2400	2404	0.16	51	2404	0.16	25	2400	0.00	23	—	—	—
9600	9615	0.16	12	—	—	—	9600	0.00	5	—	—	—

37.3.4 SMTxCLK

Name: SMTxCLK
Address: 0x49B,0x51B

SMT Clock Selection Register

Bit	7	6	5	4	3	2	1	0
						CSEL[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:0 – CSEL[2:0] SMT Clock Selection bits

Table 37-5. SMT Clock Source Selection

CSEL<2:0>	Clock Source
111	CLKREF output
110	SOSC
101	MFINTOSC (31.25kHz)
100	MFINTOSC (500kHz)
011	LFINTOSC
010	HFINTOSC
001	F_{OSC}
000	$F_{OSC}/4$

Address	Name	Bit Pos.								
0x1A09	WREG	7:0	WREG[7:0]							
0x1A0A	PCLATH	7:0		PCLATH[6:0]						
0x1A0B	INTCON	7:0	GIE	PEIE						INTEDG
0x1A0C ... 0x1A7F	Reserved									
0x1A80	INDF0	7:0	INDF0[7:0]							
0x1A81	INDF1	7:0	INDF1[7:0]							
0x1A82	PCL	7:0	PCL[7:0]							
0x1A83	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1A84	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1A86	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1A88	BSR	7:0			BSR[5:0]					
0x1A89	WREG	7:0	WREG[7:0]							
0x1A8A	PCLATH	7:0		PCLATH[6:0]						
0x1A8B	INTCON	7:0	GIE	PEIE						INTEDG
0x1A8C ... 0x1AFF	Reserved									
0x1B00	INDF0	7:0	INDF0[7:0]							
0x1B01	INDF1	7:0	INDF1[7:0]							
0x1B02	PCL	7:0	PCL[7:0]							
0x1B03	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1B04	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1B06	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1B08	BSR	7:0			BSR[5:0]					
0x1B09	WREG	7:0	WREG[7:0]							
0x1B0A	PCLATH	7:0		PCLATH[6:0]						
0x1B0B	INTCON	7:0	GIE	PEIE						INTEDG
0x1B0C ... 0x1B7F	Reserved									
0x1B80	INDF0	7:0	INDF0[7:0]							
0x1B81	INDF1	7:0	INDF1[7:0]							
0x1B82	PCL	7:0	PCL[7:0]							
0x1B83	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1B84	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1B86	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1B88	BSR	7:0			BSR[5:0]					
0x1B89	WREG	7:0	WREG[7:0]							

$T_{A\_MIN} \le T_A \le T_{A\_MAX}$

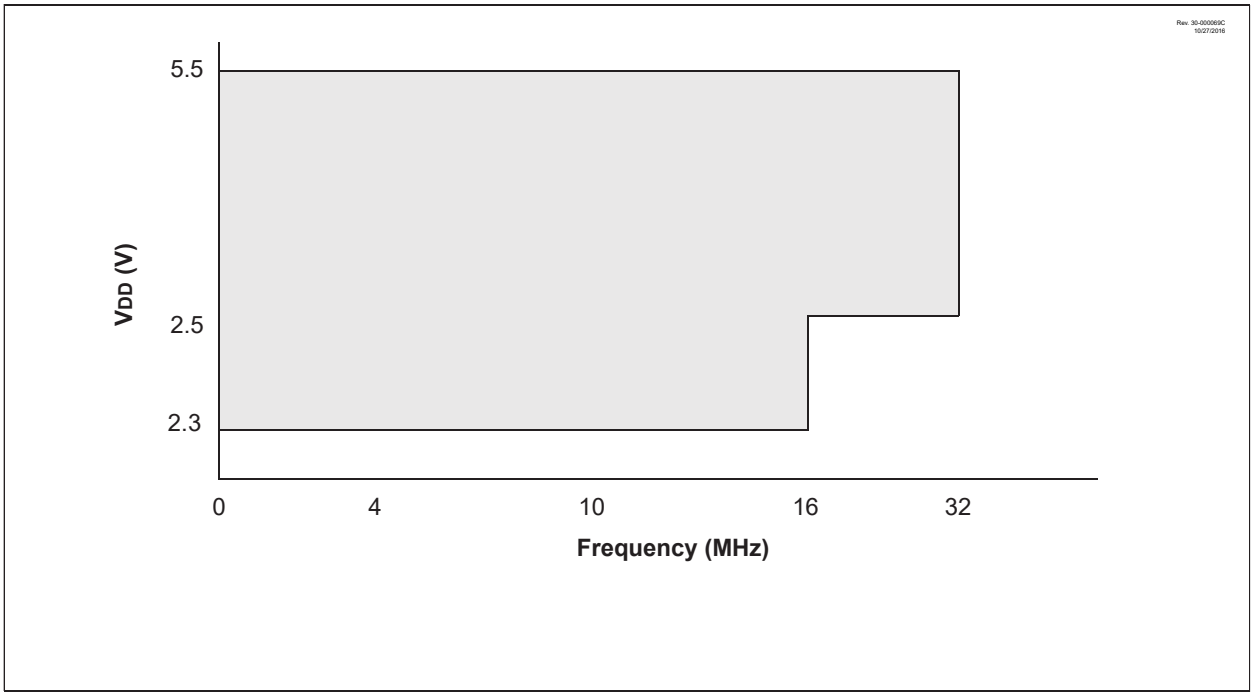
Operating Temperature:

Parameter		Ratings
V_{DD} — Operating Supply Voltage(1)		
PIC16LF18455/56	V_{DDMIN} ($F_{OSC} \le$ 16 MHz)	+1.8V
	V_{DDMIN} ($F_{OSC} \le$ 32 MHz)	+2.5V
	V_{DDMAX}	+3.6V
PIC16F18455/56	V_{DDMIN} ($F_{OSC} \le$ 16 MHz)	+2.3V
	V_{DDMIN} ($F_{OSC} \le$ 32 MHz)	+2.5V
	V_{DDMAX}	+5.5V
T_A — Operating Ambient Temperature Range		
Industrial Temperature	T_{A_MIN}	-40°C
	T_{A_MAX}	+85°C
Extended Temperature	T_{A_MIN}	-40°C
	T_{A_MAX}	+125°C

Note:

1. See Parameter *D002*, DC Characteristics: Supply Voltage.

Figure 42-1. Voltage Frequency Graph, -40°C ≤ T_A≤ +125°C, for PIC16F18455/56 only

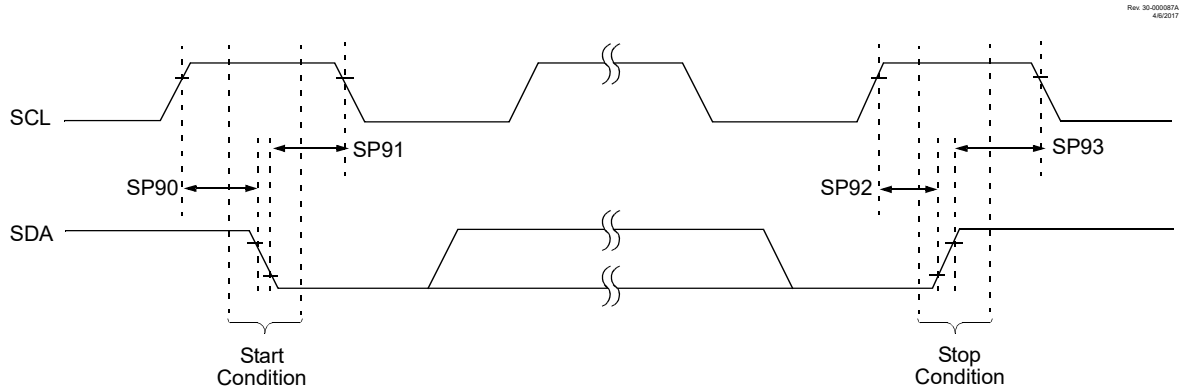


Note:

1. The shaded region indicates the permissible combinations of voltage and frequency.
2. Refer to 42.4.1 External Clock/Oscillator Timing Requirements for each Oscillator mode's supported frequencies.

Standard Operating Conditions (unless otherwise stated)								
Param. No.	Sym.	Characteristic		Min.	Typ. †	Max.	Units	Conditions
			400 kHz mode	600	—	—		
* - These parameters are characterized but not tested.								

Figure 42-21. I²C Bus Start/Stop Bits Timing



Note: Refer to Figure 42-4 for load conditions.

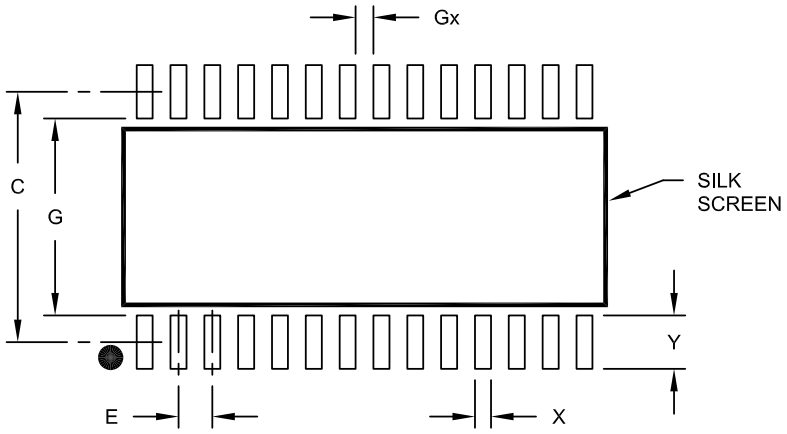
42.4.20 I²C Bus Data Requirements

Table 42-26.

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Sym.	Characteristic		Min.	Max.	Units	Conditions
SP100*	T_{HIGH}	Clock high time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			SSP module	$1.5T_{CY}$	—		
SP101*	T_{LOW}	Clock low time	100 kHz mode	4.7	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	Device must operate at a minimum of 10 MHz

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A