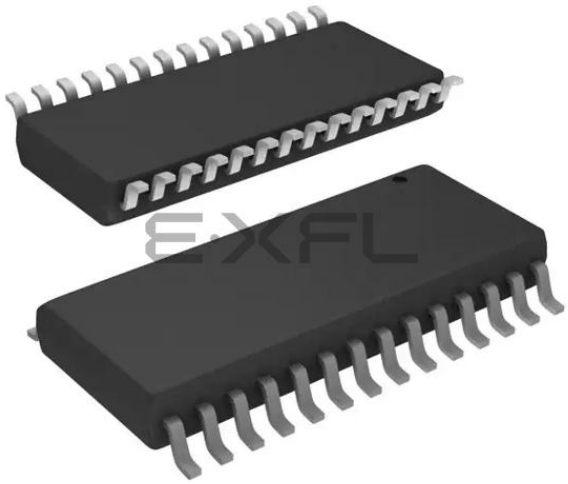

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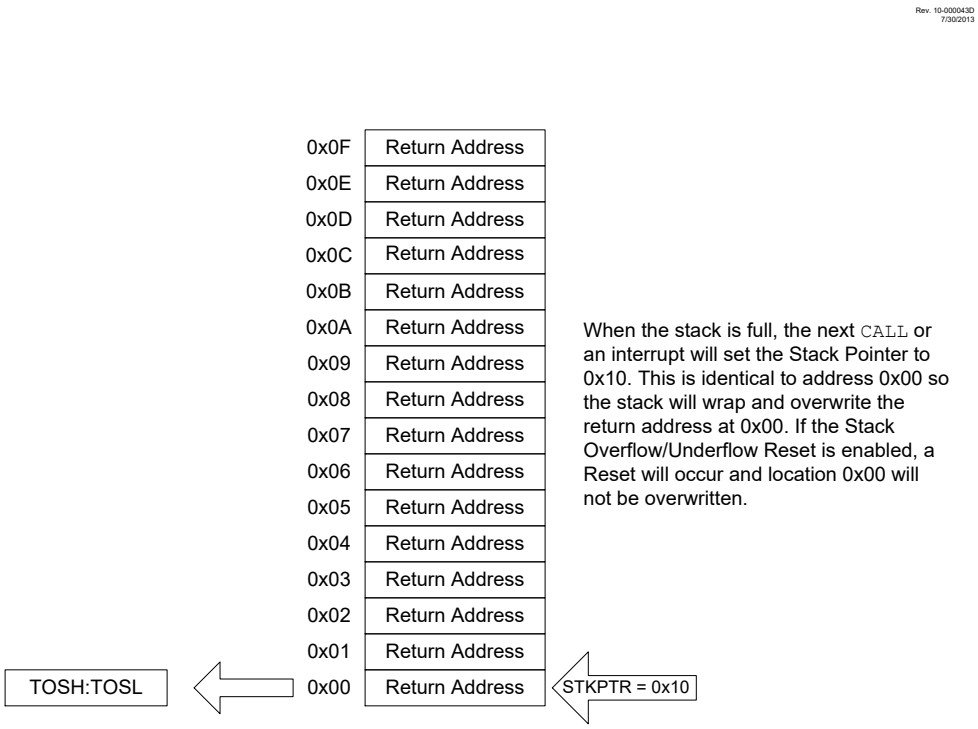
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18456-e-so

Figure 7-7. Accessing the Stack Example 4



Related Links

7.8.11 TOS

7.5.2 Overflow/Underflow Reset

If the STVREN bit in Configuration Word 2 is programmed to '1', the device will be Reset if the stack is PUSHed beyond the sixteenth level or POPed beyond the first level, setting the appropriate bits (STKOVF or STKUNF, respectively) in the PCON register.

Related Links

4.7.2 CONFIG2

7.6 Indirect Addressing

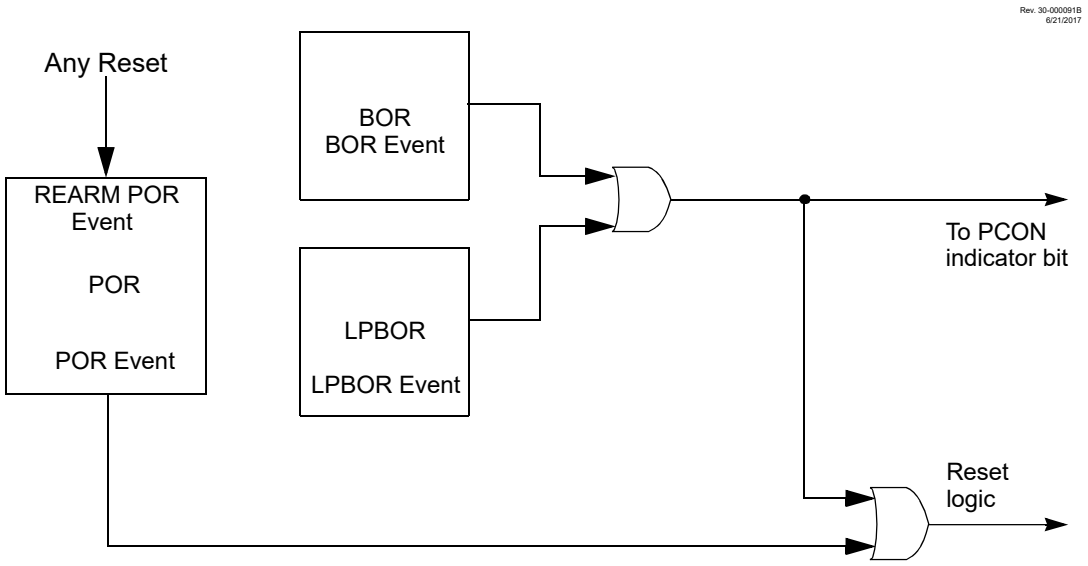
The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the File Select Registers (FSR). If the FSRn address specifies one of the two INDFn registers, the read will return '0' and the write will not occur (though Status bits may be affected). The FSRn register value is created by the pair FSRnH and FSRnL.

The FSR registers form a 16-bit address that allows an addressing space with 65536 locations. These locations are divided into three memory regions:

- Traditional/Banked Data Memory
- Linear Data Memory
- Program Flash Memory

The LPBOR is used to monitor the external V_{DD} pin. When too low of a voltage is detected, the device is held in Reset.

Figure 8-3. LPBOR, BOR, POR Relationship



8.3.1 Enabling LPBOR

The LPBOR is controlled by the $\overline{\text{LPBOREN}}$ bit of Configuration Word 2. When the device is erased, the LPBOR module defaults to disabled.

Related Links

4.7.2 CONFIG2

8.3.2 LPBOR Module Output

The output of the LPBOR module is a signal indicating whether or not a Reset is to be asserted. This signal is OR'd together with the Reset signal of the BOR module to provide the generic $\overline{\text{BOR}}$ signal, which goes to the PCON0 register and to the power control block.

8.4 $\overline{\text{MCLR}}$ Reset

The $\overline{\text{MCLR}}$ is an optional external input that can reset the device. The $\overline{\text{MCLR}}$ function is controlled by the MCLRE bit of Configuration Words and the LVP bit of Configuration Words (see table below). The $\overline{\text{RMCLR}}$ bit in the PCON0 register will be set to '0' if a $\overline{\text{MCLR}}$ has occurred.

Table 8-2. $\overline{\text{MCLR}}$ Configuration

MCLRE	LVP	$\overline{\text{MCLR}}$
x	1	Enabled
1	0	Enabled
0	0	Disabled

9.6.3 OSCCON3

Name: OSCCON3
Address: 0x88F

Oscillator Control Register 3

Bit	7	6	5	4	3	2	1	0
	CSWHOLD	SOSCPWR		ORDY	NOSCR			
Access	R/W/HC	R/W		RO	RO			
Reset	0	0		0	0			

Bit 7 – CSWHOLD Clock Switch Hold bit

Value	Description
1	Clock switch will hold (with interrupt) when the oscillator selected by NOSC is ready
0	Clock switch may proceed when the oscillator selected by NOSC is ready; when NOSCR becomes '1', the switch will occur

Bit 6 – SOSCPWR Secondary Oscillator Power Mode Select bit

Value	Description
1	Secondary oscillator operating in High-Power mode
0	Secondary oscillator operating in Low-Power mode

Bit 4 – ORDY Oscillator Ready bit (read-only)

Value	Description
1	OSCCON1 = OSCCON2; the current system clock is the clock specified by NOSC
0	A clock switch is in progress

Bit 3 – NOSCR New Oscillator is Ready bit (read-only)(1)

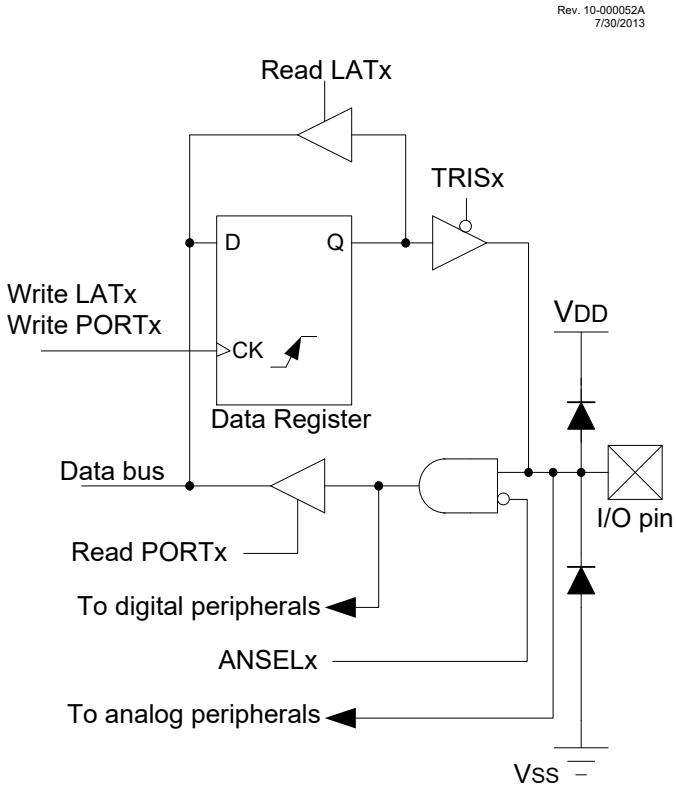
Value	Description
1	A clock switch is in progress and the oscillator selected by NOSC indicates a ready condition
0	A clock switch is not in progress, or the NOSC-selected oscillator is not yet ready

Note:

1. If CSWHOLD = 0, the user may not see this bit set because the bit is set for less than one instruction cycle.

Disabling the input buffer prevents analog signal levels on the pin between a logic high and low from causing excessive current in the logic input circuitry. A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in the following figure:

Figure 14-1. Generic I/O Port Operation



14.3 I/O Priorities

Each pin defaults to the PORT data latch after Reset. Other functions are selected with the peripheral pin select logic. See *"Peripheral Pin Select (PPS) Module"* for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELx register. Digital output functions may continue to control the pin when it is in Analog mode.

Analog outputs, when enabled, take priority over digital outputs and force the digital output driver into a high-impedance state.

The pin function priorities are as follows:

1. Configuration bits
2. Analog outputs (disable the input buffers)
3. Analog inputs
4. Port inputs and outputs from PPS

Related Links

15. (PPS) Peripheral Pin Select Module

14.7.18 ODCONA

Name: ODCONA
Address: 0x1F3A

Open-Drain Control Register

Bit	7	6	5	4	3	2	1	0
	ODCA7	ODCA6	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 – ODCAn Open-Drain Configuration on Pins Rx<7:0>

Value	Description
1	Output drives only low-going signals (sink current only)
0	Output drives both high-going and low-going signals (source and sink current)

14.7.23 SLRCONC

Name: SLRCONC
Address: 0x1F51

Slew Rate Control Register

Bit	7	6	5	4	3	2	1	0
	SLRC7	SLRC6	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 0, 1, 2, 3, 4, 5, 6, 7 – SLRCn Slew Rate Control on Pins Rx<7:0>, respectively

Value	Description
1	Port pin slew rate is limited
0	Port pin slews at maximum rate

17.6.1 IOCAF

Name: IOCAF
Address: 0x1F3F

PORTA Interrupt-on-Change Flag Register Example

Bit	7	6	5	4	3	2	1	0
	IOCAF7	IOCAF6	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0
Access	R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 – IOCAFn Interrupt-on-Change Flag bits

Value	Condition	Description
1	IOCAP[n]=1	A positive edge was detected on the RA[n] pin
1	IOCAN[n]=1	A negative edge was detected on the RA[n] pin
0	IOCAP[n]=x and IOCAN[n]=x	No change was detected, or the user cleared the detected change

17.6.11 IOCCP

Name: IOCCP
Address: 0x1F53

Interrupt-on-Change Positive Edge Register

Bit	7	6	5	4	3	2	1	0
	IOCCP7	IOCCP6	IOCCP5	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 – IOCCPn Interrupt-on-Change Positive Edge Enable bits

Value	Description
1	Interrupt-on-Change enabled on the IOCC pin for a positive-going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0	Interrupt-on-Change disabled for the associated pin.

18. (FVR) Fixed Voltage Reference

The Fixed Voltage Reference (FVR) is a stable voltage reference, independent of V_{DD}, with the following selectable output levels:

- 1.024V
- 2.048V
- 4.096V

The output of the FVR can be configured to supply a reference voltage to the following:

- ADC input channel
- ADC positive reference
- Comparator input
- Digital-to-Analog Converter (DAC)

The FVR can be enabled by setting the FVREN bit of the FVRCON register.

Important: Fixed Voltage Reference output cannot exceed V_{DD}.

Related Links

18.4.1 FVRCON

18.1 Independent Gain Amplifiers

The output of the FVR, which is connected to the ADC, Comparators, and DAC, is routed through two independent programmable gain amplifiers. Each amplifier can be programmed for a gain of 1x, 2x or 4x, to produce the three possible voltage levels.

The ADFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the ADC module. Reference the ADC chapter for additional information.

The CDAFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the DAC and comparator module.

Related Links

20. (ADC2) Analog-to-Digital Converter with Computation Module

23. (CMP) Comparator Module

21. (DAC) 5-Bit Digital-to-Analog Converter Module

18.2 FVR Stabilization Period

When the Fixed Voltage Reference module is enabled, it requires time for the reference and amplifier circuits to stabilize. Once the circuits stabilize and are ready for use, the FVRRDY bit of the FVRCON register will be set.

FVRRDY is an indicator of the reference being ready.

23.14 Register Summary - Comparator

Address	Name	Bit Pos.								
0x098F	CMOUT	7:0							MC2OUT	MC1OUT
0x0990	CM1CON0	7:0	EN	OUT		POL			HYS	SYNC
0x0991	CM1CON1	7:0							INTP	INTN
0x0992	CM1NCH	7:0						NCH[2:0]		
0x0993	CM1PCH	7:0						PCH[2:0]		
0x0994	CM2CON0	7:0	EN	OUT		POL			HYS	SYNC
0x0995	CM2CON1	7:0							INTP	INTN
0x0996	CM2NCH	7:0						NCH[2:0]		
0x0997	CM2PCH	7:0						PCH[2:0]		

23.15 Register Definitions: Comparator Control

Long bit name prefixes for the comparator peripherals are shown in the table below. Refer to the *"Long Bit Names Section"* for more information.

Table 23-2. Comparator Bit Name Prefixes

Peripheral	Bit Name Prefix
C1	C1
C2	C2

Related Links

1.4.2.2 Long Bit Names

- Accurate long term time measurement
- Dimmer phase delayed drive
- Low EMI cycle switching

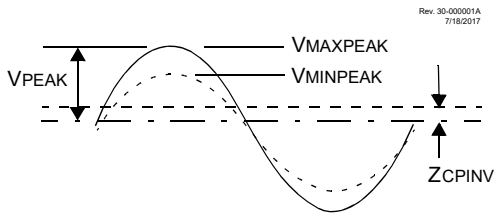
24.1 External Resistor Selection

The ZCD module requires a current-limiting resistor in series with the external voltage source. The impedance and rating of this resistor depends on the external source peak voltage. Select a resistor value that will drop all of the peak voltage when the current through the resistor is nominally 300 µA. Make sure that the ZCD I/O pin internal weak pull-up is disabled so it does not interfere with the current source and sink.

Equation 24-1. External Resistor

$$R_{SERIES} = \frac{V_{PEAK}}{3 \times 10^{-4}}$$

Figure 24-2. External Voltage Source



24.2 ZCD Logic Output

The ZCD module includes a Status bit, which can be read to determine whether the current source or sink is active. The OUT bit is set when the current sink is active, and cleared when the current source is active. The OUT bit is affected by the polarity bit.

The OUT signal can also be used as input to other modules. This is controlled by the registers of the corresponding module. OUT can be used as follows:

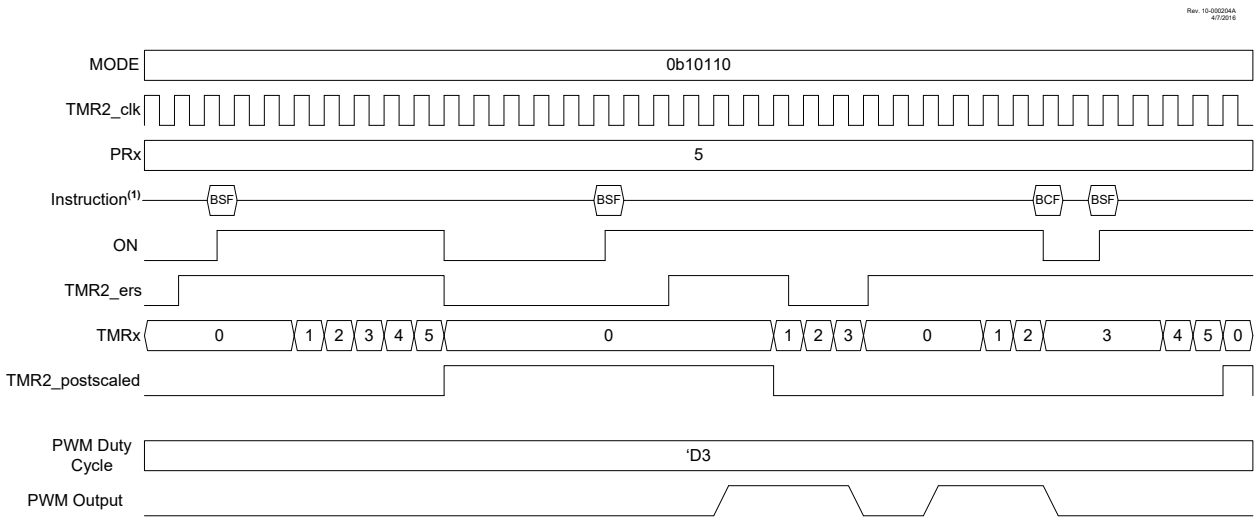
- Gate source for TMR1/3/5
- Clock source for TMR2/4/6
- Reset source for TMR2/4/6

24.3 ZCD Logic Polarity

The POL bit inverts the OUT bit relative to the current source and sink output. When the POL bit is set, a OUT high indicates that the current source is active, and a low output indicates that the current sink is active.

The POL bit affects the ZCD interrupts.

Figure 27-12. Level-Triggered hardware Limit one-Shot Mode Timing Diagram (MODE = 10110)



Note:

1. BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

Related Links

29.4 PWM Overview

30. (PWM) Pulse-Width Modulation

27.7 Timer2 Operation During Sleep

When PSYNC = 1, Timer2 cannot be operated while the processor is in Sleep mode. The contents of the T2TMR and T2PR registers will remain unchanged while processor is in Sleep mode.

When PSYNC = 0, Timer2 will operate in Sleep as long as the clock source selected is also still running. If any internal oscillator is selected as the clock source, it will stay active during Sleep mode.

30.11 Register Summary - Registers Associated with PWM

Address	Name	Bit Pos.									
0x038C	PWM6DC	7:0	DCL[1:0]								
		15:8	DCH[7:0]								
0x038E	PWM6CON	7:0	EN		OUT	POL					
0x038F	Reserved										
0x0390	PWM7DC	7:0	DCL[1:0]								
		15:8	DCH[7:0]								
0x0392	PWM7CON	7:0	EN		OUT	POL					

30.12 Register Definitions: PWM Control

Long bit name prefixes for the PWM peripherals are shown in the table below. Refer to the *"Long Bit Names Section"* for more information.

Table 30-3. PWM Bit Name Prefixes

Peripheral	Bit Name Prefix
PWM6	PWM6
PWM7	PWM7

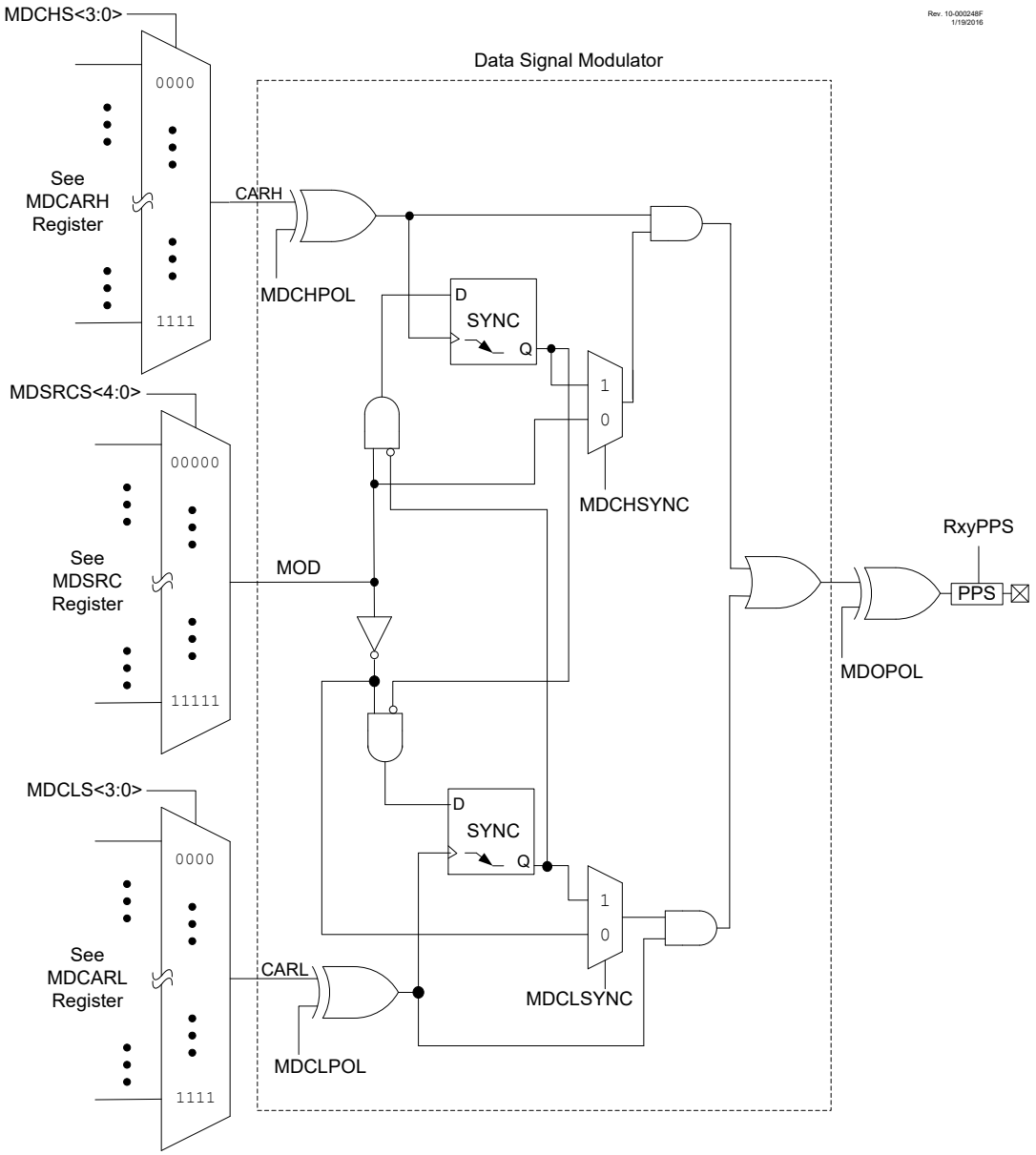
Related Links

1.4.2.2 Long Bit Names

11. Select the clock source with the CS bits.
12. Set the EN bit to enable the module.
13. Clear the TRIS bits that correspond to the CWG outputs to set them as outputs.

If auto-restart is to be used, set the REN bit and the SHUTDOWN bit will be cleared automatically. Otherwise, clear the SHUTDOWN bit in software to start the CWG.

Figure 32-1. Simplified Block Diagram of the Data Signal Modulator



32.1 DSM Operation

The DSM module can be enabled by setting the EN bit in the MDCON0 register. Clearing the EN bit, disables the output of the module but retain the carrier and source signal selections. The module will resume operation when the EN bit is set again. The output of the DSM module can be rerouted to several pins using the RxyPPS register. When the EN bit is cleared the output pin is held low.

32.2 Modulator Signal Sources

The modulator signal can be supplied from the following sources selected with the SRCS bits:

34.6.2 CLKRCLK

Name: CLKRCLK
Address: 0x896

Clock Reference Clock Selection MUX

Bit	7	6	5	4	3	2	1	0
					CLK[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – CLK[3:0] CLKR Clock Selection bits
See the Clock Sources table.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the Global Interrupt Enable (GIE) bit is also set then the Interrupt Service Routine at address 0004h will be called.

Address	Name	Bit Pos.								
0x059E	T0CON0	7:0	T0EN		T0OUT	T016BIT	T0OUTPS[3:0]			
0x059F	T0CON1	7:0	T0CS[2:0]			T0ASYNC	T0CKPS[3:0]			
0x05A0 ... 0x05FF	Reserved									
0x0600	INDF0	7:0	INDF0[7:0]							
0x0601	INDF1	7:0	INDF1[7:0]							
0x0602	PCL	7:0	PCL[7:0]							
0x0603	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x0604	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0606	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0608	BSR	7:0			BSR[5:0]					
0x0609	WREG	7:0	WREG[7:0]							
0x060A	PCLATH	7:0		PCLATH[6:0]						
0x060B	INTCON	7:0	GIE	PEIE						INTEDG
0x060C	CWG1CLK	7:0								CS
0x060D	CWG1ISM	7:0					ISM[3:0]			
0x060E	CWG1DBR	7:0			DBR[5:0]					
0x060F	CWG1DBF	7:0			DBF[5:0]					
0x0610	CWG1CON0	7:0	EN	LD				MODE[2:0]		
0x0611	CWG1CON1	7:0			IN		POLD	POLC	POLB	POLA
0x0612	CWG1AS0	7:0	SHUTDOWN	REN	LSBD[1:0]		LSAC[1:0]			
0x0613	CWG1AS1	7:0			AS5E	AS4E	AS3E	AS2E	AS1E	AS0E
0x0614	CWG1STR	7:0	OVRD	OVRC	OVRB	OVRA	STRD	STRC	STRB	STRA
0x0615	Reserved									
0x0616	CWG2CLK	7:0								CS
0x0617	CWG2ISM	7:0					ISM[3:0]			
0x0618	CWG2DBR	7:0			DBR[5:0]					
0x0619	CWG2DBF	7:0			DBF[5:0]					
0x061A	CWG2CON0	7:0	EN	LD				MODE[2:0]		
0x061B	CWG2CON1	7:0			IN		POLD	POLC	POLB	POLA
0x061C	CWG2AS0	7:0	SHUTDOWN	REN	LSBD[1:0]		LSAC[1:0]			
0x061D	CWG2AS1	7:0			AS5E	AS4E	AS3E	AS2E	AS1E	AS0E
0x061E	CWG2STR	7:0	OVRD	OVRC	OVRB	OVRA	STRD	STRC	STRB	STRA
0x061F ... 0x067F	Reserved									
0x0680	INDF0	7:0	INDF0[7:0]							
0x0681	INDF1	7:0	INDF1[7:0]							
0x0682	PCL	7:0	PCL[7:0]							
0x0683	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x0684	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0686	FSR1	7:0	FSRL[7:0]							

Note:

1. If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.
2. If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.
3. Details on `MOVIW` and `MOVWI` instruction descriptions are available in the next section.

40.2.1 Standard Instruction Set

ADDFSR	Add Literal to FSRn
Syntax:	[*label*] ADDFSR FSRn, k
Operands:	-32 ≤ k ≤ 31; n ∈ [0, 1]
Operation:	FSR(n) + k → FSR(n)
Status Affected:	None
Description:	The signed 6-bit literal ‘k’ is added to the contents of the FSRnH:FSRnL register pair. FSRn is limited to the range 0000h-FFFFh. Moving beyond these bounds will cause the FSR to wrap-around.

ADDLW	ADD literal to W
Syntax:	[*label*] ADDLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) + k → (W)
Status Affected:	C, DC, Z
Description:	The contents of W are added to the 8-bit literal ‘k’ and the result is placed in W.

ADDWF	ADD W to f
Syntax:	[*label*] ADDWF f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) + (f) → dest
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register ‘f’. If ‘d’ is ‘`0`’, the result is stored in the W register. If ‘d’ is ‘`1`’, the result is stored back in register ‘f’.