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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18456-e-ss

Pin Allocation Tables

1 28-Pin Allocation Table

I/O	28-pin SPDIP/SOIC/SSOP	28-pin VQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupts	Pull-up	Basic
RA0	2	27	ANA0	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	—	CLCIN0(1)	—	IOCA0	Y	—
RA1	3	28	ANA1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—	CLCIN1(1)	—	IOCA1	Y	—
RA2	4	1	ANA2	ADCVREF-	C1IN0+ C2IN0+	—	DAC1VREF- DAC1OUT1	—	—	—	—	—	—	—	—	—	—	IOCA2	Y	—
RA3	5	2	ANA3	ADCVREF+	C1IN1+	—	DAC1VREF+	MDCARL(1)	—	—	—	—	—	—	—	—	—	IOCA3	Y	—
RA4	6	3	ANA4	—	—	—	—	MDCARH(1)	T0CKI(1)	CCP5IN(1)	—	—	—	—	—	—	—	IOCA4	Y	—
RA5	7	4	ANA5	—	—	—	—	MDSRC(1)	—	—	—	—	$\overline{SS1}$(1)	—	—	—	—	IOCA5	Y	—
RA6	10	7	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA6	Y	OSC2 CLKOUT
RA7	9	6	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA7	Y	OSC1 CLKIN
RB0	21	18	ANB0	—	C2IN1+	—	—	—	—	CCP4IN(1)	—	CWG1IN(1)	—	ZCD1	—	—	—	IOCB0	Y	INT(1)
RB1	22	19	ANB1	—	C1IN3- C2IN3-	—	—	—	—	—	—	CWG2IN(1)	SCK2(1) SCL2(1,3)	—	—	—	—	IOCB1	Y	—
RB2	23	20	ANB2	—	—	—	—	—	—	—	—	CWG3IN(1)	SDI2(1) SDA2(1,3)$\overline{SS2}$(1)	—	—	—	—	IOCB2	Y	—
RB3	24	21	ANB3	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	—	—	IOCB3	Y	—
RB4	25	22	ANB4 ADACT(1)	—	—	—	—	—	T5G(1) SMT2WIN(1)	—	—	—	—	—	—	—	—	—	IOCB4	Y	—
RB5	26	23	ANB5	—	—	—	—	—	T1G(1) SMT2SIG(1)	CCP3IN(1)	—	—	—	—	—	—	—	IOCB5	Y	—
RB6	27	24	ANB6	—	—	—	—	—	—	—	—	—	—	—	CK2(1,3)	CLCIN2(1)	—	IOCB6	Y	ICSPCLK ICDCLK
RB7	28	25	ANB7	—	—	—	DAC1OUT2	—	T6IN(1)	—	—	—	—	—	RX2(1) DT2(1,3)	—	—	IOCB7	Y	ICSPDAT ICDDAT
RC0	11	8	ANC0	—	—	—	—	—	T1CKI(1) T3CKI(1) T3G(1)	—	—	—	—	—	—	—	—	IOCC0	Y	SOSCO

2. Guidelines for Getting Started with PIC16(L)F18455/56 Microcontrollers

2.1 Basic Connection Requirements

Getting started with the PIC16(L)F18455/56 family of 8-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All V_{DD} and V_{SS} pins (see 2.2 Power Supply Pins)
- $\overline{MCLR}$ pin (see 2.3 Master Clear (MCLR) Pin)

These pins must also be connected if they are being used in the end application:

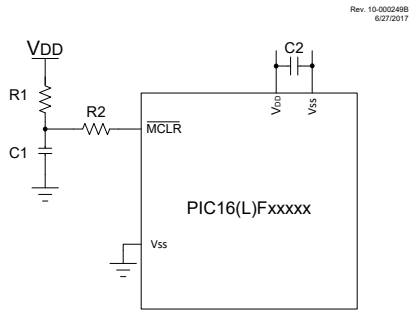
- PGC/PGD pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see 2.4 In-Circuit Serial Programming™ ICSP™ Pins)
- OSCI and OSCO pins when an external oscillator source is used (see 2.5 External Oscillator Pins)

Additionally, the following may be required:

- $V_{REF}+/V_{REF}-$ pins are used when external voltage reference for analog modules is implemented

The minimum mandatory connections are shown in the figure below.

Figure 2-1. Recommended Minimum Connections



Key (all values are recommendations):
C1: 10 nF, 16V ceramic
C2: 0.1 uF, 16V ceramic
R1: 10 kΩ
R2: 100Ω to 470Ω

2.2 Power Supply Pins

2.2.1 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins (V_{DD} and V_{SS}) is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: A 0.1 µF (100 nF), 10-25V capacitor is recommended. The capacitor should be a low-ESR device, with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.

9. Oscillator Module (with Fail-Safe Clock Monitor)

9.1 Overview

The oscillator module has multiple clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. The following figure illustrates a block diagram of the oscillator module.

Clock sources can be supplied from external oscillators, quartz-crystal resonators and ceramic resonators. In addition, the system clock source can be supplied from one of two internal oscillators and PLL circuits, with a choice of speeds selectable via software. Additional clock features include:

- Selectable system clock source between external or internal sources via software.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, ECH, ECM, ECL) and switch automatically to the internal oscillator.
- Oscillator Start-up Timer (OST) ensures stability of crystal oscillator sources.

The RSTOSC bits of Configuration Word 1 determine the type of oscillator that will be used when the device runs after Reset, including when it is first powered up.

The internal clock modes, LFINTOSC, HFINTOSC (set at 1 MHz), or HFINTOSC (set at 32 MHz) can be set through the RSTOSC bits.

If an external clock source is selected, the FEXTOSC bits of Configuration Word 1 must be used in conjunction with the RSTOSC bits to select the External Clock mode.

The external oscillator module can be configured in one of the following clock modes, by setting the FEXTOSC bits of Configuration Word 1:

1. ECL – External Clock Low-Power mode
   (≤ 500 kHz)
2. ECM – External Clock Medium-Power mode
   (≤ 8 MHz)
3. ECH – External Clock High-Power mode
   (≤ 32 MHz)
4. LP – 32 kHz Low-Power Crystal mode.
5. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode (between 100 kHz and 4 MHz)
6. HS – High Gain Crystal or Ceramic Resonator mode (above 4 MHz)

The ECH, ECM, and ECL Clock modes rely on an external logic level signal as the device clock source. The LP, XT, and HS Clock modes require an external crystal or resonator to be connected to the device. Each mode is optimized for a different frequency range. The internal oscillator block produces low and high-frequency clock sources, designated LFINTOSC and HFINTOSC. Multiple device clock frequencies may be derived from these clock sources.

10.7.10 PIE8

Name: PIE8
Address: 0x71E

Peripheral Interrupt Enable Register 8

Bit	7	6	5	4	3	2	1	0
			SMT2PWAIE	SMT2PRAIE	SMT2IE	SMT1PWAIE	SMT1PRAIE	SMT1IE
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit 5 – SMT2PWAIE SMT2 Pulse-width Acquisition Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 4 – SMT2PRAIE SMT2 Period Acquisition Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 3 – SMT2IE SMT2 Counter Overflow Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 2 – SMT1PWAIE SMT1 Pulse-width Acquisition Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 1 – SMT1PRAIE SMT1 Period Acquisition Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 0 – SMT1IE SMT1 Counter Overflow Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by registers PIE1-PIE8.

10.7.11 PIR0

Name: PIR0
Address: 0x70C

Peripheral Interrupt Request (Flag) Register 0

Bit	7	6	5	4	3	2	1	0
			TMR0IF	IOCIF				INTF
Access			R/W/HS	RO				R/W/HS
Reset			0	0				0

Bit 5 – TMR0IF Timer0 Interrupt Flag bit

Value	Description
1	TMR0 register has overflowed (must be cleared by software)
0	TMR0 register has not overflowed

Bit 4 – IOCIF Interrupt-on-Change Flag bit(2)

Value	Description
1	One or more of the IOCAF-IOCEF register bits are currently set, indicating an enabled edge was detected by the IOC module.
0	None of the IOCAF-IOCEF register bits are currently set

Bit 0 – INTF External Interrupt Flag bit(1)

Value	Description
1	External Interrupt has occurred
0	External Interrupt has not occurred

Note:

1. The External Interrupt INT pin is selected by INTPPS.
2. The IOCIF bit is the logical OR of all the IOCAF-IOCEF flags. Therefore, to clear the IOCIF flag, application firmware must clear all of the lower level IOCAF-IOCEF register bits.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON appropriate interrupt flag bits are clear prior to enabling an interrupt.

Related Links

15.9.1 xxxPPS

13.6.4 NVMCON2

Name: NVMCON2
Address: 0x81F

Nonvolatile Memory Control 2 Register

Bit	7	6	5	4	3	2	1	0
	NVMCON2[7:0]							
Access	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – NVMCON2[7:0] Flash Memory Unlock Pattern bits

Note: To unlock writes, a 55h must be written first followed by an AAh before setting the WR bit of the NVMCON1 register. The value written to this register is used to unlock the writes.

15.8 Register Summary - PPS

Address	Name	Bit Pos.								
0x1E8F	PPSLOCK	7:0								PPSLOCKED
0x1E90	INTPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E91	T0CKIPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E92	T1CKIPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E93	T1GPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E94	T3CKIPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E95	T3GPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E96	T5CKIPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E97	T5GPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E98 ... 0x1E9B	Reserved									
0x1E9C	T2INPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E9D	T4INPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E9E	T6INPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E9F ... 0x1EA0	Reserved									
0x1EA1	CCP1PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EA2	CCP2PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EA3	CCP3PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EA4	CCP4PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EA5	CCP5PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EA6 ... 0x1EA8	Reserved									
0x1EA9	SMT1WINPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EAA	SMT1SIGPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EAB	SMT2WINPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EAC	SMT2SIGPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EAD ... 0x1EB0	Reserved									
0x1EB1	CWG1PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EB2	CWG2PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EB3	CWG3PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EB4 ... 0x1EB7	Reserved									
0x1EB8	MDCARLPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EB9	MDCARHPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBA	MDSRCPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBB	CLCIN0PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBC	CLCIN1PPS	7:0				PORT[1:0]		PIN[2:0]		

17.6.1 IOCAF

Name: IOCAF
Address: 0x1F3F

PORTA Interrupt-on-Change Flag Register Example

Bit	7	6	5	4	3	2	1	0
	IOCAF7	IOCAF6	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0
Access	R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 – IOCAFn Interrupt-on-Change Flag bits

Value	Condition	Description
1	IOCAP[n]=1	A positive edge was detected on the RA[n] pin
1	IOCAN[n]=1	A negative edge was detected on the RA[n] pin
0	IOCAP[n]=x and IOCAN[n]=x	No change was detected, or the user cleared the detected change

17.6.5 IOCAN

Name: IOCAN
Address: 0x1F3E

Interrupt-on-Change Negative Edge Register Example

Bit	7	6	5	4	3	2	1	0
	IOCAN7	IOCAN6	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 – IOCANn Interrupt-on-Change Negative Edge Enable bits

Value	Description
1	Interrupt-on-Change enabled on the IOCA pin for a negative-going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0	Interrupt-on-Change disabled for the associated pin

Note: Where:
ADC_{MEAS} = ADC reading at temperature being estimated

ADC_{DIA} = ADC reading stored in the DIA

FVRA2X = FVR value stored in the DIA for 2x setting

N = Resolution of the ADC

Mv = Temperature Indicator voltage sensitivity (mV/°C)

Note: It is recommended to take the average of ten measurements of ADC_{MEAS} to reduce noise and improve accuracy.

Related Links
42.4.6 Temperature Indicator Requirements

19.4.1 Calibration

19.4.1.1 Higher-Order Calibration

If the application requires more precise temperature measurement, additional calibrations steps will be necessary. For these applications, two-point or three-point calibration is recommended. An Application Note will be released in future that demonstrates higher-order calibration process. An Application Note will be released in future that demonstrates higher-order calibration process.

19.4.2 Temperature Resolution

The resolution of the ADC reading, Ma (°C/count), depends on both the ADC resolution N and the reference voltage used for conversion, as shown in the equation below. It is recommended to use the smallest V_{REF} value, such as the ADC FVR1 Output Voltage for 2x setting (FVRA2X) value from the DIA Table.

Related Links
42.4.11 Fixed Voltage Reference (FVR) Specifications

19.5 ADC Acquisition Time

To ensure accurate temperature measurements, the user must wait a minimum of 25 µs for the ADC value to settle, after the ADC input multiplexer is connected to the temperature indicator output, before the conversion is performed.

20.6.1 Digital Filter/Average

The digital filter/average module consists of an accumulator with data feedback options, and control logic to determine when threshold tests need to be applied. The accumulator is a 16-bit wide register that can be accessed through the ADACCH:ADACCL register pair.

Upon each trigger event (the GO bit set or external event trigger), the ADC conversion result is added to the accumulator. If the accumulated result exceeds $2^{(accumulator\_width)}$-1, the OV Accumulator Overflow bit is set.

The number of samples to be accumulated is determined by the ADRPT (A/D Repeat Setting) register. Each time a sample is added to the accumulator, the ADCNT register is incremented. Once ADRPT samples are accumulated (ADCNT = ADRPT), an accumulator clear command can be issued by the software by setting the ACLR bit. Setting the ACLR bit will also clear the OV bit, as well as the ADCNT register. The ACLR bit is cleared by the hardware when accumulator clearing action is complete.

Important: When ADC is operating from FRC, five FRC clock cycles are required to execute the ADACC clearing operation.

The CRS bits control the data shift on the accumulator result, which effectively divides the value in accumulator (ADACCU:ADACCH:ADACCL) register pair. For the Accumulate mode of the digital filter, the shift provides a simple scaling operation. For the Average/Burst Average mode, the Shift bits are used to determine the number of logical right shifts to be performed on the accumulated result. For the Low-pass Filter mode, the shift is an integral part of the filter, and determines the cut-off frequency of the filter. The table below shows the -3 dB cut-off frequency in ωT (radians) and the highest signal attenuation obtained by this filter at nyquist frequency (ωT = π).

Table 20-5. Low-pass Filter -3 dB Cut-off Frequency

CRS	ωT (radians) @ -3 dB Frequency	dB @ $F_{nyquist}$=1/(2T)
1	0.72	-9.5
2	0.284	-16.9
3	0.134	-23.5
4	0.065	-29.8
5	0.032	-36.0
6	0.016	-42.0
7	0.0078	-48.1

20.6.2 Basic Mode

Basic mode (MD = 000) disables all additional computation features. In this mode, no accumulation occurs but threshold error comparison is performed. Double sampling, Continuous mode, and all CVD features are still available, but no features involving the digital filter/average features are used.

20.6.3 Accumulate Mode

In Accumulate mode (MD = 001), after every conversion, the ADC result is added to the ADACC register. The ADACC register is right-shifted by the value of the CRS bits. This right-shifted value is copied into the ADFLT register. The Formatting mode does not affect the right-justification of the ADFLT value. Upon

23. (CMP) Comparator Module

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed-signal building blocks because they provide analog functionality independent of program execution. The PIC16(L)F18455/56 devices have 2 comparators (C1/C2).

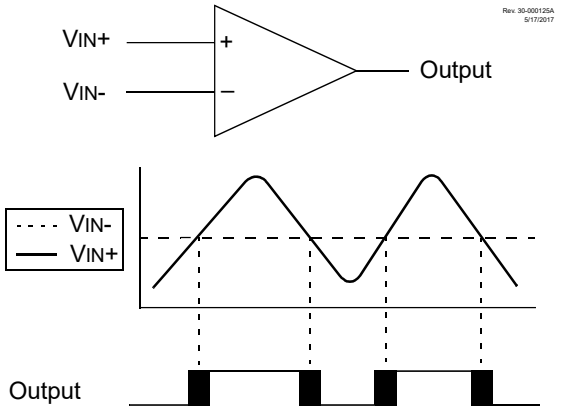
The analog comparator module includes the following features:

- Programmable Input Selection
- Programmable Output Polarity
- Rising/Falling Output Edge Interrupts
- Wake-up from Sleep
- CWG Auto-shutdown Source
- Selectable Voltage Reference
- ADC Auto-Trigger
- Odd Numbered Timers (Timer1, Timer3, etc.) Gate
- Even Numbered Timers (Timer2, Timer4, etc.) Reset
- CCP Capture Mode Input
- DSM Modulator Source
- Input and Window Signal-to-Signal Measurement Timer

23.1 Comparator Overview

A single comparator is shown in Figure 23-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at V_{IN}+ is less than the analog voltage at V_{IN}-, the output of the comparator is a digital low level. When the analog voltage at V_{IN}+ is greater than the analog voltage at V_{IN}-, the output of the comparator is a digital high level.

Figure 23-1. Single Comparator



Note:

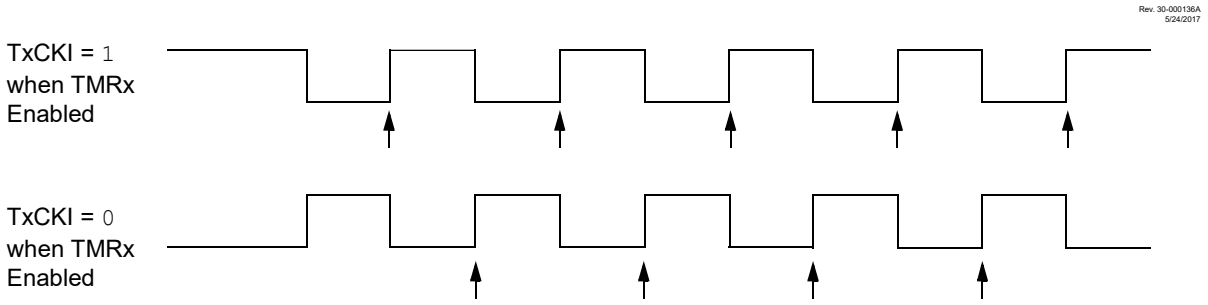
1. The black areas of the output of the comparator represent the uncertainty due to input offsets and response time.

When the F_{OSC} internal clock source is selected, the Timer1 register value will increment by four counts every instruction clock cycle. Due to this condition, a 2 LSB error in resolution will occur when reading the Timer1 value. To utilize the full resolution of Timer1, an asynchronous input signal must be used to gate the Timer1 clock input.

Important: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after any one or more of the following conditions:

- Timer1 enabled after POR
- Write to TMRxH or TMRxL
- Timer1 is disabled
- Timer1 is disabled (TMRxON = 0) when TxCKI is high then Timer1 is enabled (TMRxON = 1) when TxCKI is low. Refer to the figure below.

Figure 26-2. Timer1 Incrementing Edge



Note:

1. Arrows indicate counter increments.
2. In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

26.2.2 External Clock Source

When the external clock source is selected, the Timer1 module may work as a timer or a counter.

When enabled to count, Timer1 is incremented on the rising edge of the external clock input of the TxCKIPPS pin. This external clock source can be synchronized to the system clock or it can run asynchronously.

26.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The CKPS bits control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMRxH or TMRxL.

26.4 Secondary Oscillator

A secondary low-power 32.768 kHz oscillator circuit is built-in between pins SOSCI (input) and SOSCO (amplifier output). This internal circuit is to be used in conjunction with an external 32.768 kHz crystal. The secondary oscillator is not dedicated only to Timer1; it can also be used by other modules.

11. Select the clock source with the CS bits.
12. Set the EN bit to enable the module.
13. Clear the TRIS bits that correspond to the CWG outputs to set them as outputs.

If auto-restart is to be used, set the REN bit and the SHUTDOWN bit will be cleared automatically. Otherwise, clear the SHUTDOWN bit in software to start the CWG.

32.12.3 MDxCARH

Name: MDxCARH
Address: 0x089B

Modulation High Carrier Control Register

Bit	7	6	5	4	3	2	1	0
					CHS[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – CHS[3:0] Modulator Carrier High Selection bits

Table 32-5. MDCARH Source Selections

MDCARH	
CHS<3:0>	**Connection**
1111	CCP5 OUT
1110	CLC4 OUT
1101	CLC3 OUT
1100	CLC2 OUT
1011	CLC1 OUT
1010	NCO1 OUT
1001	PWM7 OUT
1000	PWM6 OUT
0111	CCP4 OUT
0110	CCP3 OUT
0101	CCP2 OUT
0100	CCP1 OUT
0011	CLKREF output
0010	HFINTOSC
0001	F_{OSC} (system clock)
0000	Pin selected by MDCARHPPS

33.8 Register Definitions: Configurable Logic Cell

Long bit name prefixes for the CLC peripherals are shown in the table below. Refer to the *"Long Bit Names Section"* for more information.

Table 33-2. CLC Bit Name Prefixes

Peripheral	Bit Name Prefix
CLC1	LC1
CLC2	LC2
CLC3	LC3
CLC4	LC4

Related Links

1.4.2.2 Long Bit Names

Address	Name	Bit Pos.								
0x1103	STATUS	7:0				TO	PD	Z	DC	C
0x1104	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1106	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1108	BSR	7:0			BSR[5:0]					
0x1109	WREG	7:0	WREG[7:0]							
0x110A	PCLATH	7:0		PCLATH[6:0]						
0x110B	INTCON	7:0	GIE	PEIE						INTEDG
0x110C ... 0x117F	Reserved									
0x1180	INDF0	7:0	INDF0[7:0]							
0x1181	INDF1	7:0	INDF1[7:0]							
0x1182	PCL	7:0	PCL[7:0]							
0x1183	STATUS	7:0				TO	PD	Z	DC	C
0x1184	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1186	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1188	BSR	7:0			BSR[5:0]					
0x1189	WREG	7:0	WREG[7:0]							
0x118A	PCLATH	7:0		PCLATH[6:0]						
0x118B	INTCON	7:0	GIE	PEIE						INTEDG
0x118C ... 0x11FF	Reserved									
0x1200	INDF0	7:0	INDF0[7:0]							
0x1201	INDF1	7:0	INDF1[7:0]							
0x1202	PCL	7:0	PCL[7:0]							
0x1203	STATUS	7:0				TO	PD	Z	DC	C
0x1204	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1206	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1208	BSR	7:0			BSR[5:0]					
0x1209	WREG	7:0	WREG[7:0]							
0x120A	PCLATH	7:0		PCLATH[6:0]						
0x120B	INTCON	7:0	GIE	PEIE						INTEDG
0x120C ... 0x127F	Reserved									
0x1280	INDF0	7:0	INDF0[7:0]							
0x1281	INDF1	7:0	INDF1[7:0]							
0x1282	PCL	7:0	PCL[7:0]							
0x1283	STATUS	7:0				TO	PD	Z	DC	C

areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KeeLoq® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

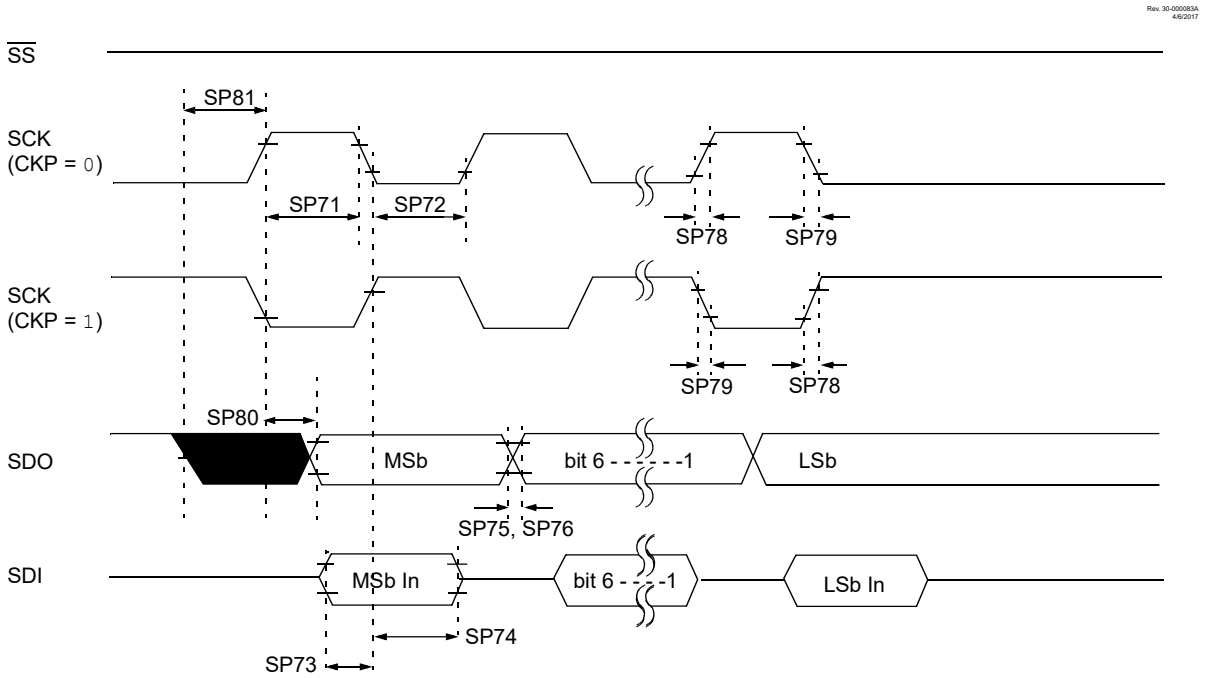
41.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

Standard Operating Conditions (unless otherwise stated)							
Param No.	Sym.	Characteristic	Min.	Typ. †	Max.	Units	Conditions
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.							

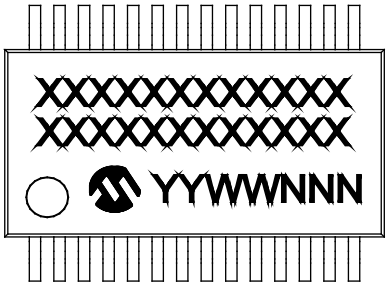
Figure 42-17. SPI Master Mode Timing (CKE = 0, SMP = 0)



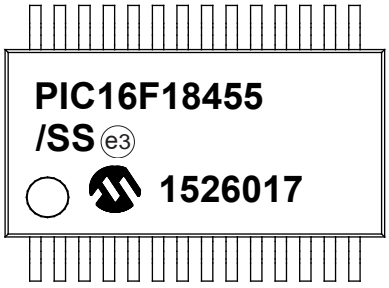
Note: Refer to Figure 42-4 for load conditions.

Rev. 30-009028C
5/17/2017

28-Lead SSOP (5.30 mm)

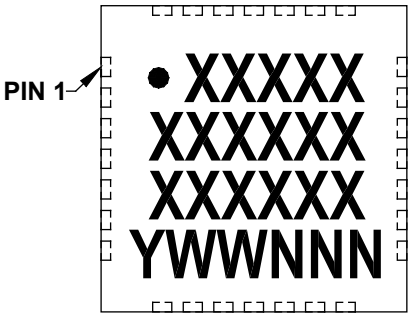


Example

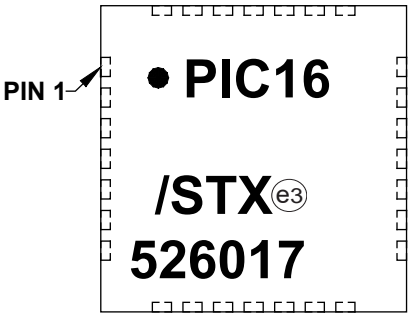


Rev. 30-009028F
4/2/2018

28-Lead VQFN (4x4x1 mm)



Example



44.1 Package Details

The following sections give the technical details of the packages.