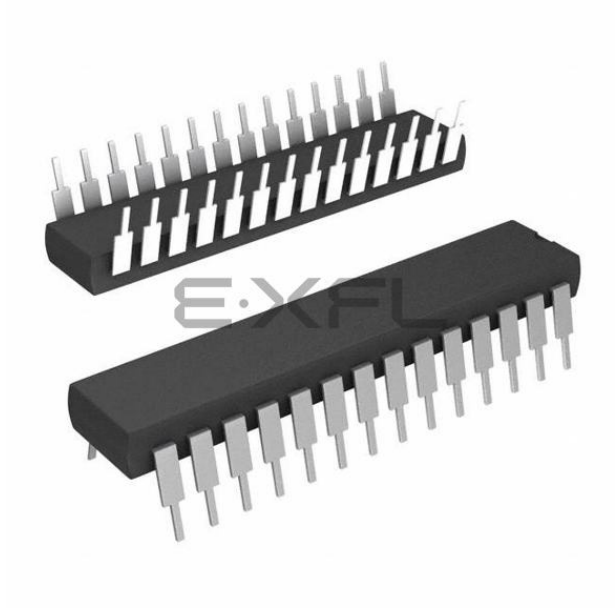


Welcome to E-XFL.COM

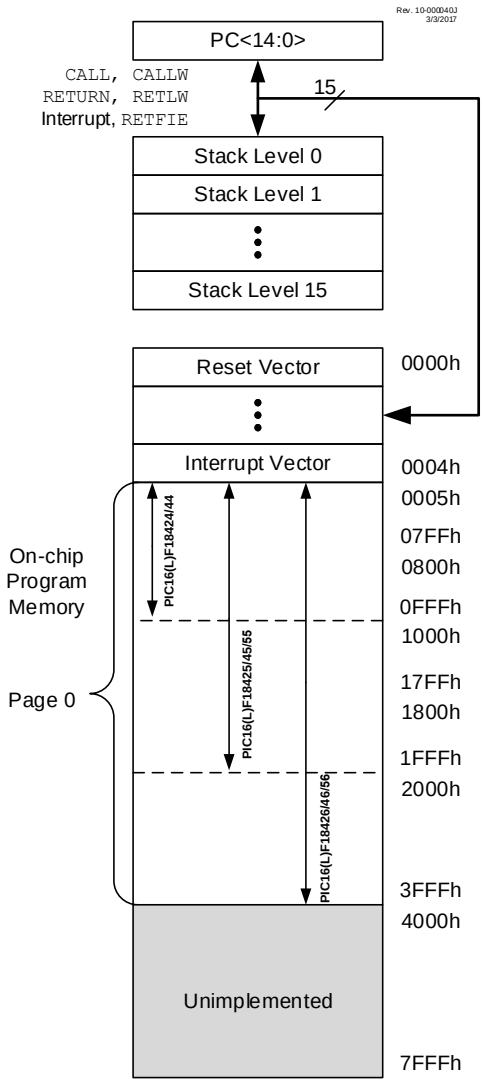
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18456-i-sp

Figure 7-1. Program Memory and Stack



Related Links

4.7.5 CONFIG5

7.2.5 Memory Violation

7.1.1 Reading Program Memory as Data

There are three methods of accessing constants in program memory. The first method is to use tables of `RETLW` instructions. The second method is to set an FSR to point to the program memory. The third method is to use the NVMREG interface to access the program memory.

Related Links

13.4 NVMREG Access

7.8.4 STATUS

Name: STATUS
Address: 0x03 + n*0x80 [n=0..63]

Status Register

Bit	7	6	5	4	3	2	1	0
				$\overline{TO}$	$\overline{PD}$	Z	DC	C
Access				RO	RO	R/W	R/W	R/W
Reset				1	1	0	0	0

Bit 4 – $\overline{TO}$ Time-Out bit
Reset States: POR/BOR = 1
All Other Resets = q

Value	Description
1	Set at power-up or by execution of `CLRWDT` or `SLEEP` instruction
0	A WDT time-out occurred

Bit 3 – $\overline{PD}$ Power-Down bit
Reset States: POR/BOR = 1
All Other Resets = q

Value	Description
1	Set at power-up or by execution of `CLRWDT` instruction
0	Cleared by execution of the `SLEEP` instruction

Bit 2 – Z Zero bit
Reset States: POR/BOR = 0
All Other Resets = u

Value	Description
1	The result of an arithmetic or logic operation is zero
0	The result of an arithmetic or logic operation is not zero

Bit 1 – DC Digit Carry/$\overline{Borrow}$ bit(1)
`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions
Reset States: POR/BOR = 0
All Other Resets = u

Value	Description
1	A carry-out from the 4th low-order bit of the result occurred
0	No carry-out from the 4th low-order bit of the result

Bit 0 – C Carry/$\overline{Borrow}$ bit(1)
`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions
Reset States: POR/BOR = 0
All Other Resets = u

11.3.2 Idle and WWDT

When in Idle, the WWDT Reset is blocked and will instead wake the device. The WWDT wake-up is not an interrupt, therefore ROI does not apply.

Important: The WWDT can bring the device out of Idle, in the same way it brings the device out of Sleep. The DOZEN bit is not affected.

12.8.4 WDTPSL

Name: WDTPSL
Address: 0x80E

WWDT Prescale Select Low Register (Read-Only)

Bit	7	6	5	4	3	2	1	0
	PSCNTL[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – PSCNTL[7:0] Prescale Select Low Byte bits(1)

Note:

1. The 18-bit WDT prescale value, PSCNT<17:0> includes the WDTPSL, WDTPSH and the lower bits of the WDTTMR registers. PSCNT<17:0> is intended for debug operations and should be read during normal operation.

14.7.3 PORTC

Name: PORTC
Address: 0x00E

PORTC Register

Bit	7	6	5	4	3	2	1	0
	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 0, 1, 2, 3, 4, 5, 6, 7 – RCn Port I/O Value bits
Reset States: POR/BOR = xxxxxxxx
All Other Resets = uuuuuuuu

Value	Description
1	Port pin is ≥ V_{IH}
0	Port pin is ≤ V_{IL}

Note: Writes to PORTC are actually written to the corresponding LATC register. Reads from PORTC register return actual I/O pin values.

14.7.7 TRISC

Name: TRISC
Address: 0x014

Tri-State Control Register

Bit	7	6	5	4	3	2	1	0
	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 0, 1, 2, 3, 4, 5, 6, 7 – TRISCn TRISC Port I/O Tri-state Control bits

Value	Description
1	Port output driver is disabled
0	Port output driver is enabled

17.6.10 IOCBP

Name: IOCBP
Address: 0x1F48

Interrupt-on-Change Positive Edge Register

Bit	7	6	5	4	3	2	1	0
	IOCBP7	IOCBP6	IOCBP5	IOCBP4	IOCBP3	IOCBP2	IOCBP1	IOCBP0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 – IOCBPn Interrupt-on-Change Positive Edge Enable bits

Value	Description
1	Interrupt-on-Change enabled on the IOCB pin for a positive-going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0	Interrupt-on-Change disabled for the associated pin.

Value	Description
01	ADC FVR Buffer Gain is 1x, (1.024V)
00	ADC FVR Buffer is off

Note:

1. Fixed Voltage Reference output cannot exceed V_{DD}.
2. See *Temperature Indicator Module* section for additional information.

Related Links

19. Temperature Indicator Module

```
movwf   ADCON0      ;Turn ADC On
call    SampleTime  ;Acquisiton delay
bsf     ADCON0,ADGO ;Start conversion
btfsc   ADCON0,ADGO ;Is conversion done?
goto    $-1         ;No, test again
BANKSEL ADRESH      ;
movf    ADRESH,W    ;Read upper 2 bits
movwf   RESULTHI    ;store in GPR space
movf    ADRESL,W    ;Read lower 8 bits
movwf   RESULTLO    ;Store in GPR space
```

Example 20-2. ADC Conversion (C)

```
/*This code block configures the ADC
for polling, VDD and VSS references, ADCRC
oscillator and AN0 input.
Conversion start & polling for completion
are included.
*/
void main() {
//System Initialize
initializeSystem();

//Setup ADC
ADCON0bits.FM = 1;      //right justify
ADCON0bits.CS = 1;      //FRC Clock
ADPCH = 0x00;           //RA0 is Analog channel
TRISAbits.TRISA0 = 1;   //Set RA0 to input
ANSELAbits.ANSELA0 = 1; //Set RA0 to analog
ADCON0bits.ON = 1;      //Turn ADC On

while (1) {
ADCON0bits.GO = 1;     //Start conversion
while (ADCON0bits.GO); //Wait for conversion done
resultHigh = ADRESH;   //Read result
resultLow = ADRESL;    //Read result
}
}
```

Related Links

20.3 ADC Acquisition Requirements

20.3 ADC Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (C_{HOLD}) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in the following figure. The source impedance (R_S) and the internal sampling switch (R_{SS}) impedance directly affect the time required to charge the capacitor C_{HOLD}. The sampling switch (R_{SS}) impedance varies over the device voltage (V_{DD}), refer to the following figure.

26.14.2 TxGCON

Name: TxGCON
Address: 0x20F,0x215,0x21B

Timer Gate Control Register

Bit	7	6	5	4	3	2	1	0
	GE	GPOL	GTM	GSPM	GGO/DONE	GVAL		
Access	R/W	R/W	R/W	R/W	R/W	RO		
Reset	0	0	0	0	0	x		

Bit 7 – GE Timer Gate Enable bit
Reset States: POR/BOR = 0
All Other Resets = u

Value	Condition	Description
1	ON = 1	Timer counting is controlled by the Timer gate function
0	ON = 1	Timer is always counting
X	ON = 0	This bit is ignored

Bit 6 – GPOL Timer Gate Polarity bit
Reset States: POR/BOR = 0
All Other Resets = u

Value	Description
1	Timer gate is active-high (Timer counts when gate is high)
0	Timer gate is active-low (Timer counts when gate is low)

Bit 5 – GTM Timer Gate Toggle Mode bit
Timer Gate Flip-Flop Toggles on every rising edge

Reset States: POR/BOR = 0
All Other Resets = u

Value	Description
1	Timer Gate Toggle mode is enabled
0	Timer Gate Toggle mode is disabled and Toggle flip-flop is cleared

Bit 4 – GSPM Timer Gate Single Pulse Mode bit
Reset States: POR/BOR = 0
All Other Resets = u

Value	Description
1	Timer Gate Single Pulse mode is enabled and is controlling Timer gate)
0	Timer Gate Single Pulse mode is disabled

Bit 3 – GGO/$\overline{\text{DONE}}$ Timer Gate Single Pulse Acquisition Status bit
This bit is automatically cleared when TxGSPM is cleared.

Reset States: POR/BOR = 0
All Other Resets = u

30. (PWM) Pulse-Width Modulation

The PWM module generates a Pulse-Width Modulated signal determined by the duty cycle, period, and resolution that are configured by the following registers:

- TxPR
- TxCON
- PWMxDC
- PWMxCON

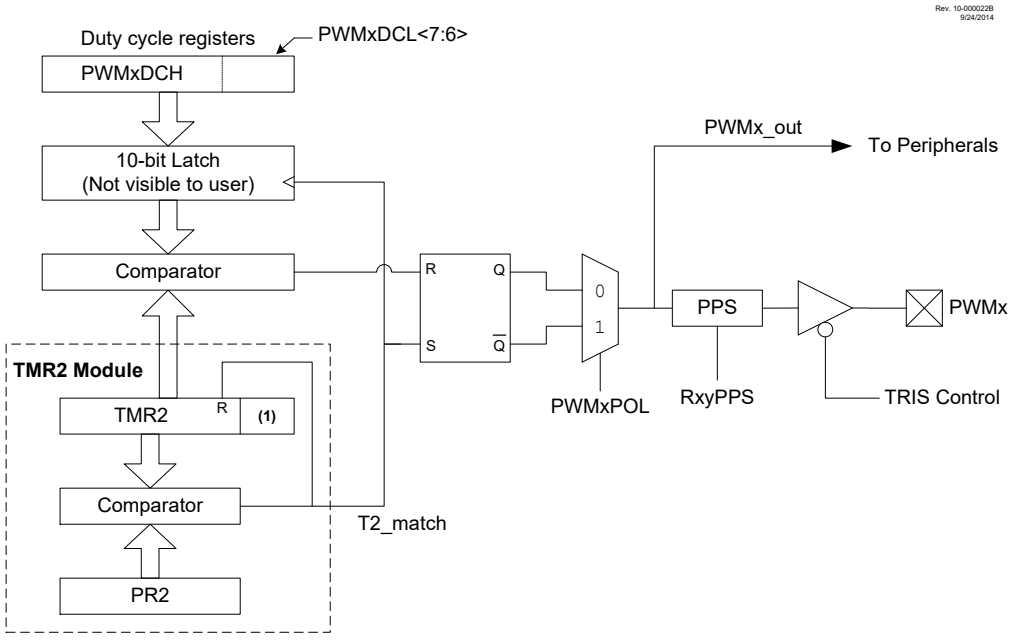
Important: The corresponding TRIS bit must be cleared to enable the PWM output on the PWMx pin.

Each PWM module can select the timer source that controls the module. Note that the PWM mode operation is described with respect to TMR2 in the following sections.

Figure 30-1 shows a simplified block diagram of PWM operation.

Figure 30-2 shows a typical waveform of the PWM signal.

Figure 30-1. Simplified PWM Block Diagram



Note:

1. 8-bit timer is concatenated with two bits generated by Fosc or two bits of the internal prescaler to create 10-bit time base.

31. (CWG) Complementary Waveform Generator Module

The Complementary Waveform Generator (CWG) produces half-bridge, full-bridge, and steering of PWM waveforms. It is backwards compatible with previous CCP functions. The PIC16(L)F18455/56 family has 3 instance(s) of the CWG module.

The CWG has the following features:

- Six Operating modes:
  - Synchronous Steering mode
  - Asynchronous Steering mode
  - Full-Bridge mode, Forward
  - Full-Bridge mode, Reverse
  - Half-Bridge mode
  - Push-Pull mode
- Output Polarity Control
- Output Steering
- Independent 6-Bit Rising and Falling Event Dead-Band Timers:
  - Clocked dead band
  - Independent rising and falling dead-band enables
- Auto-Shutdown Control With:
  - Selectable shutdown sources
  - Auto-restart option
  - Auto-shutdown pin override control

31.1 Fundamental Operation

The CWG generates two output waveforms from the selected input source.

The off-to-on transition of each output can be delayed from the on-to-off transition of the other output, thereby, creating a time delay immediately where neither output is driven. This is referred to as dead time and is covered in 31.7 Dead-Band Control.

It may be necessary to guard against the possibility of circuit faults or a feedback event arriving too late or not at all. In this case, the active drive must be terminated before the Fault condition causes damage. This is referred to as auto-shutdown and is covered in 31.11 Auto-Shutdown.

31.2 Operating Modes

The CWG module can operate in six different modes, as specified by the MODE bits:

- Half-Bridge mode
- Push-Pull mode
- Asynchronous Steering mode
- Synchronous Steering mode
- Full-Bridge mode, Forward
- Full-Bridge mode, Reverse

34.6.2 CLKRCLK

Name: CLKRCLK
Address: 0x896

Clock Reference Clock Selection MUX

Bit	7	6	5	4	3	2	1	0
					CLK[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – CLK[3:0] CLKR Clock Selection bits
See the Clock Sources table.

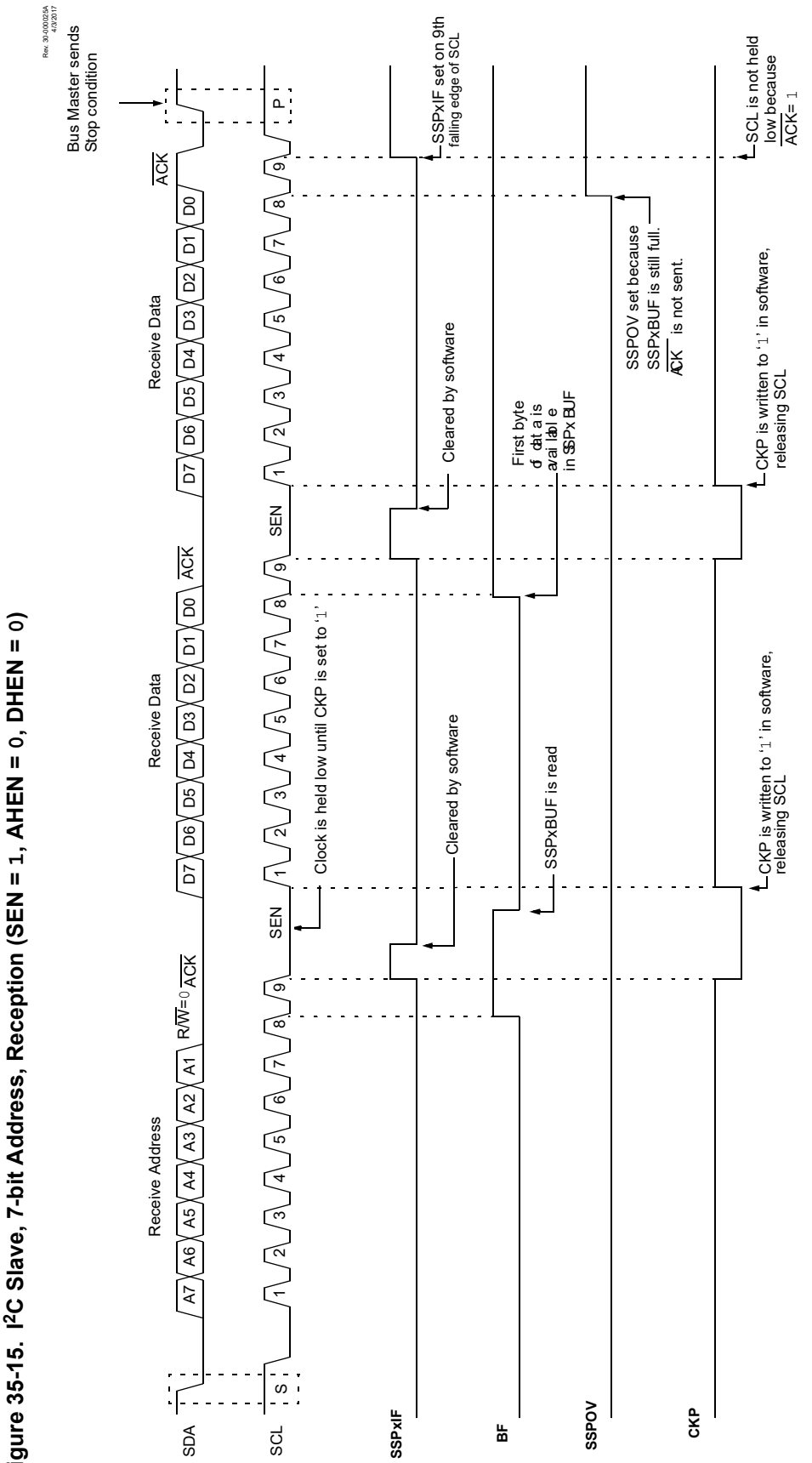
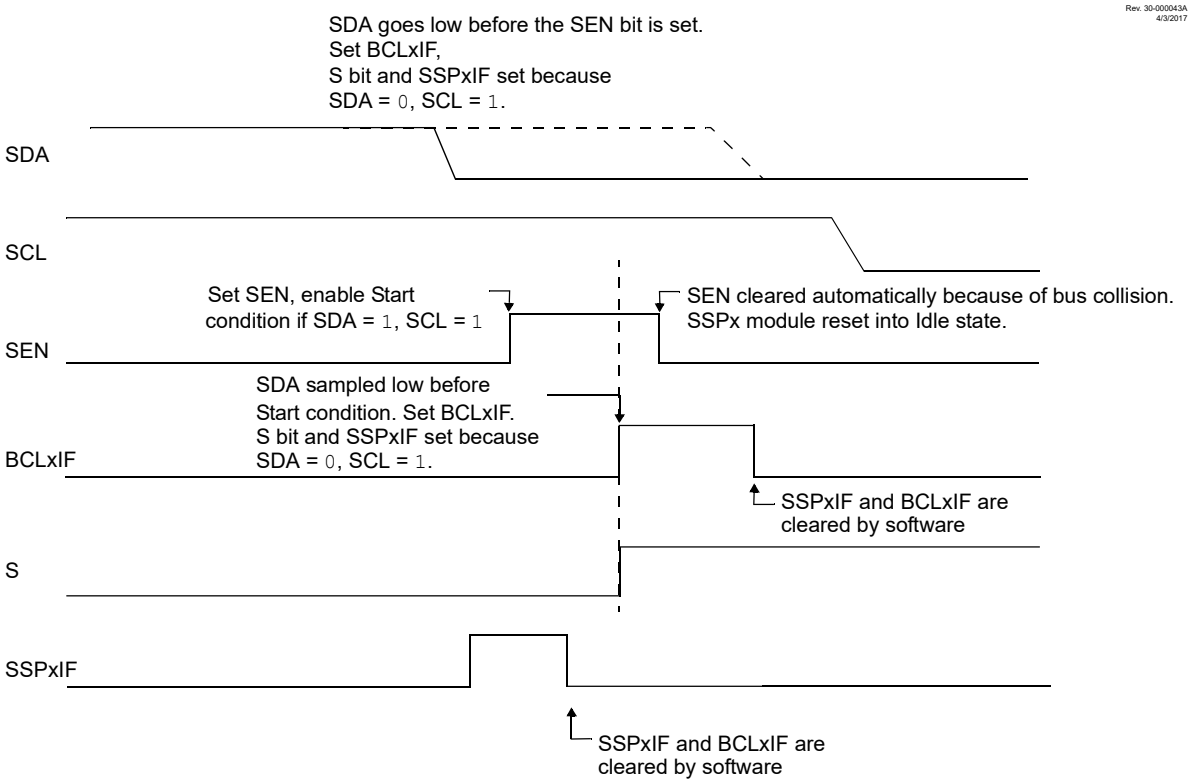


Figure 35-15. I²C Slave, 7-bit Address, Reception (SEN = 1, AHEN = 0, DHEN = 0)

Figure 35-33. Bus Collision During Start Condition (SDA Only)



The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCL pin is sampled low while SDA is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

Figure 35-34. Bus Collision During Start Condition (SCL = 0)

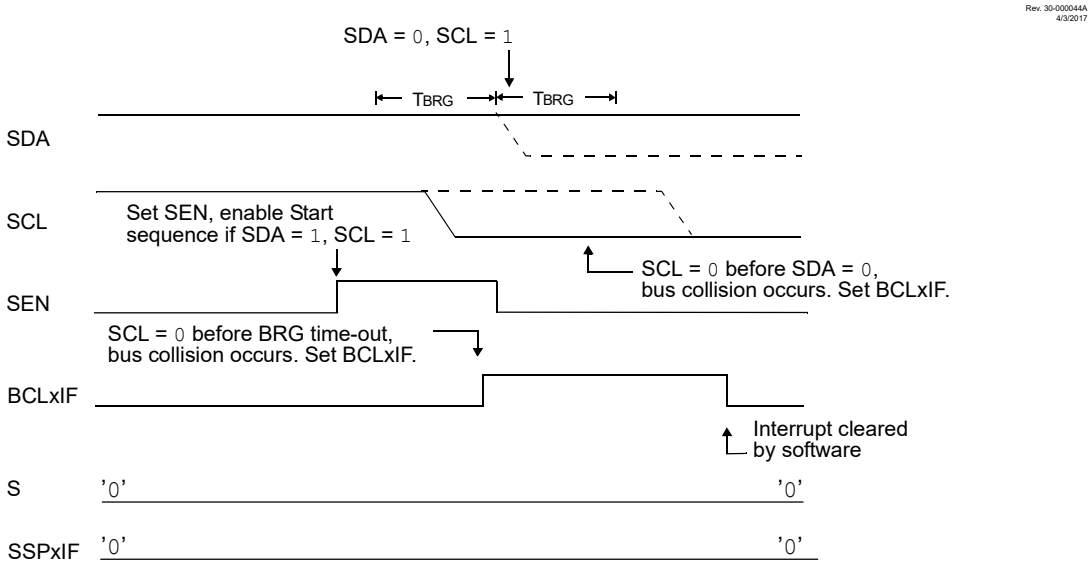
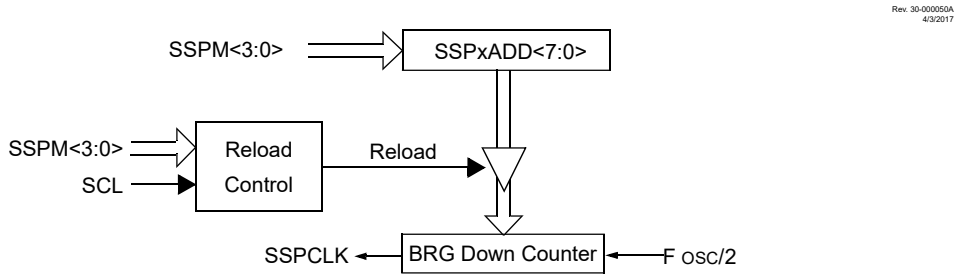


Table 35-1 illustrates clock rates based on instruction cycles and the BRG value loaded into SSPxADD.

Example 35-1. MSSP Baud Rate Generator Frequency Equation

$$F_{CLOCK} = \frac{F_{OSC}}{4 \times (SSPxADD + 1`)}$$

Figure 35-40. Baud Rate Generator Block Diagram



Important: Values of 0x00, 0x01 and 0x02 are not valid for SSPxADD when used as a Baud Rate Generator for I^2C. This is an implementation limitation.

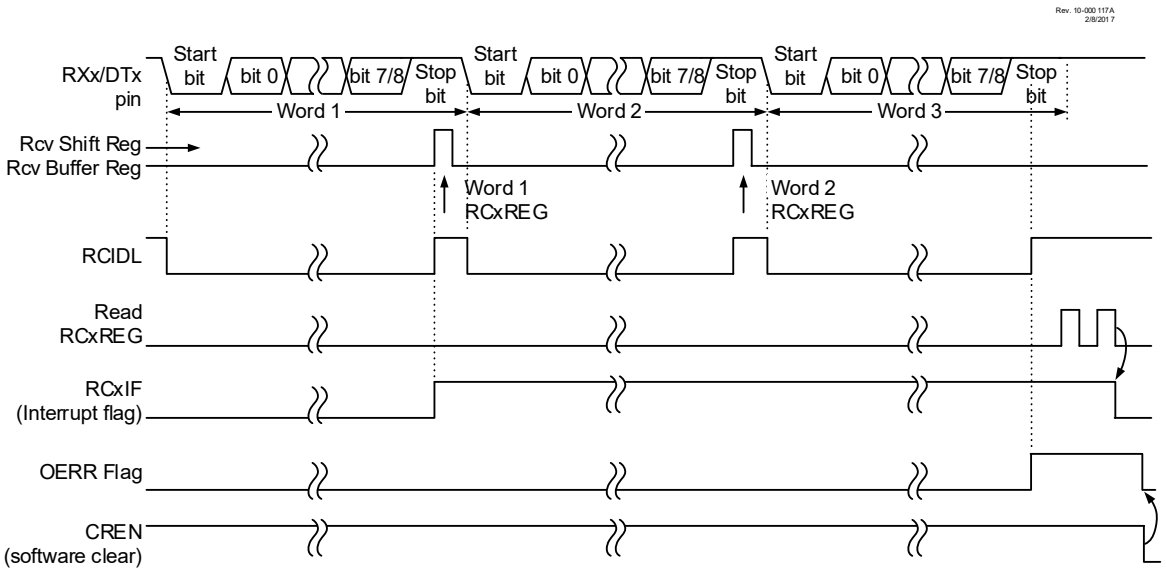
Table 35-1. MSSP Clock Rate w/BRG

F_{OSC}	F_{CY}	BRG Value	Fclock (2 Rollovers of BRG)
32 MHz	8 MHz	13h	400 kHz
32 MHz	8 MHz	19h	308 kHz
32 MHz	8 MHz	4Fh	100 kHz
16 MHz	4 MHz	09h	400 kHz
16 MHz	4 MHz	0Ch	308 kHz
16 MHz	4 MHz	27h	100 kHz
4 MHz	1 MHz	09h	100 kHz

Note: Refer to the I/O port electrical specifications in the "*Electrical Specifications*" section, Internal Oscillator Parameters, to ensure the system is designed to support Iol requirements.

5. If interrupts are desired, set the RCxIE bit of the PIEx register and the GIE and PEIE bits of the INTCON register.
6. Enable 9-bit reception by setting the RX9 bit.
7. Enable address detection by setting the ADDEN bit.
8. Enable reception by setting the CREN bit.
9. The RCxIF interrupt flag bit will be set when a character with the ninth bit set is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCxIE interrupt enable bit is also set.
10. Read the RCxSTA register to get the error flags. The ninth data bit will always be set.
11. Get the received eight Least Significant data bits from the receive buffer by reading the RCxREG register. Software determines if this is the device's address.
12. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.
13. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and generate interrupts.

Figure 36-5. Asynchronous Reception



Note: This timing diagram shows three bytes appearing on the RXx input. The OERR flag is set because the RCxREG is not read before the third word is received.

36.1.3 Clock Accuracy with Asynchronous Operation

The factory calibrates the internal oscillator block output (INTOSC). However, the INTOSC frequency may drift as V_{DD} or temperature changes, and this directly affects the asynchronous baud rate. Two methods may be used to adjust the baud rate clock, but both require a reference clock source of some kind.

The first (preferred) method uses the OSCTUNE register to adjust the INTOSC output. Adjusting the value in the OSCTUNE register allows for fine resolution changes to the system clock source.

The other method adjusts the value in the Baud Rate Generator. This can be done automatically with the Auto-Baud Detect feature (see 36.2.1 Auto-Baud Detect). There may not be fine enough resolution when adjusting the Baud Rate Generator to compensate for a gradual change in the peripheral clock frequency.

Address	Name	Bit Pos.								
0x0E01	INDF1	7:0	INDF1[7:0]							
0x0E02	PCL	7:0	PCL[7:0]							
0x0E03	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x0E04	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0E06	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0E08	BSR	7:0			BSR[5:0]					
0x0E09	WREG	7:0	WREG[7:0]							
0x0E0A	PCLATH	7:0		PCLATH[6:0]						
0x0E0B	INTCON	7:0	GIE	PEIE						INTEDG
0x0E0C ... 0x0E7F	Reserved									
0x0E80	INDF0	7:0	INDF0[7:0]							
0x0E81	INDF1	7:0	INDF1[7:0]							
0x0E82	PCL	7:0	PCL[7:0]							
0x0E83	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x0E84	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0E86	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0E88	BSR	7:0			BSR[5:0]					
0x0E89	WREG	7:0	WREG[7:0]							
0x0E8A	PCLATH	7:0		PCLATH[6:0]						
0x0E8B	INTCON	7:0	GIE	PEIE						INTEDG
0x0E8C ... 0x0EFF	Reserved									
0x0F00	INDF0	7:0	INDF0[7:0]							
0x0F01	INDF1	7:0	INDF1[7:0]							
0x0F02	PCL	7:0	PCL[7:0]							
0x0F03	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x0F04	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0F06	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0F08	BSR	7:0			BSR[5:0]					
0x0F09	WREG	7:0	WREG[7:0]							
0x0F0A	PCLATH	7:0		PCLATH[6:0]						
0x0F0B	INTCON	7:0	GIE	PEIE						INTEDG
0x0F0C ... 0x0F7F	Reserved									
0x0F80	INDF0	7:0	INDF0[7:0]							
0x0F81	INDF1	7:0	INDF1[7:0]							

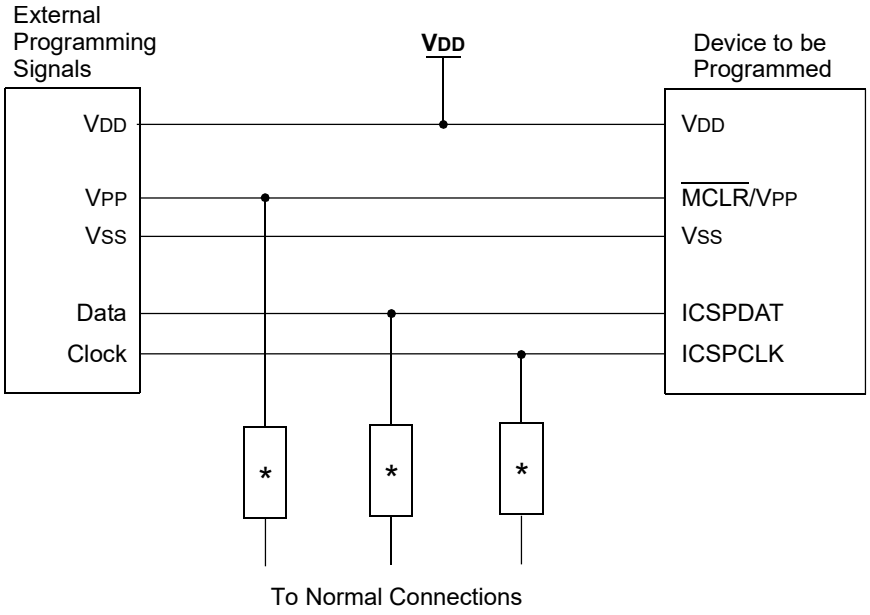
5 = ICSPCLK

6 = No Connect

Note:

1. **Note:** The 6-pin header (0.100" spacing) accepts 0.025" square pins.

Figure 39-3. Typical Connection for ICSP™ Programming



* Isolation devices (as required).

43.1 Graphs

Figure 43-1. High Range Temperature Indicator Voltage Sensitivity Across Temperature

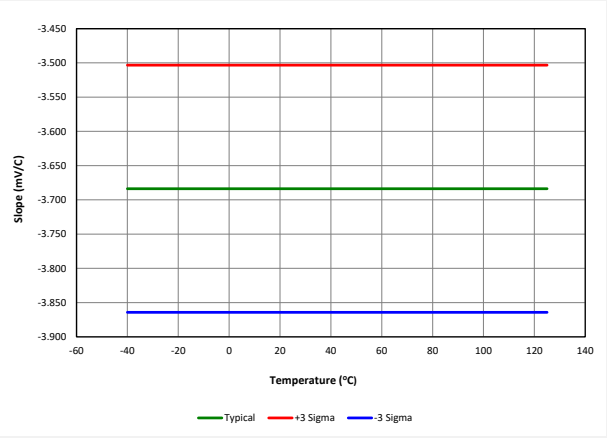


Figure 43-2. Low Range Temperature Indicator Voltage Sensitivity Across Temperature