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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18456-i-ss

7.10.1 STATUS_SHAD

Name: STATUS_SHAD
Address: 0x1FE4

Shadow of Status Register

Bit	7	6	5	4	3	2	1	0
				$\overline{TO}$	$\overline{PD}$	Z	DC	C
Access				RO	RO	R/W	R/W	R/W
Reset				x	x	x	x	x

Bit 4 – $\overline{TO}$ Time-Out bit
Reset States: POR/BOR = x
All Other Resets = u

Value	Description
1	Set at power-up or by execution of CLRWDT or SLEEP instruction
0	A WDT time-out occurred

Bit 3 – $\overline{PD}$ Power-Down bit
Reset States: POR/BOR = x
All Other Resets = u

Value	Description
1	Set at power-up or by execution of CLRWDT instruction
0	Cleared by execution of the SLEEP instruction

Bit 2 – Z Zero bit
Reset States: POR/BOR = x
All Other Resets = u

Value	Description
1	The result of an arithmetic or logic operation is zero
0	The result of an arithmetic or logic operation is not zero

Bit 1 – DC Digit Carry/$\overline{Borrow}$ bit(1)
ADDWF, ADDLW, SUBLW, SUBWF instructions
Reset States: POR/BOR = x
All Other Resets = u

Value	Description
1	A carry-out from the 4th low-order bit of the result occurred
0	No carry-out from the 4th low-order bit of the result

Bit 0 – C Carry/$\overline{Borrow}$ bit(1)
ADDWF, ADDLW, SUBLW, SUBWF instructions
Reset States: POR/BOR = x
All Other Resets = u

NDIV<3:0>	Clock Divider
0001	2
0000	1

Note:

1. The default value (f) is determined by the CONFIG1[RSTOSC] Configuration bits.
2. If NOSC is written with a reserved value, the operation is ignored and NOSC is not written.
3. When CONFIG1[CSWEN] = 0, this register is read-only and cannot be changed from the POR value.
4. When NOSC = 110 (HFINTOSC 1 MHz), the NDIV bits will default to '0010' upon Reset; for all other NOSC settings the NDIV bits will default to '0000' upon Reset.
5. EXTOSC configured by CONFIG1[FEXTOSC].
6. HFINTOSC frequency is set with the FRQ bits of the OSCFRQ register.

Related Links

4.7.1 CONFIG1
42.4.3 PLL Specifications

Value	Description
1	Enabled
0	Disabled

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by registers PIE1-PIE8.

10.7.19 PIR8

Name: PIR8
Address: 0x714

Peripheral Interrupt Request (Flag) Register 8

Bit	7	6	5	4	3	2	1	0
			SMT2PWAIF	SMT2PRAIF	SMT2IF	SMT1PWAIF	SMT1PRAIF	SMT1IF
Access			R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS
Reset			0	0	0	0	0	0

Bit 5 – SMT2PWAIF SMT2 Pulse-Width Acquisition Interrupt Flag bit

Value	Description
1	Interrupt has occurred (must be cleared by software)
0	Interrupt event has not occurred

Bit 4 – SMT2PRAIF SMT2 Period Acquisition Interrupt Flag bit

Value	Description
1	Interrupt has occurred (must be cleared by software)
0	Interrupt event has not occurred

Bit 3 – SMT2IF SMT2 Interrupt Flag bit

Value	Description
1	Interrupt has occurred (must be cleared by software)
0	Interrupt event has not occurred

Bit 2 – SMT1PWAIF SMT1 Pulse-Width Acquisition Interrupt Flag bit

Value	Description
1	Interrupt has occurred (must be cleared by software)
0	Interrupt event has not occurred

Bit 1 – SMT1PRAIF SMT1 Period Acquisition Interrupt Flag bit

Value	Description
1	Interrupt has occurred (must be cleared by software)
0	Interrupt event has not occurred

Bit 0 – SMT1IF SMT1 Interrupt Flag bit

Value	Description
1	Interrupt has occurred (must be cleared by software)
0	Interrupt event has not occurred

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON appropriate interrupt flag bits are clear prior to enabling an interrupt.

12.8.4 WDTPSL

Name: WDTPSL
Address: 0x80E

WWDT Prescale Select Low Register (Read-Only)

Bit	7	6	5	4	3	2	1	0
	PSCNTL[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – PSCNTL[7:0] Prescale Select Low Byte bits(1)

Note:

1. The 18-bit WDT prescale value, PSCNT<17:0> includes the WDTPSL, WDTPSH and the lower bits of the WDTTMR registers. PSCNT<17:0> is intended for debug operations and should be read during normal operation.

9. Clear the LWLO bit of the NVMCON1 register. When the LWLO bit of the NVMCON1 register is '0', the write sequence will initiate the write to Flash program memory.
10. Load the NVMDATH:NVMDATL register pair with the program memory data to be written.
11. Execute the unlock sequence. The entire program memory latch content is now written to Flash program memory.

Important: The program memory write latches are reset to the blank state (0x7FFF) at the completion of every write or erase operation. As a result, it is not necessary to load all the program memory write latches. Unloaded latches will remain in the blank state.

An example of the complete write sequence is shown in Writing to Program Flash Memory. The initial address is loaded into the NVMADRH:NVMADRL register pair; the data is loaded using indirect addressing.

Figure 13-4. NVMREG Writes to Program Flash Memory With 32 Write Latches

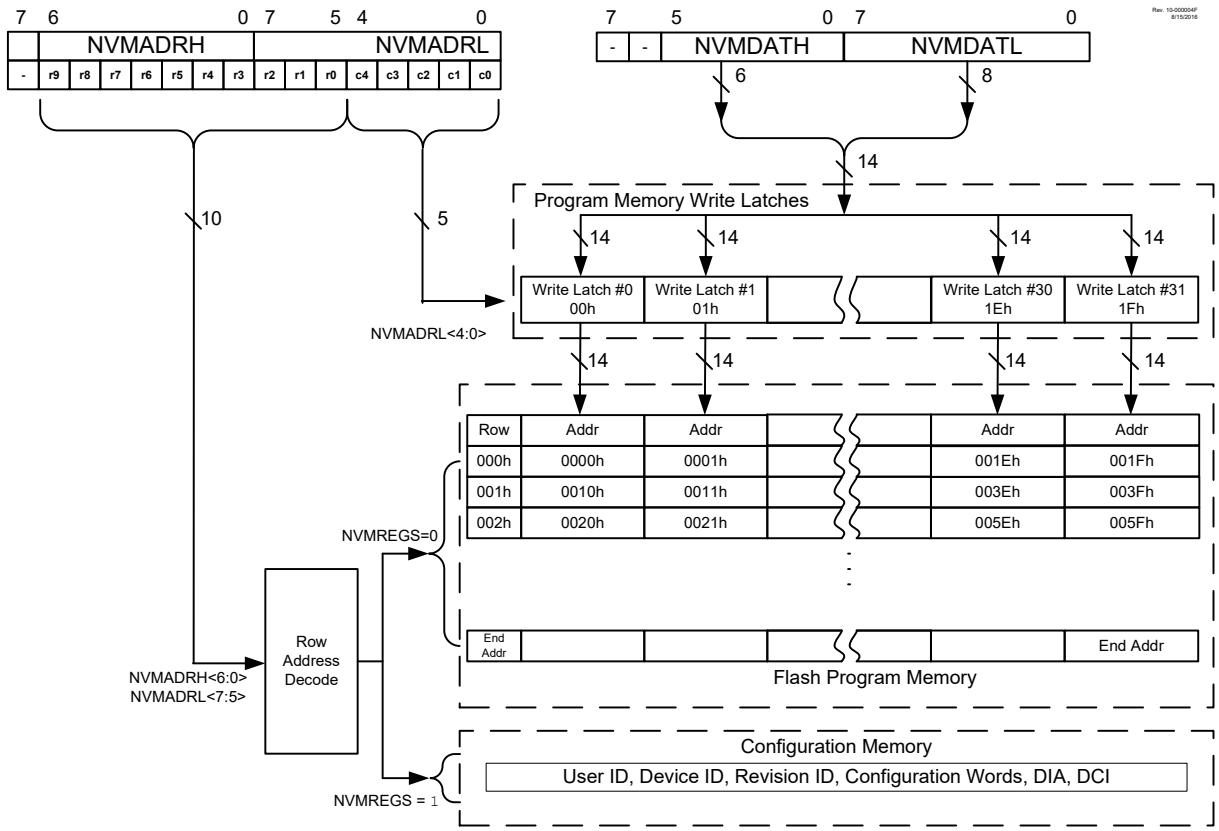
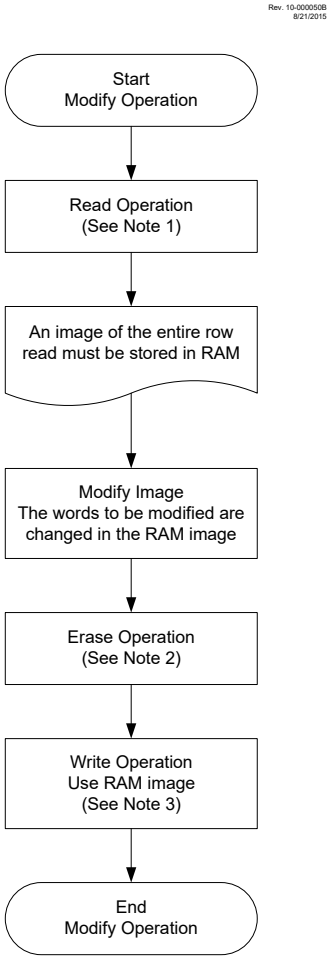


Figure 13-6. Flash Program Memory Modify Flowchart



Note:

1. See Flash Program Memory Read Flowchart.
2. See NVM Erase Flowchart.
3. See Program Flash Memory Flowchart.

13.4.7 NVMREG Access to Device Information Area, Device Configuration Area, User ID, Device ID, EEPROM, and Configuration Words

NVMREGS can be used to access the following memory regions:

- Device Information Area (DIA)
- Device Configuration Information (DCI)
- User ID region
- Device ID and Revision ID
- Configuration Words
- EEPROM

The value of NVMREGS is set to '1' in the NVMCON1 register to access these regions. The memory regions listed above would be pointed to by PC<15> = 1, but not all addresses reference valid data. Different access may exist for reads and writes. Refer to the table below. When read access is initiated on

17.6.4 IOCEF

Name: IOCEF
Address: 0x1F6B

PORTE Interrupt-on-Change Flag Register

Bit	7	6	5	4	3	2	1	0
					IOCEF3			
Access					R/W/HS			
Reset					0			

Bit 3 – IOCEF3 PORTE Interrupt-on-Change Flag bits(1)

Value	Condition	Description
1	IOCEP[n]=1	A positive edge was detected on the RE[n] pin
1	IOCEN[n]=1	A negative edge was detected on the RE[n] pin
0	IOCEP[n]=x and IOCEN[n]=x	No change was detected, or the user cleared the detected change

Note:

1. If MCLRE = 1 or LVP = 1, RE3 port functionality is disabled and IOC on RE3 is not available.

20.8.3 ADCON2

Name: ADCON2
Address: 0x113

ADC Control Register 2

Bit	7	6	5	4	3	2	1	0
	PSIS	CRS[2:0]			ACLR	MD[2:0]		
Access	R/W	R/W	R/W	R/W	R/W/HC	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – PSIS ADC Previous Sample Input Select bits

Value	Description
1	FLTR is transferred to PREV at start-of-conversion
0	ADRES is transferred to PREV at start-of-conversion

Bits 6:4 – CRS[2:0] ADC Accumulated Calculation Right Shift Select bits

Value	Condition	Description
0 to 7	MD = b'100'	Low-pass filter time constant is 2^{CRS}, filter gain is 1:1
0 to 7	MD = b'011' to b'001'	The accumulated value is right-shifted by CRS (divided by 2^{CRS}) **(1,2)**
x	MD = b'000' to b'001'	These bits are ignored

Bit 3 – ACLR A/D Accumulator Clear Command bit**(3)**

Value	Description
1	ACC, OV and CNT bits are cleared
0	Clearing action is complete (or not started)

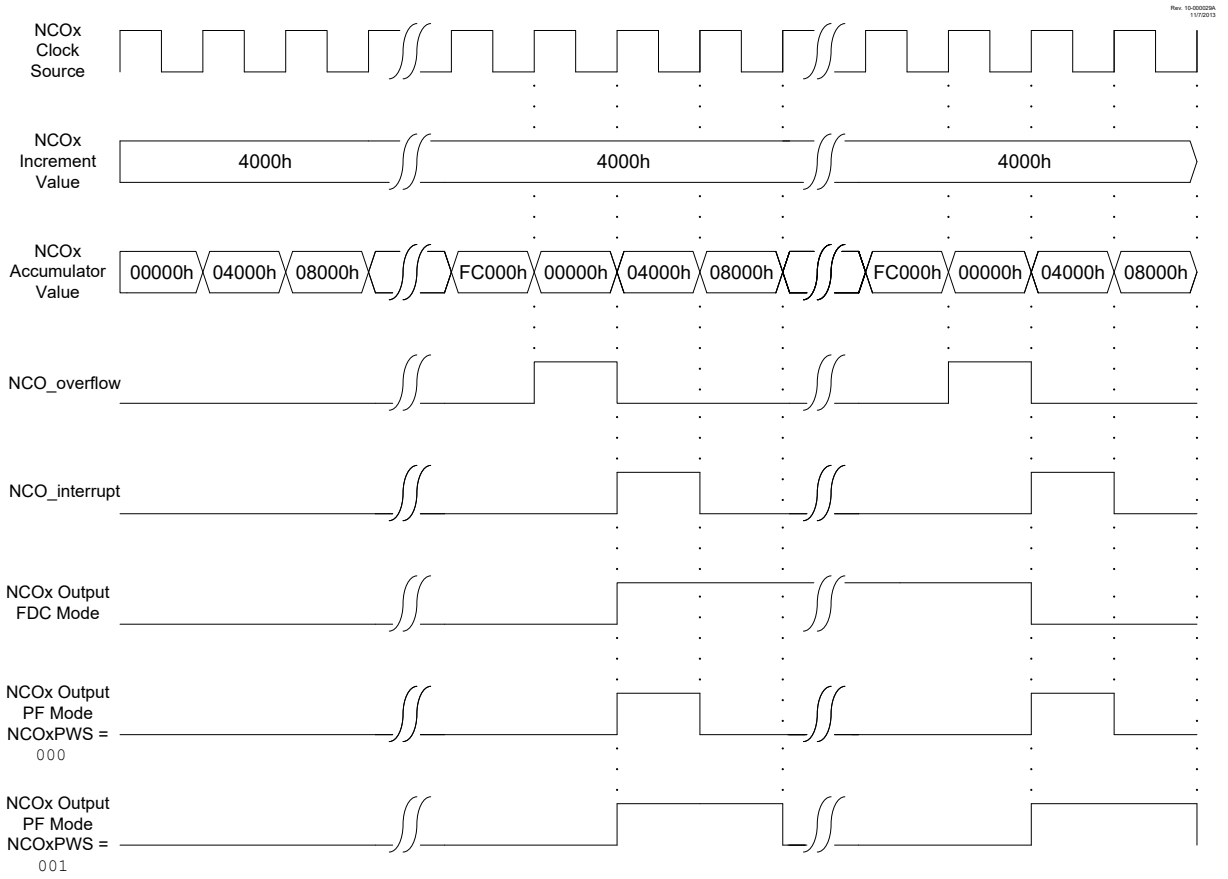
Bits 2:0 – MD[2:0] ADC Operating Mode Selection bits**(4)**

Value	Description
111-101	Reserved
100	Low-pass Filter mode
011	Burst Average mode
010	Average mode
001	Accumulate mode
000	Basic (Legacy) mode

Note:

1. To correctly calculate an average, the number of samples (set in RPT) must be 2^{CRS}.
2. CRS = 3'b111 is a reserved option.
3. This bit is cleared by hardware when the accumulator operation is complete; depending on oscillator selections, the delay may be many instructions.
4. See Computation Modes for full mode descriptions.

Figure 22-2. FDC Output Mode Operation Diagram



Related Links

22.9.1 NCOxCON

22.3 Pulse Frequency Mode

In Pulse Frequency (PF) mode, every time the Accumulator overflows, the output becomes active for one or more clock periods. Once the clock period expires, the output returns to an inactive state. This provides a pulsed output. The output becomes active on the rising clock edge immediately following the overflow event. For more information, see the figure above.

The value of the active and inactive states depends on the POL bit.

The PF mode is selected by setting the PFM bit.

Related Links

22.9.1 NCOxCON

22.3.1 Output Pulse Width Control

When operating in PF mode, the active state of the output can vary in width by multiple clock periods. Various pulse widths are selected with the PWS bits.

When the selected pulse width is greater than the Accumulator overflow time frame, then NCO output does not toggle.

Equation 24-6. Series R for V range

$$R_{SERIES} = \frac{V_{MAX\_PEAK} + V_{MIN\_PEAK}}{7 \times 10^{-4}}$$

24.7 Operation During Sleep

The ZCD current sources and interrupts are unaffected by Sleep.

24.8 Effects of a Reset

The ZCD circuit can be configured to default to the active or inactive state on Power-on Reset (POR). When the $\overline{ZCD}$ Configuration bit is cleared, the ZCD circuit will be active at POR. When the $\overline{ZCD}$ Configuration bit is set, the SEN bit must be set to enable the ZCD module.

24.9 Disabling the ZCD Module

The ZCD module can be disabled in two ways:

1. The $\overline{ZCD}$ Configuration bit disables the ZCD module when set. When this is the case then the ZCD module will be enabled by setting the SEN bit. When the $\overline{ZCD}$ bit is clear, the ZCD is always enabled and the SEN bit has no effect.
2. The ZCD can also be disabled using the ZCDMD bit of the PMDx register. This is subject to the status of the $\overline{ZCD}$ bit.

Mode	MODE<4:0>		Output Operation	Operation	Timer Control		
	<4:3>	<2:0>			Start	Reset	Stop
		100	Edge Triggered Start and Hardware Reset (Note 1)	Rising edge start and Rising edge Reset (Figure 27-9)	ON = 1 and TMRx_ers ↑	TMRx_ers ↑	
		101		Falling edge start and Falling edge Reset	ON = 1 and TMRx_ers ↓	TMRx_ers ↓	
		110		Rising edge start and Low level Reset (Figure 27-10)	ON = 1 and TMRx_ers ↑	TMRx_ers = 0	
		111		Falling edge start and High level Reset	ON = 1 and TMRx_ers ↓	TMRx_ers = 1	
Mono-stable	10	000	Reserved				
		001	Edge Triggered Start (Note 1)	Rising edge start (Figure 27-11)	ON = 1 and TMRx_ers ↑	—	ON = 0 or Next clock after TMRx = PRx (Note 3)
		010		Falling edge start	ON = 1 and TMRx_ers ↓	—	
		011		Any edge start	ON = 1 and TMRx_ers ↕	—	
Reserved		100	Reserved				
Reserved		101	Reserved				
One-shot		110	Level Triggered Start and Hardware Reset	High level start and Low level Reset (Figure 27-12)	ON = 1 and TMRx_ers = 1	TMRx_ers = 0	ON = 0 or Held in Reset (Note 2)
		111		Low level start & High level Reset	ON = 1 and TMRx_ers = 0	TMRx_ers = 1	

Value	Description
0001	1:2 Postscaler
0000	1:1 Postscaler

Note:

1. In certain modes, the ON bit will be auto-cleared by hardware. See Table 27-3.

27.9.5 TxCLKCON

Name: TxCLKCON
Address: 0x290,0x296,0x29C

Timer Clock Source Selection Register

Bit	7	6	5	4	3	2	1	0
					CS[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – CS[3:0] Timer Clock Source Selection bits

Value	Description
n	See Clock Source Selection table

Figure 35-7. SPI Mode Waveform (Slave Mode with CKE = 0)

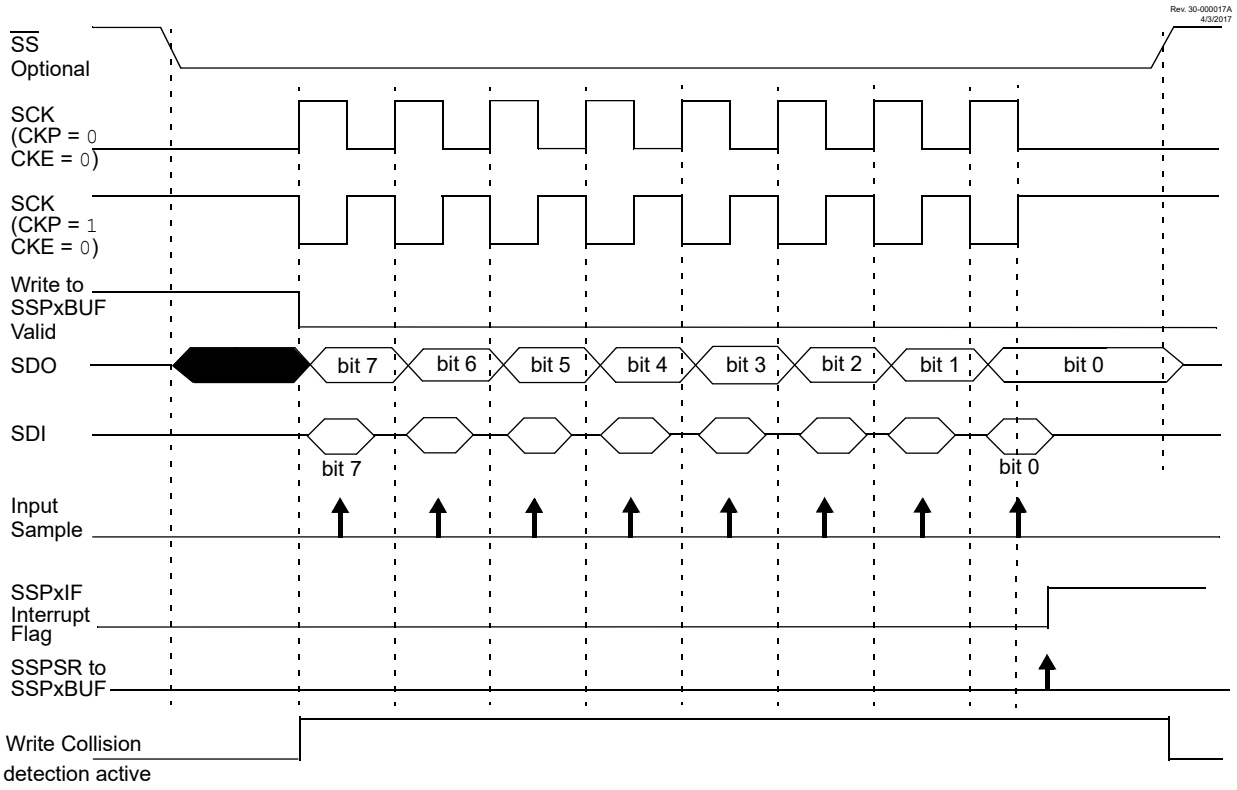
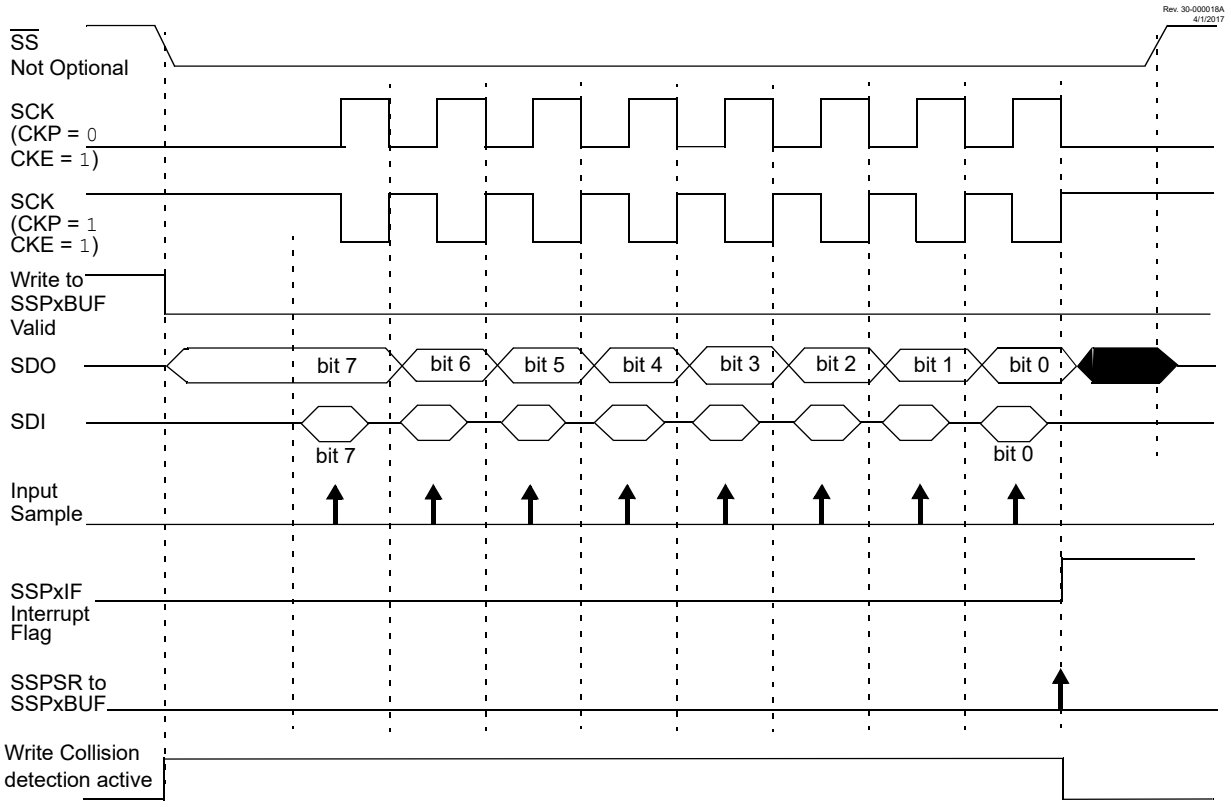


Figure 35-8. SPI Mode Waveform (Slave Mode with CKE = 1)



35.2.5 SPI Operation in Sleep Mode

In SPI Master mode, module clocks may be operating at a different speed than when in Full-Power mode; in the case of the Sleep mode, all clocks are halted.

Special care must be taken by the user when the MSSP clock is much faster than the system clock.

In Slave mode, when MSSP interrupts are enabled, after the master completes sending data, an MSSP interrupt will wake the controller from Sleep.

If an exit from Sleep mode is not desired, MSSP interrupts should be disabled.

In SPI Master mode, when the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all eight bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device.

35.3 I²C Mode Overview

The Inter-Integrated Circuit (I^2C) bus is a multi-master serial data communication bus. Devices communicate in a master/slave environment where the master devices initiate the communication. A

35.4.2 Arbitration

Each master device must monitor the bus for Start and Stop bits. If the device detects that the bus is busy, it cannot begin a new message until the bus returns to an Idle state.

However, two master devices may try to initiate a transmission on or about the same time. When this occurs, the process of arbitration begins. Each transmitter checks the level of the SDA data line and compares it to the level that it expects to find. The first transmitter to observe that the two levels do not match, loses arbitration, and must stop transmitting on the SDA line.

For example, if one transmitter holds the SDA line to a logical one (lets it float) and a second transmitter holds it to a logical zero (pulls it low), the result is that the SDA line will be low. The first transmitter then observes that the level of the line is different than expected and concludes that another transmitter is communicating.

The first transmitter to notice this difference is the one that loses arbitration and must stop driving the SDA line. If this transmitter is also a master device, it also must stop driving the SCL line. It then can monitor the lines for a Stop condition before trying to reissue its transmission. In the meantime, the other device that has not noticed any difference between the expected and actual levels on the SDA line continues with its original transmission. It can do so without any complications, because so far, the transmission appears exactly as expected with no other transmitter disturbing the message.

Slave Transmit mode can also be arbitrated, when a master addresses multiple slaves, but this is less common.

If two master devices are sending a message to two different slave devices at the address stage, the master sending the lower slave address always wins arbitration. When two master devices send messages to the same slave address, and addresses can sometimes refer to multiple slaves, the arbitration process must continue into the data stage.

Arbitration usually occurs very rarely, but it is a necessary process for proper multi-master support.

35.4.3 Byte Format

All communication in I^2C is done in 9-bit segments. A byte is sent from a master to a slave or vice-versa, followed by an Acknowledge bit sent back. After the eighth falling edge of the SCL line, the device outputting data on the SDA changes that pin to an input and reads in an acknowledge value on the next clock pulse.

The clock signal, SCL, is provided by the master. Data is valid to change while the SCL signal is low, and sampled on the rising edge of the clock. Changes on the SDA line while the SCL line is high define special conditions on the bus, explained below.

35.4.4 Definition of I^2C Terminology

There is language and terminology in the description of I^2C communication that have definitions specific to I^2C. That word usage is defined below and may be used in the rest of this document without explanation. This table was adapted from the Philips I^2C specification.

TERM	Description
Transmitter	The device which shifts data out onto the bus.
Receiver	The device which shifts data in from the bus.
Master	The device that initiates a transfer, generates clock signals and terminates a transfer.

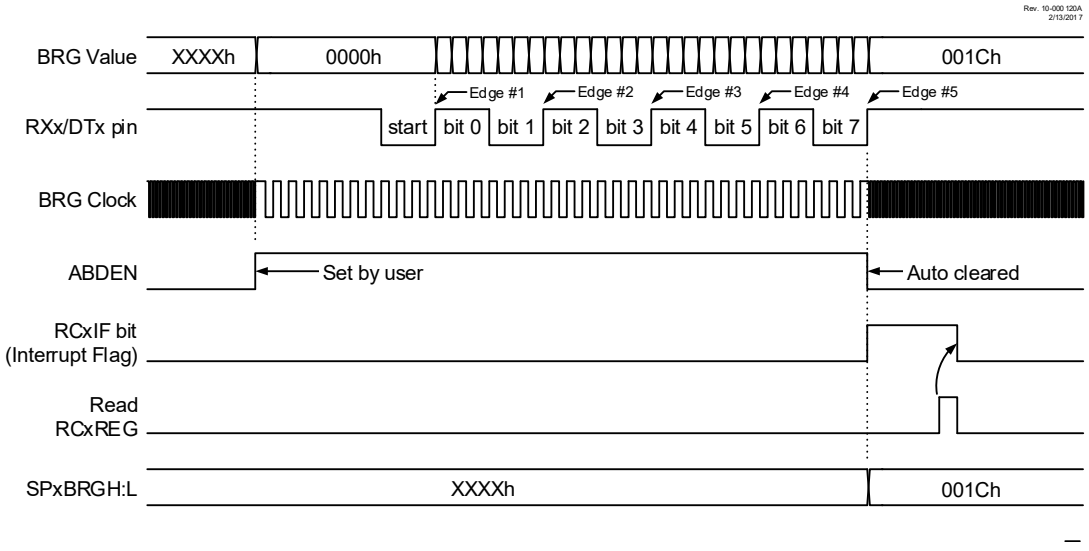
1. If the WUE bit is set with the ABDEN bit, auto-baud detection will occur on the byte following the Break character (see 36.2.3 Auto-Wake-up on Break).
2. It is up to the user to determine that the incoming character baud rate is within the range of the selected BRG clock source. Some combinations of oscillator frequency and EUSART baud rates are not possible.
3. During the auto-baud process, the auto-baud counter starts counting at one. Upon completion of the auto-baud sequence, to achieve maximum accuracy, subtract 1 from the SPxBRGH:SPxBRGL register pair.

Table 36-3. BRG Counter Clock Rates

BRG16	BRGH	BRG Base Clock	BRG ABD Clock
1	1	$F_{OSC}/4$	$F_{OSC}/32$
1	0	$F_{OSC}/16$	$F_{OSC}/128$
0	1	$F_{OSC}/16$	$F_{OSC}/128$
0	0	$F_{OSC}/64$	$F_{OSC}/512$

Note: During the ABD sequence, SPxBRGL and SPxBRGH registers are both used as a 16-bit counter, independent of the BRG16 setting.

Figure 36-6. Automatic Baud Rate Calibration



36.2.2 Auto-Baud Overflow

During the course of automatic baud detection, the ABDOVF bit of the BAUDxCON register will be set if the baud rate counter overflows before the fifth rising edge is detected on the RXx pin. The ABDOVF bit indicates that the counter has exceeded the maximum count that can fit in the 16 bits of the SPxBRGH:SPxBRGL register pair. After the ABDOVF bit has been set, the counter continues to count until the fifth rising edge is detected on the RXx pin. Upon detecting the fifth RX edge, the hardware will set the RCxIF interrupt flag and clear the ABDEN bit of the BAUDxCON register. The RCxIF flag can be subsequently cleared by reading the RCxREG register. The ABDOVF flag of the BAUDxCON register can be cleared by software directly.

Address	Name	Bit Pos.								
0x1E8E										
0x1E8F	PPSLOCK	7:0								PPSLOCKED
0x1E90	INTPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E91	T0CKIPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E92	T1CKIPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E93	T1GPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E94	T3CKIPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E95	T3GPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E96	T5CKIPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E97	T5GPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E98 ... 0x1E9B	Reserved									
0x1E9C	T2INPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E9D	T4INPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E9E	T6INPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1E9F ... 0x1EA0	Reserved									
0x1EA1	CCP1PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EA2	CCP2PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EA3	CCP3PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EA4	CCP4PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EA5	CCP5PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EA6 ... 0x1EA8	Reserved									
0x1EA9	SMT1WINPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EAA	SMT1SIGPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EAB	SMT2WINPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EAC	SMT2SIGPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EAD ... 0x1EB0	Reserved									
0x1EB1	CWG1PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EB2	CWG2PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EB3	CWG3PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EB4 ... 0x1EB7	Reserved									
0x1EB8	MDCARLPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EB9	MDCARHPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBA	MDSRCPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBB	CLCIN0PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBC	CLCIN1PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBD	CLCIN2PPS	7:0				PORT[1:0]		PIN[2:0]		