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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18456t-i-ss

1. Device Overview

This document contains device-specific information for the following devices:

• PIC16F18455	• PIC16LF18455
• PIC16F18456	• PIC16LF18456

1.1 New Core Features

1.1.1 XLP Technology

All of the devices in the PIC16(L)F184XX family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the secondary oscillator or the internal oscillator block, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-Fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- **Peripheral Module Disable:** Modules that are not being used in the code can be selectively disabled using the PMD module. This further reduces the power consumption.

1.1.2 Multiple Oscillator Options and Features

All of the devices in the PIC16(L)F184XX family offer several different oscillator options. The PIC16(L)F184XX family can be clocked from several different sources:

- HFINTOSC
  - 1-32 MHz precision digitally controlled internal oscillator
- LFINTOSC
  - 31 kHz internal oscillator
- EXTOSC
  - External clock (EC)
  - Low-power oscillator (LP)
  - Medium-power oscillator (XT)
  - High-power oscillator (HS)
- SOSC
  - Secondary oscillator circuit optimized for 32 kHz clock crystals
- A Phase Lock Loop (PLL) frequency multiplier (2x/4x) is available to the External Oscillator modes enabling clock speeds of up to 32 MHz
- Fail-Safe Clock Monitor: This option constantly monitors the main clock source against a reference signal provided by the LFINTOSC. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued operation or a safe application shutdown.

The CALLW instruction enables computed calls by combining PCLATH and W to form the destination address. A computed CALLW is accomplished by loading the W register with the desired address and executing CALLW. The PCL register is loaded with the value of W and PCH is loaded with PCLATH.

7.4.4 Branching

The branching instructions add an offset to the PC. This allows relocatable code and code that crosses page boundaries. There are two forms of branching, BRW and BRA. The PC will have incremented to fetch the next instruction in both cases. When using either branching instruction, a PCL memory boundary may be crossed.

If using BRW, load the W register with the desired unsigned address and execute BRW. The entire PC will be loaded with the address PC + 1 + W.

If using BRA, the entire PC will be loaded with PC + 1 + the signed value of the operand of the BRA instruction.

7.5 Stack

All devices have a 16-level by 15-bit wide hardware stack. The stack space is not part of either program or data space. The PC is PUSHed onto the stack when CALL or CALLW instructions are executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer if the STVREN Configuration bit is programmed to '0'. This means that after the stack has been PUSHed sixteen times, the seventeenth PUSH overwrites the value that was stored from the first PUSH. The eighteenth PUSH overwrites the second PUSH (and so on). The STKOVF and STKUNF flag bits will be set on an Overflow/Underflow, regardless of whether the Reset is enabled.

Important: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, CALLW, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

7.5.1 Accessing the Stack

The stack is accessible through the TOSH, TOSL and STKPTR registers. STKPTR is the current value of the Stack Pointer. TOSH:TOSL register pair points to the TOP of the stack. Both registers are read/writable. TOS is split into TOSH and TOSL due to the 15-bit size of the PC. To access the stack, adjust the value of STKPTR, which will position TOSH:TOSL, then read/write to TOSH:TOSL. STKPTR is five bits to allow detection of overflow and underflow.

Important: Care should be taken when modifying the STKPTR while interrupts are enabled.

During normal program operation, CALL, CALLW and interrupts will increment STKPTR while RETLW, RETURN, and RETFIE will decrement STKPTR. STKPTR can be monitored to obtain to value of stack

bit of the PIR0 register will be set when a valid edge appears on the INT pin. If the GIE and INTE bits are also set, the processor will redirect program execution to the interrupt vector.

10.5 Automatic Context Saving

Upon entering an interrupt, the return PC address is saved on the stack. Additionally, the following registers are automatically saved in the shadow registers:

- W register
- STATUS register (except for $\overline{TO}$ and $\overline{PD}$)
- BSR register
- FSR registers
- PCLATH register

Upon exiting the Interrupt Service Routine, these registers are automatically restored. Any modifications to these registers during the ISR will be lost. If modifications to any of these registers are desired, the corresponding shadow register should be modified and the value will be restored when exiting the ISR. The shadow registers are available in Bank 63 and are readable and writable. Depending on the user's application, other registers may also need to be saved.

Related Links

7.10 Register Definitions: Shadow Registers

12.7 Register Summary - WDT Control

Address	Name	Bit Pos.								
0x080C	WDTCON0	7:0			WDTPS[4:0]					SEN
0x080D	WDTCON1	7:0		WDTCS[2:0]				WINDOW[2:0]		
0x080E	WDTPSL	7:0	PSCNTL[7:0]							
0x080F	WDTPSH	7:0	PSCNTH[7:0]							
0x0810	WDTTMR	7:0	WDTTMR[4:0]					STATE	PSCNT[1:0]	

12.8 Register Definitions: Windowed Watchdog Timer Control

12.8.5 WDTTMR

Name: WDTTMR
Address: 0x810

WDT Timer Register (Read-Only)

Bit	7	6	5	4	3	2	1	0
	WDTTMR[4:0]					STATE	PSCNT[1:0]	
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 7:3 – WDTTMR[4:0] Watchdog Window Value bits

WINDOW	WDT Window State		Open Percent
	Closed	Open	
111	**N/A**	00000-11111	100
110	00000-00011	00100-11111	87.5
101	00000-00111	01000-11111	75
100	00000-01011	01100-11111	62.5
011	00000-01111	10000-11111	50
010	00000-10011	10100-11111	37.5
001	00000-10111	11000-11111	25
000	00000-11011	11100-11111	12.5

Bit 2 – STATE WDT Armed Status bit

Value	Description
1	WDT is armed
0	WDT is not armed

Bits 1:0 – PSCNT[1:0] Prescale Select Upper Byte bits(1)

Note:

1. The 18-bit WDT prescale value, PSCNT<17:0> includes the WDTPSL, WDTPSH and the lower bits of the WDTTMR registers. PSCNT<17:0> is intended for debug operations and should be read during normal operation.

an address outside the parameters listed in the following table, the NVMDATH: NVMDATL register pair is cleared, reading back '0's.

Table 13-2. NVMREG Access to Device Information Area, Device Configuration Area, User ID, Device ID, EEPROM, and Configuration Words (NVMREGS = 1)

Address	Function	Read Access	Write Access
8000h-8003h	User IDs	Yes	Yes
8005h-8006h	Device ID/Revision ID	Yes	No
8007h-800Bh	Configuration Words 1-5	Yes	Yes
8100h-82FFh	DIA and DCI	Yes	No
F000h-F0FFh	EEPROM	Yes	Yes

Example 13-5. Device ID Access

```
   ; This write routine assumes the following:
   ; 1. A full row of data are loaded, starting at the address in DATA_ADDR
   ; 2. Each word of data to be written is made up of two adjacent bytes in
DATA_ADDR,
   ; stored in little endian format
   ; 3. A valid starting address (the least significant bits = 00000) is
loaded in ADDRH:ADDRL
   ; 4. ADDRH and ADDRL are located in common RAM (locations 0x70 - 0x7F)
   ; 5. NVM interrupts are not taken into account

      BANKSEL    NVMADRH
      MOVF       ADDRH,W
      MOVWF      NVMADRH             ; Load initial address
      MOVF       ADDRL,W
      MOVWF      NVMADRL
      MOVLW      LOW DATA_ADDR       ; Load initial data address
      MOVWF      FSR0L
      MOVLW      HIGH DATA_ADDR
      MOVWF      FSR0H
      BCF        NVMCON1,NVMREGS     ; Set PFM as write location
      BSF        NVMCON1,WREN        ; Enable writes
      BSF        NVMCON1,LWLO        ; Load only write latches

   LOOP

      MOVIW      FSR0++
      MOVWF      NVMDATL             ; Load first data byte
      MOVIW      FSR0++
      MOVWF      NVMDATH             ; Load second data byte
      CALL       UNLOCK_SEQ          ; If not, go load latch
      INCF       NVMADRL,F           ; Increment address
      MOVF       NVMADRL,W
      XORLW      0x1F                ; Check if lower bits of address are 00000
      ANDLW      0x1F                ; and if on last of 32 addresses
      BTFSC      STATUS,Z            ; Last of 32 words?
      GOTO       START_WRITE         ; If so, go write latches into memory

      GOTO       LOOP


   START_WRITE

      BCF        NVMCON1,LWLO        ; Latch writes complete, now write memory
      CALL       UNLOCK_SEQ          ; Perform required unlock sequence
      BCF        NVMCON1,LWLO        ; Disable writes

   UNLOCK_SEQ

      MOVLW      55h
```

14.7.3 PORTC

Name: PORTC
Address: 0x00E

PORTC Register

Bit	7	6	5	4	3	2	1	0
	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 0, 1, 2, 3, 4, 5, 6, 7 – RCn Port I/O Value bits
Reset States: POR/BOR = xxxxxxxx
All Other Resets = uuuuuuuu

Value	Description
1	Port pin is ≥ V_{IH}
0	Port pin is ≤ V_{IL}

Note: Writes to PORTC are actually written to the corresponding LATC register. Reads from PORTC register return actual I/O pin values.

14.7.11 ANSELA

Name: ANSELA
Address: 0x1F38

Analog Select Register

Bit	7	6	5	4	3	2	1	0
	ANSELA7	ANSELA6	ANSELA5	ANSELA4	ANSELA3	ANSELA2	ANSELA1	ANSELA0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 0, 1, 2, 3, 4, 5, 6, 7 – ANSELAn Analog Select on Pins RA<7:0>

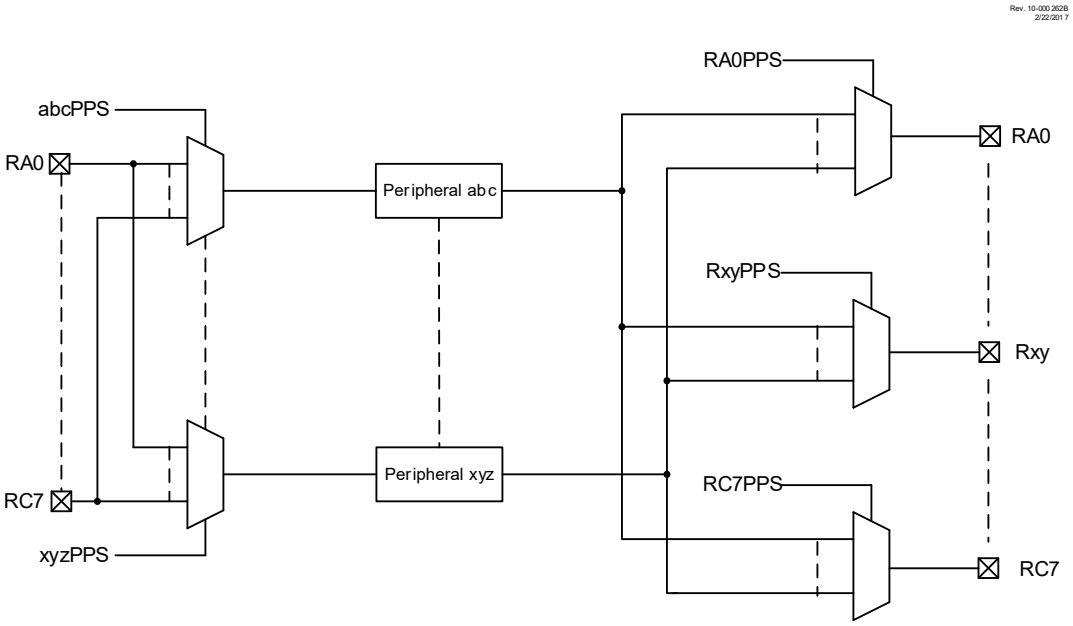
Value	Description
1	Digital Input buffers are disabled
0	ST and TTL input buffers are enabled

15. (PPS) Peripheral Pin Select Module

The Peripheral Pin Select (PPS) module connects peripheral inputs and outputs to the device I/O pins. Only digital signals are included in the selections.

All analog inputs and outputs remain fixed to their assigned pins. Input and output selections are independent as shown in the figure below.

Figure 15-1. Simplified PPS Block Diagram



15.1 PPS Inputs

Each peripheral has an xxxPPS register with which the input pin to the peripheral is selected. Not all ports are available for input as shown in the following table.

Multiple peripherals can operate from the same source simultaneously. Port reads always return the pin level regardless of peripheral PPS selection. If a pin also has analog functions associated, the ANSEL bit for that pin must be cleared to enable the digital input buffer.

Important: The notation “xxx” in the generic register name is a place holder for the peripheral identifier. For example, xxx = INT for the INTPPS register.

Table 15-1. PPS Input Signal Routing Options

Input Signal Name	Input Register Name	Default Location at POR	Reset Value (xxxPPS<4:0>)	PORT From Which Input Is Available		
INT0	INT0PPS	RB0	0 1000	A	B	—
T0CKI	T0CKIPPS	RA4	0 0100	A	B	—

Address	Name	Bit Pos.								
0x1EBD	CLCIN2PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBE	CLCIN3PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBF ... 0x1EC2	Reserved									
0x1EC3	ADACTPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC4	Reserved									
0x1EC5	SSP1CLKPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC6	SSP1DATPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC7	SSP1SSPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC8	SSP2CLKPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC9	SSP2DATPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECA	SSP2SSPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECB	RX1PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECC	CK1PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECD	RX2PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECE	CK2PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECF ... 0x1F0F	Reserved									
0x1F10	RA0PPS	7:0			PPS[5:0]					
0x1F11	RA1PPS	7:0			PPS[5:0]					
0x1F12	RA2PPS	7:0			PPS[5:0]					
0x1F13	RA3PPS	7:0			PPS[5:0]					
0x1F14	RA4PPS	7:0			PPS[5:0]					
0x1F15	RA5PPS	7:0			PPS[5:0]					
0x1F16	RA6PPS	7:0			PPS[5:0]					
0x1F17	RA7PPS	7:0			PPS[5:0]					
0x1F18	RB0PPS	7:0			PPS[5:0]					
0x1F19	RB1PPS	7:0			PPS[5:0]					
0x1F1A	RB2PPS	7:0			PPS[5:0]					
0x1F1B	RB3PPS	7:0			PPS[5:0]					
0x1F1C	RB4PPS	7:0			PPS[5:0]					
0x1F1D	RB5PPS	7:0			PPS[5:0]					
0x1F1E	RB6PPS	7:0			PPS[5:0]					
0x1F1F	RB7PPS	7:0			PPS[5:0]					
0x1F20	RC0PPS	7:0			PPS[5:0]					
0x1F21	RC1PPS	7:0			PPS[5:0]					
0x1F22	RC2PPS	7:0			PPS[5:0]					
0x1F23	RC3PPS	7:0			PPS[5:0]					
0x1F24	RC4PPS	7:0			PPS[5:0]					
0x1F25	RC5PPS	7:0			PPS[5:0]					
0x1F26	RC6PPS	7:0			PPS[5:0]					
0x1F27	RC7PPS	7:0			PPS[5:0]					

17.5 Register Summary - Interrupt-on-Change

Address	Name	Bit Pos.								
0x1F3D	IOCAP	7:0	IOCAP7	IOCAP6	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0
0x1F3E	IOCAN	7:0	IOCAN7	IOCAN6	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0
0x1F3F	IOCAF	7:0	IOCAF7	IOCAF6	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0
0x1F40 ... 0x1F47	Reserved									
0x1F48	IOCBP	7:0	IOCBP7	IOCBP6	IOCBP5	IOCBP4	IOCBP3	IOCBP2	IOCBP1	IOCBP0
0x1F49	IOCBN	7:0	IOCBN7	IOCBN6	IOCBN5	IOCBN4	IOCBN3	IOCBN2	IOCBN1	IOCBN0
0x1F4A	IOCBF	7:0	IOCBF7	IOCBF6	IOCBF5	IOCBF4	IOCBF3	IOCBF2	IOCBF1	IOCBF0
0x1F4B ... 0x1F52	Reserved									
0x1F53	IOCCP	7:0	IOCCP7	IOCCP6	IOCCP5	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0
0x1F54	IOCCN	7:0	IOCCN7	IOCCN6	IOCCN5	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0
0x1F55	IOCCF	7:0	IOCCF7	IOCCF6	IOCCF5	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0
0x1F56 ... 0x1F68	Reserved									
0x1F69	IOCEP	7:0					IOCEP3			
0x1F6A	IOCEN	7:0					IOCEN3			
0x1F6B	IOCEF	7:0					IOCEF3			

17.6 Register Definitions: Interrupt-on-Change Control

26.14.4 TMRxGATE

Name: TMRxGATE
Address: 0x210,0x216,0x21C

Timer Gate Source Selection Register

Bit	7	6	5	4	3	2	1	0
				GSS[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – GSS[4:0] Timer Gate Source Selection bits
Refer to the gate source selection table.

Reset States: POR/BOR = 00000
All Other Resets = uuuuu

31.3 Start-up Considerations

The application hardware must use the proper external pull-up and/or pull-down resistors on the CWG output pins. This is required because all I/O pins are forced to high-impedance at Reset.

The polarity control bits (POLy) allow the user to choose whether the output signals are active-high or active-low.

31.4 Clock Source

The clock source is used to drive the dead-band timing circuits. The CWG module allows the following clock sources to be selected:

- F_{OSC} (system clock)
- HFINTOSC

When the HFINTOSC is selected, the HFINTOSC will be kept running during Sleep. Therefore, CWG modes requiring dead band can operate in Sleep, provided that the CWG data input is also active during Sleep. The clock sources are selected using the CS bit. The system clock F_{OSC}, is disabled in Sleep and thus dead-band control cannot be used.

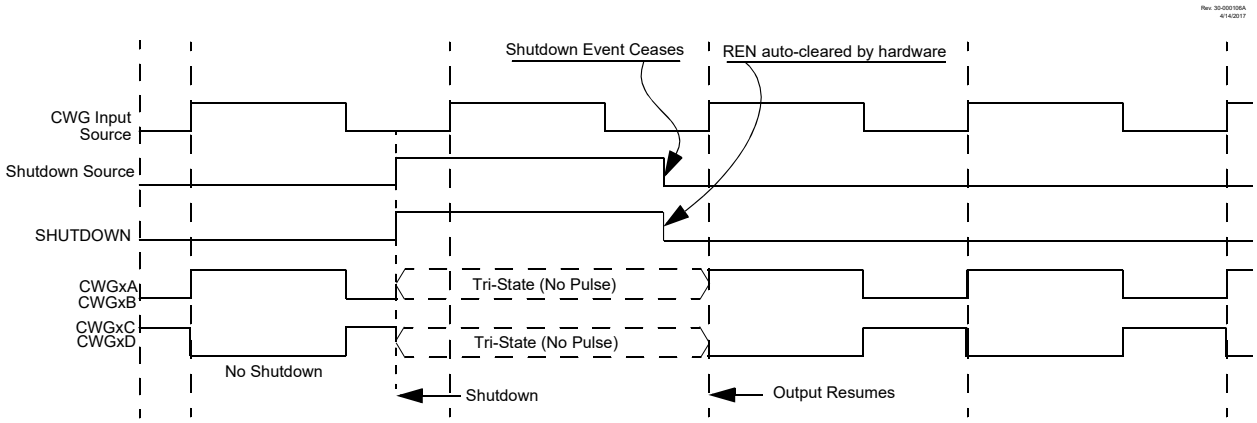
31.5 Selectable Input Sources

The CWG generates the output waveforms from the input sources which are selected with the ISM bits as shown below.

Table 31-1. CWG Data Input Sources

ISM	Data Source
1111	CCP5_out
1110	CLC4_out
1101	CLC3_out
1100	CLC2_out
1011	CLC1_out
1010	DSM1_out
1001	C2_out
1000	C1_out
0111	NCO1_out
0110	PWM7_out
0101	PWM6_out
0100	CCP4_out
0011	CCP3_out
0010	CCP2_out

Figure 31-16. SHUTDOWN FUNCTIONALITY, AUTO-RESTART ENABLED (REN = 1, LSAC = 01, LSBD = 01)



31.12 Operation During Sleep

The CWG module operates independently from the system clock and will continue to run during Sleep, provided that the clock and input sources selected remain active.

The HFINTOSC remains active during Sleep when all the following conditions are met:

- CWG module is enabled
- Input source is active
- HFINTOSC is selected as the clock source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as the system clock and the CWG clock source, when the CWG is enabled and the input source is active, then the CPU will go idle during Sleep, but the HFINTOSC will remain active and the CWG will continue to operate. This will have a direct effect on the Sleep mode current.

31.13 Configuring the CWG

1. Ensure that the TRIS control bits corresponding to CWG outputs are set so that all are configured as inputs, ensuring that the outputs are inactive during setup. External hardware should ensure that pin levels are held to safe levels.
2. Clear the EN bit, if not already cleared.
3. Configure the MODE bits to set the output operating mode.
4. Configure the POLy bits to set the output polarities.
5. Configure the ISM bits to select the data input source.
6. If a steering mode is selected, configure the STRy bits to select the desired output on the CWG outputs.
7. Configure the LSBD and LSAC bits to select the auto-shutdown output override states (this is necessary even if not using auto-shutdown because start-up will be from a shutdown state).
8. If auto-restart is desired, set the REN bit.
9. If auto-shutdown is desired, configure the ASyE bits to select the shutdown source.
10. Set the desired rising and falling dead-band times with the CWGxDBR and CWGxDBF registers.

33.8.6 CLCxSEL3

Name: CLCxSEL3
Address: 0x1E15,0x1E1F,0x1E29,0x1E33

Generic CLCx Data 4 Select Register

Bit	7	6	5	4	3	2	1	0
			D4S[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			x	x	x	x	x	x

Bits 5:0 – D4S[5:0]
CLCx Data4 Input Selection bits
Reset States: POR/BOR = xxxxxx
All Other Resets = uuuuuu

Value	Description
n	Refer to CLC Input Sources for input selections

35.9.1 SSPxSTAT

Name: SSPxSTAT
Address: 0x18F,0x199

MSSP Status Register

Bit	7	6	5	4	3	2	1	0
	SMP	CKE	$\overline{D/A}$	P	S	$\overline{R/W}$	UA	BF
Access	R/W	R/W	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 7 – SMP Slew Rate Control bit

Value	Mode	Description
1	SPI Master	Input data is sampled at the end of data output time
0	SPI Master	Input data is sampled at the middle of data output time
0	SPI Slave	Keep this bit cleared in SPI Slave mode
1	I^2C	Slew rate control is disabled for Standard Speed mode (100 kHz and 1 MHz)
0	I^2C	Slew rate control is enabled for High-Speed mode (400 kHz)

Bit 6 – CKE

SPI: Clock select bit(4) I^2C: SMBus Select bit

Value	Mode	Description
1	SPI	Transmit occurs on the transition from active to Idle clock state
0	SPI	Transmit occurs on the transition from Idle to active clock state
1	I^2C	Enables SMBus-specific inputs
0	I^2C	Disables SMBus-specific inputs

Bit 5 – D/$\overline{A}$
Data/$\overline{Address}$ bit

Value	Mode	Description
x	SPI or I^2C Master	Reserved
1	I^2C Slave	Indicates that the last byte received or transmitted was data
0	I^2C Slave	Indicates that the last byte received or transmitted was address

Bit 4 – P
Stop bit(1)

Value	Mode	Description
x	SPI	Reserved
1	I^2C	Stop bit was detected last
0	I^2C	Stop bit was not detected last

Bit 3 – S
Start bit(1)

Figure 37-9. Windowed Measurement Mode, Repeat Acquisition Timing Diagram

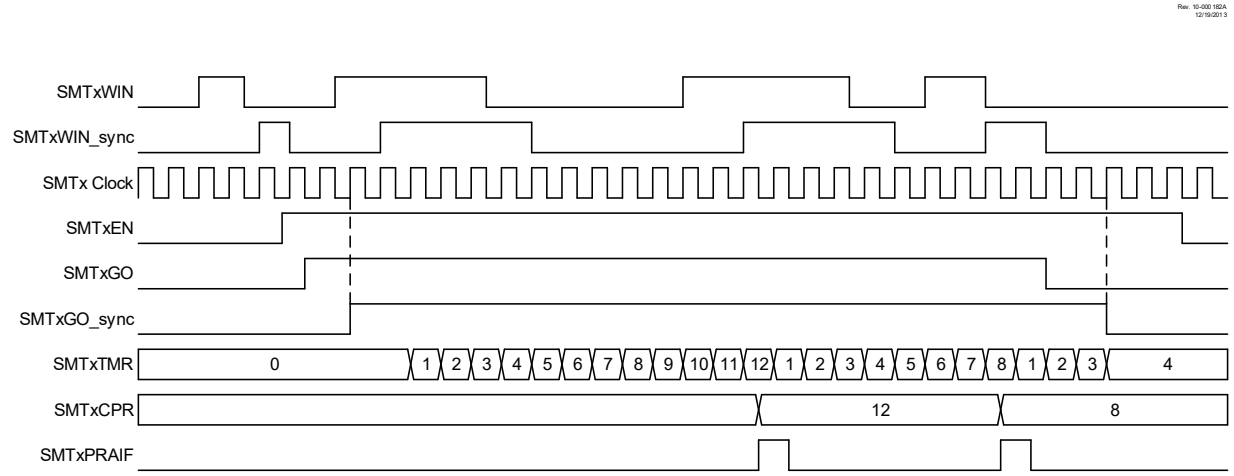
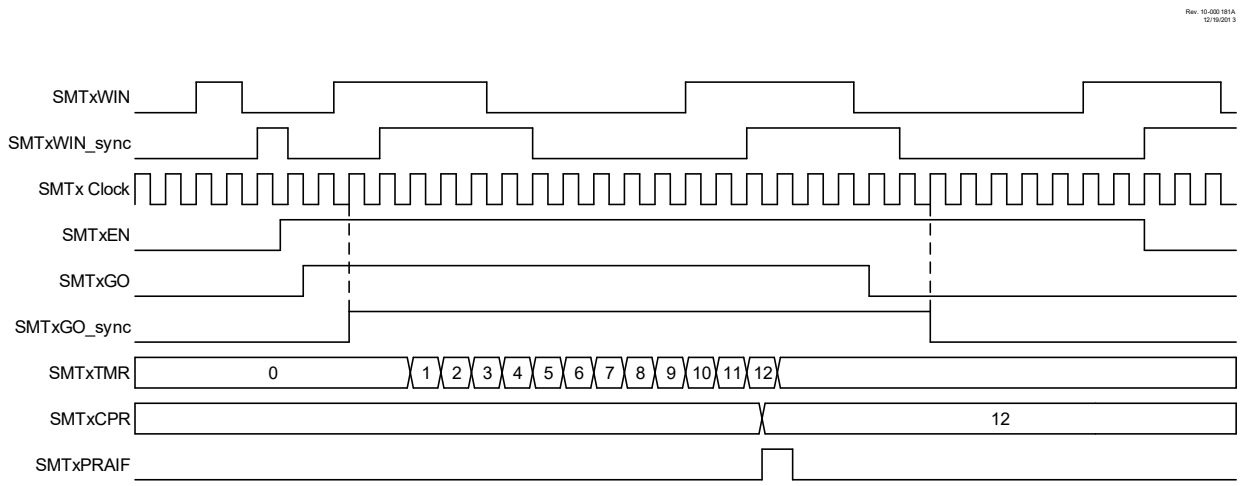


Figure 37-10. Windowed Measurement Mode, Single Acquisition Timing Diagram



37.1.6.6 Gated Window Measurement Mode

This mode measures the duty cycle of the signal input over a known input window. It does so by incrementing the timer on each pulse of the clock signal while the signal input is high, updating the SMTxCPR register and resetting the timer on every rising edge of the window input after the first. See figures below.

Figure 37-11. Gated Windowed Measurement Mode, Repeat Acquisition Timing Diagram

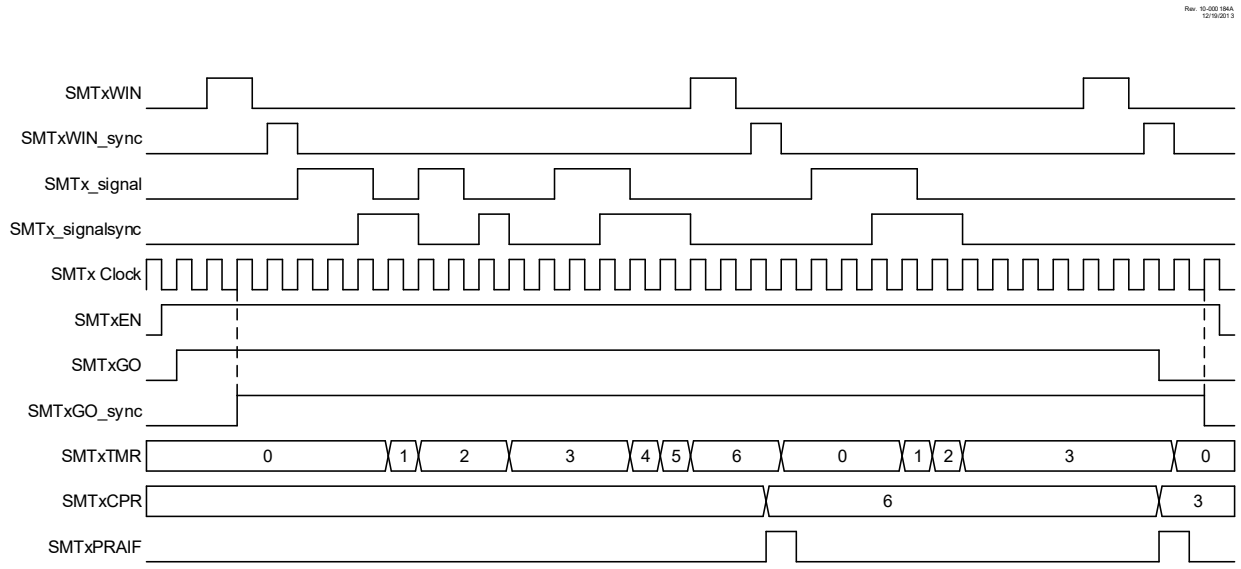
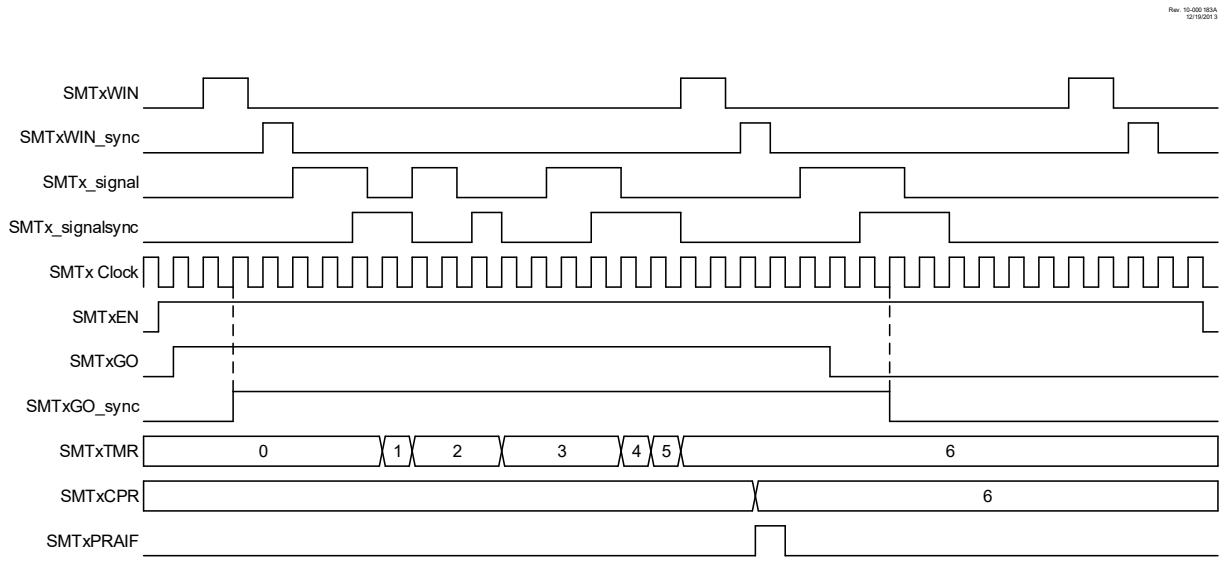


Figure 37-12. Gated Windowed Measurement Mode, Single Acquisition Timing Diagram

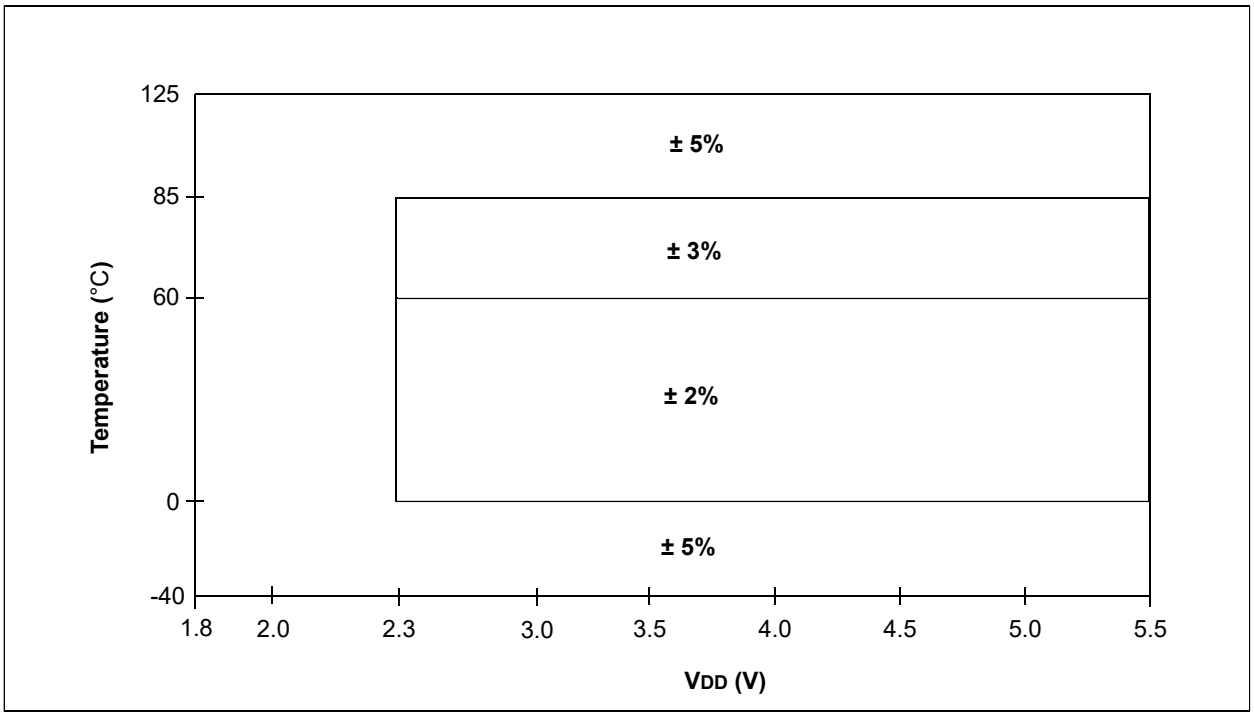


37.1.6.7 Time of Flight Measurement Mode

This mode measures the time interval between a rising edge on the window input and a rising edge on the signal input, beginning to increment the timer upon observing a rising edge on the window input, while updating the SMTxCPR register and resetting the timer upon observing a rising edge on the signal input. In the event of two rising edges of the window signal without a signal rising edge, it will update the SMTxCPW register with the current value of the timer and reset the timer value. See figures below.

WSEL<4:0>	SMT1 Window Source	SMT2 Window Source
00011	SOSC	SOSC
00010	MFINTOSC (31.25kHz)	MFINTOSC (31.25kHz)
00001	LFINTOSC (31.25kHz)	LFINTOSC (31.25kHz)
00000	Pin Selected by SMT1WINPPS	Pin Selected by SMT1WINPPS

Figure 42-6. Precision Calibrated HFINTOSC Frequency Accuracy Over Device V_{DD} and Temperature



42.4.3 PLL Specifications

Table 42-9.

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ. †**	**Max.**	**Units**	**Conditions**
PLL01	F_{PLLIN}	PLL Input Frequency Range	4	—	16	MHz	
PLL02	F_{PLLOUT}	PLL Output Frequency Range	16	—	32	MHz	(**Note 1**)
PLL03	F_{PLLST}	PLL Lock Time from Start-up	—	200	—	µs	
PLL04	F_{PLLJIT}	PLL Output Frequency Stability (Jitter)	-0.25	—	0.25	%	

* - These parameters are characterized but not tested.

† - Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:

1. The output frequency of the PLL must meet the F_{OSC} requirements listed in Parameter D002.