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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ST10
Core Size	16-Bit
Speed	40MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	144-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f273m-4q3

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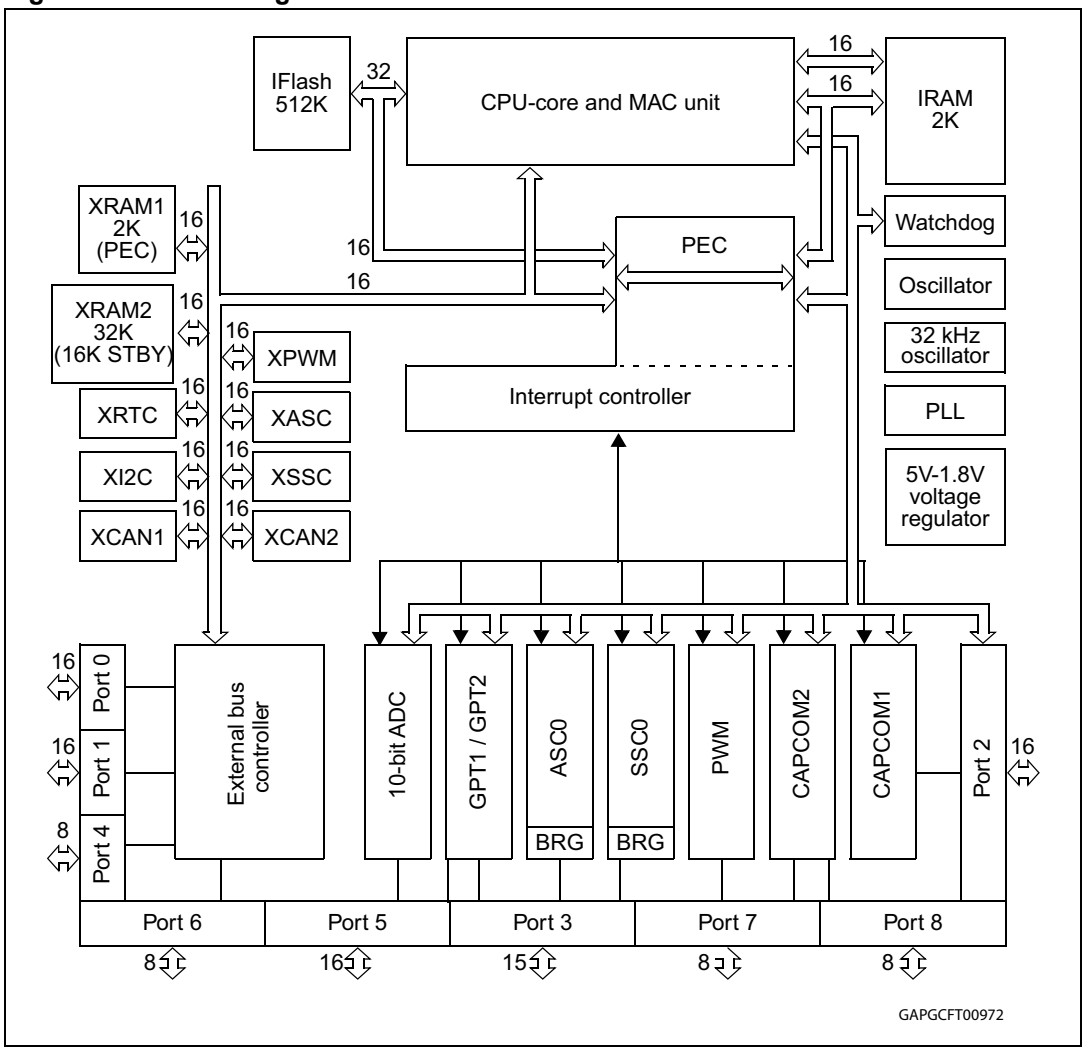
Table 1. Pin description

Symbol	Pin	Type	Function		
P6.0 - P6.7	1 - 8	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 6 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 6 is selectable (TTL or CMOS). The following Port 6 pins have alternate functions:		
	1	O	P6.0	$\overline{CS0}$	Chip select 0 output
	...	...	...	...	...
	5	O	P6.4	$\overline{CS4}$	Chip select 4 output
	6	I	P6.5	$\overline{HOLD}$	External master hold request input
		I/O		SCLK1	SSC1: master clock output / slave clock input
	7	O	P6.6	$\overline{HLDA}$	Hold acknowledge output
		I/O		MTSR1	SSC1: master-transmitter / slave-receiver O/I
	8	O	P6.7	$\overline{BREQ}$	Bus request output
		I/O		MRST1	SSC1: master-receiver / slave-transmitter I/O
P8.0 - P8.7	9-16	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 8 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or CMOS). The following Port 8 pins have alternate functions:		
	9	I/O	P8.0	CC16IO	CAPCOM2: CC16 capture input / compare output
		O		XPWM0	PWM1: channel 0 output
	...	...	...	...	...
	12	I/O	P8.3	CC19IO	CAPCOM2: CC19 capture input / compare output
		O		XPWM0	PWM1: channel 3 output
	13	I/O	P8.4	CC20IO	CAPCOM2: CC20 capture input / compare output
	14	I/O	P8.5	CC21IO	CAPCOM2: CC21 capture input / compare output
	15	I/O	P8.6	CC22IO	CAPCOM2: CC22 capture input / compare output
		I/O		RxD1	ASC1: Data input (Asynchronous) or I/O (Synchronous)
	16	I/O	P8.7	CC23IO	CAPCOM2: CC23 capture input / compare output
		O		TxD1	ASC1: Clock / Data output (Asynchronous/Synchronous)

3 Functional description

The architecture of the ST10F273M combines advantages of both RISC and CISC processors and an advanced peripheral subsystem. The block diagram gives an overview of the different on-chip components and the high bandwidth internal bus structure of the ST10F273M.

Figure 3. Block diagram



5.4.4 Flash control register 1 high (FCR1H)

The Flash Control Register 1 High (FCR1H), together with Flash Control Register 1 Low (FCR1L), is used to select the sectors to erase or during any write operation, to monitor the status of each sector and bank.

FCR1H (0x0E 0006) FCR Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						DB1S	B0S	Reserved						B0F11 /B1F1	B0F10 /B1F0
-						RS	RS	-						RS	RS

Table 10. FCR1H register description

Bit	Name	Function
15:10	-	Reserved. These bits must be kept to their default value (0).
9	DB1S	Dummy Bank1 status This is a replication of B0S bit. In order to maintain compatibility with the ST10F273E where operations on the last 2 sectors were flagged in this position.
8	B0S	Bank0 status During any erase operation, this bit is automatically modified and gives the status of the Bank 0. The meaning of B0S bit is given in the next *Table 11: Bank (BxS) and sectors (BxFy) status bits meaning*. This bit is automatically reset at the end of a erase operation if no errors are detected.
7:2	-	Reserved. These bits must be kept to their default value (0).
1:0	B0F10/B1F0 B0F11/B1F1	Bank0 IFlash sector 11:10 status / Bank1 IFlash sector 1:0 status These bits must be set during a Sector Erase operation to select the last 2 sectors of Bank0. Besides, during any erase operation, these bits are automatically set and give the status of the last two sectors of Bank0 (B0F11-B0F10). The meaning of B0Fy bit for Sector y of Bank 0 is given by the next *Table 11: Bank (BxS) and sectors (BxFy) status bits meaning*. These bits are automatically reset at the end of a Write operation if no errors are detected. *Note: These bits can also be seen as selecting the two sectors of Bank1 for compatibility with the ST10F273E.*

Table 11. Bank (BxS) and sectors (BxFy) status bits meaning

Operation		BxS = 1 meaning	BxFy = 1 meaning
Erase	Suspend		
1	-	Erase error	Erase error in sector y
0	1	Erase suspended in bank x	Erase suspended in sector y of bank x
0	0	Don't care	Don't care

10 Capture / compare (CAPCOM) units

The ST10F273M has two 16-channel CAPCOM units which support generation and control of timing sequences on up to 32 channels with a maximum resolution of 200ns at 40 MHz CPU clock.

The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), digital to analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2.

This provides a wide range of variation for the timer period and resolution and allows precise adjustments to application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Each of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare functions. Each of the 32 registers has one associated port pin which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (captured) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated.

Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture / compare register, specific actions will be taken based on the selected compare mode.

The input frequencies f_{Tx}, for the timer input selector Tx, are determined as a function of the CPU clocks. The timer input frequencies, resolution and periods which result from the selected prescaler option in TxI when using a 40 MHz CPU clock are listed in *Table 34*.

The numbers for the timer periods are based on a reload value of 0000h. Note that some numbers may be rounded off to three significant figures.

Table 33. Compare modes

Compare modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated

17 CAN modules

The two integrated CAN modules (CAN1 and CAN2) are identical and handle the completely autonomous transmission and reception of CAN frames according to the CAN specification V2.0 part B (active). It is based on the C-CAN specification.

Each on-chip CAN module can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Because of duplication of the CAN controllers, the following adjustments are to be considered:

- Same internal register addresses of both CAN controllers, but with base addresses differing in address bit A8; separate chip select for each CAN module. Refer to *Section 4: Memory organization on page 21*.
- The CAN1 transmit line (CAN1_TxD) is the alternate function of the Port P4.6 pin and the receive line (CAN1_RxD) is the alternate function of the Port P4.5 pin.
- The CAN2 transmit line (CAN2_TxD) is the alternate function of the Port P4.7 pin and the receive line (CAN2_RxD) is the alternate function of the Port P4.4 pin.
- Interrupt request lines of the CAN1 and CAN2 modules are connected to the XBUS interrupt lines together with other X-Peripherals sharing the four vectors.
- The CAN modules must be selected with corresponding CANxEN bit of XPERCON register before the bit XPEN of SYSCON register is set.
- The reset default configuration is: CAN1 enabled, CAN2 disabled.

Note: If one or both CAN modules is used, Port 4 cannot be programmed to output all eight segment address lines. Thus, only four segment address lines can be used, reducing the external memory space to 5 Mbytes (1 Mbyte per $\overline{CS}$ line).

17.1 Configuration support

It is possible that both CAN controllers are working on the same CAN bus, supporting together up to 64 message objects. In this configuration, both receive signals and both transmit signals are linked together when using the same CAN transceiver. This configuration is especially supported by providing open drain outputs for the CAN1_Txd and CAN2_TxD signals. The open drain function is controlled with the ODP4 register for port P4: in this way it is possible to connect together P4.4 with P4.5 (receive lines) and P4.6 with P4.7 (transmit lines configured to be configured as Open-Drain).

The user may also map internally both CAN modules on the same pins P4.5 and P4.6. In this way, P4.4 and P4.7 can be used either as general purpose I/O lines, or used for I^2C interface. This is possible by setting bit CANPAR of the XMISC register. To access this register it is necessary to set bit XMISCEN of the XPERCON register and bit XPEN of the SYSCON register.

17.2 CAN bus configurations

Depending on the application, CAN bus configuration may be one single bus with a single or multiple interfaces or a multiple bus with a single or multiple interfaces. The ST10F273M can support both configurations.

20.2 Asynchronous reset

An asynchronous reset is triggered when $\overline{\text{RSTIN}}$ pin is pulled low while RPD pin is at low level. Then the ST10F273M is immediately (after the input filter delay) forced in reset default state. It pulls low $\overline{\text{RSTOUT}}$ pin, it cancels pending internal hold states if any, it aborts all internal/external bus cycles, it switches buses (data, address and control signals) and I/O pin drivers to high-impedance, it pulls high Port0 pins.

Note: If an asynchronous reset occurs during a read or write phase in internal memories, the content of the memory itself could be corrupted: To avoid this, synchronous reset usage is strongly recommended.

Power-on reset

The asynchronous reset must be used during the power-on of the device. Depending on crystal or resonator frequency, the on-chip oscillator needs about 1ms to 10ms to stabilize (refer to *Section 24: Electrical characteristics*), with an already stable V_{DD}. The logic of the ST10F273M does not need a stabilized clock signal to detect an asynchronous reset, so it is suitable for power-on conditions. To ensure a proper reset sequence, the $\overline{\text{RSTIN}}$ pin and the RPD pin must be held at low level until the device clock signal is stabilized and the system configuration value on Port0 is settled.

At power-on it is important to respect some additional constraints introduced by the start-up phase of the different embedded modules.

In particular the on-chip voltage regulator needs at least 1ms to stabilize the internal 1.8V for the core logic: this time is computed from when the external reference (V_{DD}) becomes stable (inside specification range, that is at least 4.5V). This is a constraint for the application hardware (external voltage regulator): the $\overline{\text{RSTIN}}$ pin assertion shall be extended to guarantee the voltage regulator stabilization.

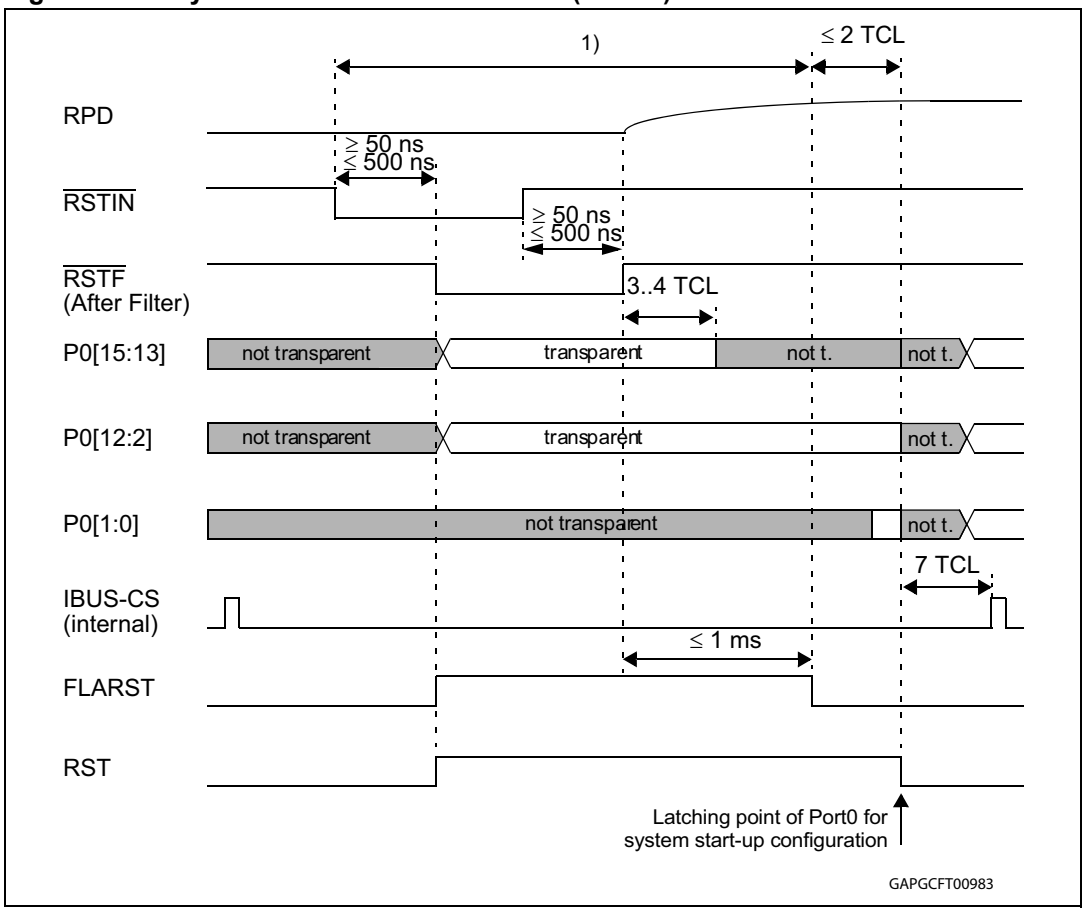
A second constraint is imposed by the embedded Flash. When booting from internal memory, starting from $\overline{\text{RSTIN}}$ releasing, it needs a maximum of 1ms for its initialization: before that, the internal reset (RST signal) is not released, so the CPU does not start code execution in internal memory.

Note: This is not true if external memory is used (pin $\overline{EA}$ held low during reset phase). In this case, once $\overline{RSTIN}$ pin is released, and after few CPU clock (Filter delay plus 3...8 TCL), the internal reset signal RST is released as well, so the code execution can start immediately after. Obviously, an eventual access to the data in internal Flash is forbidden before its initialization phase is completed: an eventual access during starting phase will return FFFFh (just at the beginning), while later 009Bh (an illegal opcode trap can be generated).

At power-on, the $\overline{\text{RSTIN}}$ pin shall be tied low for a minimum time that includes also the start-up time of the main oscillator (t_{STUP} = 1ms for resonator, 10ms for crystal) and PLL synchronization time (t_{PSUP} = 200µs): this means that if the internal Flash is used, the $\overline{\text{RSTIN}}$ pin could be released before the main oscillator and PLL are stable to recover some time in the start-up phase (Flash initialization only needs stable V_{18}, but does not need stable system clock since an internal dedicated oscillator is used).

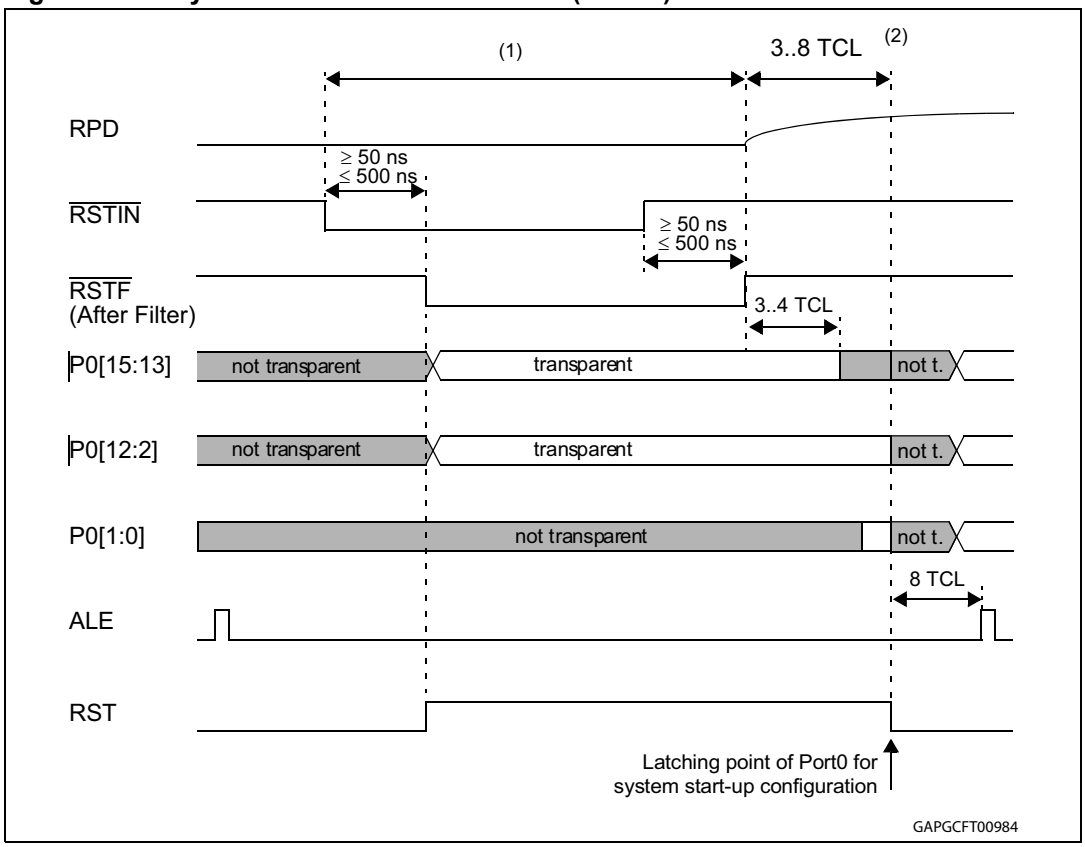
Warning: It is recommended to provide the external hardware with a current limitation circuitry. This is necessary to avoid permanent damage of the device during the power-on transient, when the capacitance on V_{18} pin is charged. For the on-chip voltage regulator functionality 10nF is sufficient:

Figure 20. Asynchronous hardware RESET ($\overline{EA}$ = 1)



1. Longer than Port0 settling time + PLL synchronization (if needed, that is P0(15:13) changed).
Longer than 500ns to take into account of Input Filter on RSTIN pin.

Figure 21. Asynchronous hardware RESET ($\overline{EA}$ = 0)



1. Longer than Port0 settling time + PLL synchronization (if needed, that is P0(15:13) changed). Longer than 500ns to take into account of Input Filter on RSTIN pin.
2. 3 to 8 TCL depending on clock source selection.

Exit from asynchronous reset state

When the $\overline{RSTIN}$ pin is pulled high, the device restarts: As already mentioned, if internal Flash is used, the restarting occurs after the embedded Flash initialization routine is completed. The system configuration is latched from Port0: ALE, $\overline{RD}$ and $\overline{WR}$/$\overline{WRL}$ pins are driven to their inactive level. The ST10F273M starts program execution from memory location 00'0000h in code segment 0. This starting location will typically point to the general initialization routine. The timings of asynchronous Hardware Reset sequence are summarized in *Figure 20* and *Figure 21*.

20.3 Synchronous reset (warm reset)

A synchronous reset is triggered when $\overline{RSTIN}$ pin is pulled low while RPD pin is at high level. In order to properly activate the internal reset logic of the device, the $\overline{RSTIN}$ pin must be held low, at least, during 4 TCL (two periods of CPU clock): refer also to *Section 20.1* for details on minimum reset pulse duration. The I/O pins are set to high impedance and $\overline{RSTOUT}$ pin is driven low. After $\overline{RSTIN}$ level is detected, a short duration of a maximum of 12 TCL (six periods of CPU clock) elapses, during which pending internal hold states are cancelled and the current internal access cycle if any is completed. External bus cycle is aborted. The internal pull-down of $\overline{RSTIN}$ pin is activated if bit BDRSTEN of SYSCON

Table 43. Reset event (continued)

Event	RPD	$\overline{EA}$	Bidir	Synch. Asynch.	RSTIN		WDTCON flags				
					Min	Max	PONR	LHWR	SHWR	SWR	WDTR
Software Reset(2)	x	0	N	Synch.	Not activated		0	0	0	1	0
	x	0	N	Synch.	Not activated		0	0	0	1	0
	0	1	Y	Synch.	Not activated		0	0	0	1	0
	1	1	Y	Synch.	Activated by internal logic for 1024 TCL		0	0	0	1	0
Watchdog Reset(2)	x	0	N	Synch.	Not activated		0	0	0	1	1
	x	0	N	Synch.	Not activated		0	0	0	1	1
	0	1	Y	Synch.	Not activated		0	0	0	1	1
	1	1	Y	Synch.	Activated by internal logic for 1024 TCL		0	0	0	1	1

1. It can degenerate into a Long Hardware Reset and consequently differently flagged (see *Section 20.3* for details).
2. When Bidirectional is active (and with RPD = 0), it can be followed by a Short Hardware Reset and consequently differently flagged (see *Section 20.6* for details).

The start-up configurations and some system features are selected on reset sequences as described in *Table 44* and *Figure 36*.

Table 44 describes the system configuration latched on PORT0 in the six different reset modes. *Figure 36* summarizes the state of bits of PORT0 latched in RP0H, SYSCON, BUSCON0 registers.

Table 44. PORT0 latched configuration for the different reset events

X: Pin is sampled -: Pin is not sampled	PORT0															
	Clock options			Segment address lines		Chip selects		WR configuration	Bus type		Reserved	BSL	Reserved	Reserved	Adapt mode	Emu mode
Sample event	P0H.7	P0H.6	P0H.5	P0H.4	P0H.3	P0H.2	P0H.1	P0H.0	P0L.7	P0L.6	P0L.5	P0L.4	P0L.3	P0L.2	P0L.1	P0L.0
Software Reset	-	-	-	X	X	X	X	X	X	X	-	-	-	-	-	-
Watchdog Reset	-	-	-	X	X	X	X	X	X	X	-	-	-	-	-	-
Synchronous Short Hardware Reset	-	-	-	X	X	X	X	X	X	X	X	X	X	X	X	X
Synchronous Long Hardware Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Asynchronous Hardware Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Asynchronous Power-On Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

21 Power reduction modes

Three different power reduction modes with different levels of power reduction have been implemented in the ST10F273M. In Idle mode only the CPU is stopped, while peripherals still operate. In Power-down mode both the CPU and peripherals are stopped. In Standby mode the main power supply (V_{DD}) can be turned off while a portion of the internal RAM remains powered via V_{STBY} dedicated power pin.

Idle and Power-down modes are software activated by a protected instruction and are terminated in different ways as described in the following sections.

Standby mode is entered by simply removing V_{DD}, holding the MCU under reset state.

*Note: All external bus actions are completed before Idle or Power-down mode is entered. However, Idle or Power-down mode is **not** entered if READY is enabled, but has not been activated (driven low for negative polarity, or driven high for positive polarity) during the last bus access.*

21.1 Idle mode

Idle mode is entered by running the IDLE protected instruction. The CPU operation is stopped and the peripherals still run.

Idle mode is terminated by any interrupt request. Whether or not the interrupt is serviced, the instruction following the IDLE instruction will be executed after the return from interrupt (RETI) instruction, and the CPU then resumes the normal program.

21.2 Power-down mode

Power-down mode starts by running the PWRDN protected instruction. The internal clock is stopped and all MCU parts including the watchdog timer are on hold. The only exception could be the Real Time Clock if programmed accordingly in conjuction with selecting one of the two oscillator circuits (either the main or the 32 kHz on-chip oscillator).

If the Real Time Clock module is used when the device is in Power-down mode, a reference clock is needed. In this case, two possible configurations may be selected by the user application according to the desired level of power reduction:

- A 32 kHz crystal is connected to the on-chip low-power oscillator (pins XTAL3 / XTAL4) and running. In this case the main oscillator is stopped when Power-down mode is entered, while the Real Time Clock continues counting using a 32 kHz clock signal as reference. The presence of a running low-power oscillator is detected after the Power-on: This clock is immediately assumed (if present, or as soon as it is detected) as reference for the Real Time Clock counter and it will be maintained indefinitely (unless specifically disabled via software).
- Only the main oscillator is running (XTAL1 / XTAL2 pins). In this case the main oscillator is not stopped when Power-down is entered, and the Real Time Clock continues counting using the main oscillator clock signal as reference.

There are two different operating Power-down modes: protected mode and interruptible mode.

Table 46. List of special function registers (continued)

Name		Physical address		8-bit address	Description	Reset value
ODP7	b	F1D2h	E	E9h	Port 7 open drain control register	- - 00h
ODP8	b	F1D6h	E	EBh	Port 8 open drain control register	- - 00h
ONES	b	FF1Eh		8Fh	Constant value 1's register (read only)	FFFFh
P0L	b	FF00h		80h	PORT0 low register (lower half of PORT0)	- - 00h
P0H	b	FF02h		81h	PORT0 high register (upper half of PORT0)	- - 00h
P1L	b	FF04h		82h	PORT1 low register (lower half of PORT1)	- - 00h
P1H	b	FF06h		83h	PORT1 high register (upper half of PORT1)	- - 00h
P2	b	FFC0h		E0h	Port 2 register	0000h
P3	b	FFC4h		E2h	Port 3 register	0000h
P4	b	FFC8h		E4h	Port 4 register (8-bit)	- - 00h
P5	b	FFA2h		D1h	Port 5 register (read only)	XXXXh
P6	b	FFCCh		E6h	Port 6 register (8-bit)	- - 00h
P7	b	FFD0h		E8h	Port 7 register (8-bit)	- - 00h
P8	b	FFD4h		EAh	Port 8 register (8-bit)	- - 00h
P5DIDIS	b	FFA4h		D2h	Port 5 digital disable register	0000h
PECC0		FEC0h		60h	PEC channel 0 control register	0000h
PECC1		FEC2h		61h	PEC channel 1 control register	0000h
PECC2		FEC4h		62h	PEC channel 2 control register	0000h
PECC3		FEC6h		63h	PEC channel 3 control register	0000h
PECC4		FEC8h		64h	PEC channel 4 control register	0000h
PECC5		FECAh		65h	PEC channel 5 control register	0000h
PECC6		FECCh		66h	PEC channel 6 control register	0000h
PECC7		FECEh		67h	PEC channel 7 control register	0000h
PICON	b	F1C4h	E	E2h	Port input threshold control register	- - 00h
PP0		F038h	E	1Ch	PWM module period register 0	0000h
PP1		F03Ah	E	1Dh	PWM module period register 1	0000h
PP2		F03Ch	E	1Eh	PWM module period register 2	0000h
PP3		F03Eh	E	1Fh	PWM module period register 3	0000h
PSW	b	FF10h		88h	CPU program status word	0000h
PT0		F030h	E	18h	PWM module up/down counter 0	0000h
PT1		F032h	E	19h	PWM module up/down counter 1	0000h
PT2		F034h	E	1Ah	PWM module up/down counter 2	0000h
PT3		F036h	E	1Bh	PWM module up/down counter 3	0000h
PW0		FE30h		18h	PWM module pulse width register 0	0000h

Table 46. List of special function registers (continued)

Name	Physical address	8-bit address	Description	Reset value
XPERCON b	F024h E	12h	XPER configuration register	- - 05h
ZEROS b	FF1Ch	8Eh	Constant value 0's register (read only)	0000h

1. The system configuration is selected during reset. SYSCON reset value is 0000 0xx0 x000 0000b.
2. Reset value depends on different triggered reset event.
3. The XPnIC Interrupt Control Registers control interrupt requests from integrated X-Bus peripherals. Some software controlled interrupt requests may be generated by setting the XPnIR bits (of XPnIC register) of the unused X-Peripheral nodes.

23.2 X-registers

The following table lists in order of their names all X-Bus registers which are implemented in the ST10F273M. Even though they are also physically mapped on XBus memory space, the Flash control registers are listed in a separate section.

Note: The X-Registers are not bit-addressable.

Table 47. List of XBus registers

Name	Physical address	Description	Reset value
CAN1BRPER	EF0Ch	CAN1: BRP extension register	0000h
CAN1BTR	EF06h	CAN1: Bit timing register	2301h
CAN1CR	EF00h	CAN1: CAN control register	0001h
CAN1EC	EF04h	CAN1: error counter	0000h
CAN1IF1A1	EF18h	CAN1: IF1 arbitration 1	0000h
CAN1IF1A2	EF1Ah	CAN1: IF1 arbitration 2	0000h
CAN1IF1CM	EF12h	CAN1: IF1 command mask	0000h
CAN1IF1CR	EF10h	CAN1: IF1 command request	0001h
CAN1IF1DA1	EF1Eh	CAN1: IF1 data A 1	0000h
CAN1IF1DA2	EF20h	CAN1: IF1 data A 2	0000h
CAN1IF1DB1	EF22h	CAN1: IF1 data B 1	0000h
CAN1IF1DB2	EF24h	CAN1: IF1 data B 2	0000h
CAN1IF1M1	EF14h	CAN1: IF1 mask 1	FFFFh
CAN1IF1M2	EF16h	CAN1: IF1 mask 2	FFFFh
CAN1IF1MC	EF1Ch	CAN1: IF1 message control	0000h
CAN1IF2A1	EF48h	CAN1: IF2 arbitration 1	0000h
CAN1IF2A2	EF4Ah	CAN1: IF2 arbitration 2	0000h
CAN1IF2CM	EF42h	CAN1: IF2 command mask	0000h
CAN1IF2CR	EF40h	CAN1: IF2 command request	0001h
CAN1IF2DA1	EF4Eh	CAN1: IF2 data A 1	0000h

24.2 Recommended operating conditions

Table 54. Recommended operating conditions

Symbol	Parameter	Value		Unit
		Min	Max	
V_{DD}	Operating supply voltage	4.5	5.5	V
V_{STBY}	Operating standby supply voltage(1)			
V_{AREF}	Operating analog reference voltage(2)	0	V_{DD} + 0.1	
T_A	Ambient temperature under bias	-40	+125	°C
T_J	Junction temperature under bias		+150	

1. The value of the V_{STBY} voltage is specified in the range of 4.5 to 5.5 Volt. Nevertheless, it is acceptable to exceed the upper limit (up to 6.0 Volt) for a maximum of 100 hours over the global 300000 hours, representing the lifetime of the device (about 30 years). On the other hand, it is possible to exceed the lower limit (down to 4.0 Volt) whenever RTC and 32 kHz on-chip oscillator amplifier are turned off (only Standby RAM powered through VSTBY pin in Standby mode). When V_{STBY} voltage is lower than main V_{DD}, the input section of V_{STBY}/EA pin can generate a spurious static consumption on V_{DD} power supply (in the range of tenth of µA).
2. For details on operating conditions concerning the usage of A/D converter refer to *Section 24.7*.

24.3 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

Equation 1:

$$T_J = T_A + (P_D \times \Theta_{JA})$$

Where:

T_A is the Ambient Temperature in °C,

Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in °C/W,

P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),

P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watt. This is the Chip Internal Power,

$P_{I/O}$ represents the Power Dissipation on Input and Output Pins; User Determined.

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

Equation 2:

$$P_D = K / (T_J + 273°C)$$

Therefore (solving equations 1 and 2):

Equation 3:

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2$$

Table 59. Flash data retention characteristics

Number of program / erase cycles ($-40°C \le T_A \le 125°C$)	Data retention time (average ambient temperature 60°C)	
	256 Kbyte (code store)	64 Kbyte (EEPROM emulation)(1)
0 - 100	> 20 years	> 20 years
1000	-	> 20 years
10000	-	10 years
100000	-	1 year

1. Two 64 Kbyte Flash Sectors may be typically used to emulate up to 4, 8 or 16 Kbytes of EEPROM. Therefore, in case of an emulation of a 16 Kbyte EEPROM, 100,000 Flash Program / Erase cycles are equivalent to 800,000 EEPROM Program/Erase cycles.
For an efficient use of the Read While Write feature and/or EEPROM Emulation, please refer to the dedicated application note *EEPROM Emulation with ST10F2xx* (AN2061). Contact your local field service, local sales person or STMicroelectronics representative to obtain a copy of such a guideline document.

24.7 A/D converter characteristics

V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = -40 to +125°C, 4.5V ≤ V_{AREF} ≤ V_{DD},
V_{SS} ≤ V_{AGND} ≤ V_{SS} + 0.2V

Table 60. A/D converter characteristics

Symbol		Parameter	Test condition	Limit values		Unit
				Min	Max	
V_{AREF}	SR	Analog reference voltage(1)		4.5	V_{DD}	V
V_{AGND}	SR	Analog ground voltage		V_{SS}	V_{SS} + 0.2	V
V_{AIN}	SR	Analog input voltage(2)		V_{AGND}	V_{AREF}	V
I_{AREF}	CC	Reference supply current	Running mode(3)	–	5	mA
			Power down mode	–	1	µA
t_S	CC	Sample time	(4)	1	–	µs
t_C	CC	Conversion time	(5)	3	–	µs
DNL	CC	Differential non linearity(6)	No overload	–1	+1	LSB
INL	CC	Integral non linearity(6)	No overload	–1.5	+1.5	LSB
OFS	CC	Offset error(6)	No overload	–1.5	+1.5	LSB
TUE	CC	Total unadjusted error(6)	Port5 Port1 - No overload(3) Port1 - Overload(3)	–2.0 –5.0 –7.0	+2.0 +5.0 +7.0	LSB
K	CC	Coupling factor between inputs(3)(7)	On both Port5 and Port1	–	10^{-6}	–
C_{P1}	CC	Input pin capacitance(3)(8)		–	3	pF
C_{P2}	CC		Port5 Port1	–	4 6	pF

Example of external network sizing

The following hypotheses are formulated in order to proceed in designing the external network on A/D converter input pins:

- Analog Signal Source Bandwidth (f_0): 10 kHz
- Conversion Rate (f_C): 25 kHz
- Sampling Time (T_S): 1µs
- Pin Input Capacitance (C_{P1}): 5pF
- Pin Input Routing Capacitance (C_{P2}): 1pF
- Sampling Capacitance (C_S): 4pF
- Maximum Input Current Injection (I_{INJ}): 3mA
- Maximum Analog Source Voltage ($V_{AM)}$: 12V
- Analog Source Impedance (R_S): 100Ω
- Channel Switch Resistance (R_{SW}): 500Ω
- Sampling Switch Resistance (R_{AD}): 200Ω

1. Supposing to design the filter with the pole exactly at the maximum frequency of the signal, the time constant of the filter is:

$$R_C C_F = \frac{1}{2\pi f_0} = 15.9\mu s$$

2. Using the relation between C_F and C_S and taking some margin (4000 instead of 2048), it is possible to define C_F:

$$C_F = 4000\, C_S = 16nF$$

3. As a consequence of step 1 and 2, RC can be chosen:

$$R_F = \frac{1}{2\pi f_0 C_F} = 995\Omega \cong 1k\Omega$$

4. Considering the current injection limitation and supposing that the source can go up to 12V, the total series resistance can be defined as:

$$R_S + R_F + R_L = \frac{V_{AM}}{I_{INJ}} = 4k\Omega$$

from which is now simple to define the value of R_L:

$$R_L = \frac{V_{AM}}{I_{INJ}} - R_F - R_S = 2.9k\Omega$$

5. Now the three elements of the external circuit R_F, C_F and R_L are defined. Some conditions discussed in the previous paragraphs have been used to size the component, the other must now be verified. The relation which allows minimization of

The frequency of CPU clock (f_{CPU}) directly follows the frequency of f_{XTAL} so the high and low time of f_{CPU} (that is, the duration of an individual TCL) is defined by the duty cycle of the input clock f_{XTAL}.

Therefore, the timings given in this chapter refer to the minimum TCL. This minimum value can be calculated by the following formula:

$$TCL_{min} = 1/f_{XTAL} \times DC_{min}$$

$$DC = \text{duty cycle}$$

For two consecutive TCLs, the deviation caused by the duty cycle of f_{XTAL} is compensated, so the duration of 2TCL is always $1/f_{XTAL}$.

The minimum value TCL_{min} has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula:

$$2TCL = 1/f_{XTAL}$$

The address float timings in Multiplexed bus mode (t_{11} and t_{45}) use the maximum duration of TCL ($TCL_{max} = 1/f_{XTAL} \times DC_{max}$) instead of TCL_{min}.

Similarly to what happen for Prescaler Operation, if the bit OWDDIS in SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

24.8.6 Oscillator watchdog (OWD)

An on-chip watchdog oscillator is implemented in the ST10F273M. This feature is used for safety operation with external crystal oscillator (available only when using direct drive mode with or without prescaler, so the PLL is not used to generate the CPU clock multiplying the frequency of the external crystal oscillator). This watchdog oscillator operates as following.

The reset default configuration enables the watchdog oscillator. It can be disabled by setting the OWDDIS (bit 4) of SYSCON register.

When the OWD is enabled, the PLL runs at its free-running frequency, and it increments the watchdog counter. On each transition of external clock, the watchdog counter is cleared. If an external clock failure occurs, then the watchdog counter overflows (after 16 PLL clock cycles).

The CPU clock signal will be switched to the PLL free-running clock signal, and the oscillator watchdog Interrupt Request is flagged. The CPU clock will not switch back to the external clock even if a valid external clock exits on XTAL1 pin. Only a hardware reset (or bidirectional Software / Watchdog reset) can switch the CPU clock source back to direct clock input.

When the OWD is disabled, the CPU clock is always the external oscillator clock (in Direct Drive or Prescaler Operation) and the PLL is switched off to decrease consumption supply current.

24.8.7 Phase locked loop (PLL)

For all other combinations of pins P0.15-13 (P0H.7-5) during reset the on-chip phase locked loop is enabled and it provides the CPU clock (see *Table 62*). The PLL multiplies the input frequency by the factor F which is selected via the combination of pins P0.15-13 (f_{CPU} =

Example 1

- f_{XTAL} = 4 MHz
- P0(15:13) = '110' (multiplication by 3)
- PLL Input Frequency = 1 MHz
- VCO frequency = 48 MHz: ***NOT VALID**, must be 64 to 128 MHz*
- f_{CPU} = NOT VALID

Example 2

- f_{XTAL} = 8 MHz
- P0(15:13) = '100' (multiplication by 5)
- PLL Input Frequency = 2 MHz
- VCO frequency = 80 MHz
- PLL Output Frequency = 40 MHz (VCO frequency divided by 2)
- f_{CPU} = 40 MHz (no effect of Output Prescaler)

24.8.9 PLL jitter

The following terminology is hereafter defined:

- **Self referred single period jitter**
  Also called "Period Jitter", it can be defined as the difference of the T_{max} and T_{min}, where T_{max} is maximum time period of the PLL output clock and T_{min} is the minimum time period of the PLL output clock.
- **Self referred long term jitter**
  Also called "N period jitter", it can be defined as the difference of T_{max} and T_{min}, where T_{max} is the maximum time difference between N + 1 clock rising edges and T_{min} is the minimum time difference between N + 1 clock rising edges. Here N should be kept sufficiently large to have the long term jitter. For N = 1, this becomes the single period jitter.

Jitter at the PLL output can be due to the following reasons:

- Jitter in the input clock
- Noise in the PLL loop

Jitter in the input clock

PLL acts like a low pass filter for any jitter in the input clock. Input Clock jitter with the frequencies within the PLL loop bandwidth is passed to the PLL output and higher frequency jitter (frequency > PLL bandwidth) is attenuated @20dB/decade.

Noise in the PLL loop

This contribution again can be caused by the following sources:

- Device noise of the circuit in the PLL
- Noise in supply and substrate.

Device noise of the circuit in the PLL

The long term jitter is inversely proportional to the bandwidth of the PLL: the wider is the loop bandwidth, the lower is the jitter due to noise in the loop. Besides, the long term jitter is practically independent on the multiplication factor.

24.8.18 CLKOUT and $\overline{\text{READY}}$

V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = -40 to + 125°C, CL = 50pF

Table 73. CLKOUT and $\overline{\text{READY}}$ timings

Symbol		Parameter	f_{CPU} = 40 MHz TCL = 12.5ns		Variable CPU clock 1/2 TCL = 1 to 40 MHz		Unit
			Min	Max	Min	Max	
t_{29}	CC	CLKOUT cycle time	25	25	2TCL	2TCL	ns
t_{30}	CC	CLKOUT high time	9	–	TCL – 3.5	–	
t_{31}	CC	CLKOUT low time	10	–	TCL – 2.5	–	
t_{32}	CC	CLKOUT rise time	–	4	–	4	
t_{33}	CC	CLKOUT fall time	–	4	–	4	
t_{34}	CC	CLKOUT rising edge to ALE falling edge	$-2 + t_A$	$8 + t_A$	$-2 + t_A$	$8 + t_A$	
t_{35}	SR	Synchronous $\overline{\text{READY}}$ setup time to CLKOUT	17	–	17	–	
t_{36}	SR	Synchronous $\overline{\text{READY}}$ hold time after CLKOUT	2	–	2	–	
t_{37}	SR	Asynchronous $\overline{\text{READY}}$ low time	35	–	2TCL + 10	–	
t_{58}	SR	Asynchronous $\overline{\text{READY}}$ setup time(1)	17	–	17	–	
t_{59}	SR	Asynchronous $\overline{\text{READY}}$ hold time (1)	2	–	2	–	
t_{60}	SR	Async. $\overline{\text{READY}}$ hold time after $\overline{\text{RD}}$, $\overline{\text{WR}}$ high (Demultiplexed bus)(2)	0	$2t_A + t_C + t_F$	0	$2t_A + t_C + t_F$	

1. These timings are given for characterization purposes only, in order to assure recognition at a specific clock edge.
2. Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating READY. $2t_A$ and t_C refer to the next following bus cycle, t_F refers to the current bus cycle.

27 Revision history

Table 80. Document revision history

Date	Revision	Changes
03-May-2007	1	Initial release
02-Jul-2007	2	Changed document status from Preliminary Data to Datasheet *Section 4: Memory organization on page 21*: - changed size of B0TF from 8 to 4Kbytes - removed 'Flash Temporary Unprotection' from X-Miscellaneous features *Table 2: Summary of IFlash address range on page 21*: Changed size of B0TF from 8 to 4Kbytes *Figure 6: Flash structure on page 27*: Changed Test-Flash size from 8 to 4Kbytes *Table 5: Flash module sectorization (write operations, or ROMS1 = '1') on page 29*: Changed B0TF address and size (8 to 4Kbytes) *Section 14: A/D converter on page 72*: Replaced '40.630 CPU clock cycles' with '40630 CPU clock cycles' in end of section *Section 21.1: Idle mode on page 109*: Made minor text changes *Section 21.2: Power-down mode on page 109*: Made minor text changes *Table 57: DC characteristics on page 134*: - changed max value and unit for I_{PD1} from 1mA to 150µA - changed max value and unit for I_{PD3} from 1.1mA to 200µA - changed test conditions and max values for I_{SB2} - changed footnote link for symbol I_{P0H} - changed footnote link for symbol I_{P0L} *Table 58: Flash characteristics on page 138*: - modified Bank 0 program parameter and values - removed Bank 1 program parameter and values - modified Bank 0 erase parameter and values - removed Bank 1 erase parameter and values *Section 24.7.4: Analog reference pins on page 143*: Minor text editing changes *Table 62: On-chip clock generator selections on page 151*: - changed external clock input range for f_{XTAL} x 5 - changed external clock input range for f_{XTAL} x 1 - replaced 'CPU clock range of 1...60 MHz' with 'CPU clock range of 1...40 MHz' in footnote 1 Added *Section 25.1: ECOPACK® on page 180* and updated content Added *Section 26.2: Mechanical data and package dimensions on page 174*
20-Aug-2012	3	Updated *Table 17: FARH register description* Updated *Chapter 25: Package information* Updated *Table 79: Order codes*
17-Sep-2013	4	Updated Disclaimer