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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ST10
Core Size	16-Bit
Speed	40MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	144-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f273m-4qr3

4 Memory organization

The memory space of the ST10F273M is configured in a unified memory architecture. Code memory, data memory, registers and I/O ports are organized within the same linear address space of 16 Mbytes. The entire memory space can be accessed Bytewise or Wordwise. Particular portions of the on-chip memory have additionally been made directly bit addressable.

IFlash: 512 Kbytes of on-chip Flash memory implemented as a unique Bank (Bank0). Bank0 is divided in 12 blocks (B0F0...B0F11).

Note: Read-while-write operations are not allowed: Write commands must be executed from a non IFlash memory area (on-chip RAM or external memory).

When Bootstrap mode is selected, the Test-Flash Block B0TF (4 Kbytes) appears at address 00'0000h: Refer to the device User Manual for more details on the memory mapping in Bootstrap mode. The summary of address range for IFlash is the following:

Table 2. Summary of IFlash address range

Blocks	User mode	Size (bytes)
B0TF	Not visible	4 K
B0F0	00'0000h - 00'1FFFh	8 K
B0F1	00'2000h - 00'3FFFh	8 K
B0F2	00'4000h - 00'5FFFh	8 K
B0F3	00'6000h - 00'7FFFh	8 K
B0F4	01'8000h - 01'FFFFh	32 K
B0F5	02'0000h - 02'FFFFh	64 K
B0F6	03'0000h - 03'FFFFh	64 K
B0F7	04'0000h - 04'FFFFh	64 K
B0F8	05'0000h - 05'FFFFh	64 K
B0F9	06'0000h - 06'FFFFh	64 K
B1F0 / B0F10 (1)	07'0000h - 07'FFFFh	64 K
B1F1 / B0F11 (1)	08'0000h - 08'FFFFh	64 K

Note: A single Flash bank is implemented on the ST10F273M compared to the ST10F273E. The last two sectors (B0F10 and B0F11) can be seen as the Bank1 of the ST10F273E in order to maintain the compatibility with the existing Flash programming drivers. For this, the control and status bit of the blocks B0F10 and B0F11 have been duplicated to be usable as blocks B1F0 and B1F1 of the ST10F273E.

XFLASH / Flash Control Registers: Address range 0E'0000h-0E'FFFFh is reserved for the Flash Control Register and other internal service memory space used by the Flash Program/Erase Controller. XFLASHEN bit in XPERCON register must be set to access the Flash Control Register. Note that when Flash Control Registers are not accessible, no program/erase operations are possible. The Flash Control Registers are accessed in 16-bit demultiplexed bus-mode without read/write delay. Byte and word accesses are allowed.

The Addresses from 0x0E 0000 to 0x0E FFFF are reserved for the Control Register Interface and other internal service memory space used by the Flash Program/Erase controller.

The following tables show the memory mapping of the Flash when it is accessed in read mode (*Table 4: Flash module sectorization (read operations)*), and when accessed in write or erase mode (*Table 5: Flash module sectorization (write operations, or ROMS1 = '1')*).

Note: With this second mapping, the first four sectors are remapped into code segment 1 (same as obtained setting bit ROMS1 in SYSCON register).

Table 4. Flash module sectorization (read operations)

Bank	Description	Addresses	Size (bytes)
B0	Bank 0 Flash 0 (B0F0)	0x00 0000 - 0x00 1FFF	8 K
	Bank 0 Flash 1 (B0F1)	0x00 2000 - 0x00 3FFF	8 K
	Bank 0 Flash 2 (B0F2)	0x00 4000 - 0x00 5FFF	8 K
	Bank 0 Flash 3 (B0F3)	0x00 6000 - 0x00 7FFF	8 K
	Bank 0 Flash 4 (B0F4)	0x01 8000 - 0x01 FFFF	32 K
	Bank 0 Flash 5 (B0F5)	0x02 0000 - 0x02 FFFF	64 K
	Bank 0 Flash 6 (B0F6)	0x03 0000 - 0x03 FFFF	64 K
	Bank 0 Flash 7 (B0F7)	0x04 0000 - 0x04 FFFF	64 K
	Bank 0 Flash 8 (B0F8)	0x05 0000 - 0x05 FFFF	64 K
	Bank 0 Flash 9 (B0F9)	0x06 0000 - 0x06 FFFF	64 K
	Bank 0 Flash 10 (B0F10 / B1F0) (1)	0x07 0000 - 0x07 FFFF	64 K
	Bank 0 Flash 11 (B0F11 / B1F1) (1)	0x08 0000 - 0x08 FFFF	64 K

1. A single bank is implemented but the last two sectors can be seen as a Bank 1 in order to maintain compatibility with the Flash Programming routines developed for the ST10F273E (based on ST10F276E). This means that the Control and Status flags for the blocks B0F10 and B0F11 are duplicated to also be accessible as blocks B1F0 and B1F1.

6.3 Alternate and selective boot mode (ABM and SBM)

6.3.1 Activation of the ABM and SBM

Alternate boot is activated with the combination ‘01’ on Port0L[5..4] at the rising edge of $\overline{\text{RSTIN}}$.

6.3.2 User mode signature integrity check

The behavior of the Selective Boot mode is based on the computing of a signature between the content of two memory locations and a comparison with a reference signature. This requires that users who use Selective Boot have reserved and programmed the Flash memory locations.

6.3.3 Selective boot mode

When the user signature is not correct, instead of executing the Standard Bootstrap Loader (triggered by P0L.4 low at reset), additional check is made.

Depending on the value at the User key location, the following behavior occurs:

- A jump is performed to the Standard Bootstrap Loader
- Only UART is enabled for bootstrapping
- Only CAN1 is enabled for bootstrapping
- The device enters an infinite loop

7.2 Instruction set summary

Table 28 lists the instructions of the ST10F273M. The detailed description of each instruction can be found in the *ST10 Family Programming Manual*.

Table 28. Standard instruction set summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-/16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise XOR, (word/byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS	Move byte operand to word operand with sign extension	2 / 4
MOVBZ	Move byte operand to word operand with zero extension	2 / 4
JMPA, JMPI, JMPR	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4

8 External bus controller

All of the external memory accesses are performed by the on-chip external bus controller.

The EBC can be programmed to single chip mode when no external memory is required, or to one of four different external memory access modes:

- 16- / 18- / 20- / 24-bit addresses and 16-bit data, demultiplexed
- 16- / 18- / 20- / 24-bit addresses and 16-bit data, multiplexed
- 16- / 18- / 20- / 24-bit addresses and 8-bit data, multiplexed
- 16- / 18- / 20- / 24-bit addresses and 8-bit data, demultiplexed

In demultiplexed bus modes addresses are output on PORT1 and data is input / output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input / output.

Timing characteristics of the external bus interface (memory cycle time, memory tri-state time, length of ALE and read / write delay) are programmable giving the choice of a wide range of memories and external peripherals.

Up to four independent address windows may be defined (using register pairs ADDRSELx / BUSCONx) to access different resources and bus characteristics.

These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1.

All accesses to locations not covered by these four address windows are controlled by BUSCON0. Up to five external $\overline{CS}$ signals (four windows plus default) can be generated in order to save external glue logic. Access to very slow memories is supported by a ‘Ready’ function.

A $\overline{HOLD}$ / $\overline{HLDA}$ protocol is available for bus arbitration which shares external resources with other bus masters.

The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7...P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In master mode (default after reset) the $\overline{HLDA}$ pin is an output. By setting bit DP6.7 to ‘1’ the slave mode is selected where pin $\overline{HLDA}$ is switched to input. This directly connects the slave controller to another master controller without glue logic.

For applications which require less external memory space, the address space can be restricted to 1 Mbyte, 256 Kbytes or to 64 Kbytes. Port 4 outputs all eight address lines if an address space of 16 Mbytes is used, otherwise four, two or no address lines.

Chip select timing can be made programmable. By default (after reset), the $\overline{CSx}$ lines change half a CPU clock cycle after the rising edge of ALE. With the CSCFG bit set in the SYSCON register the $\overline{CSx}$ lines change with the rising edge of ALE.

The active level of the READY pin can be set by bit RDYPOL in the BUSCONx registers. When the READY function is enabled for a specific address window, each bus cycle within the window must be terminated with the active level defined by bit RDYPOL in the associated BUSCON register.

Table 30. Interrupt sources (continued)

Source of interrupt or PEC service request	Request flag	Enable flag	Interrupt vector	Vector location	Trap number
CAPCOM Register 6	CC6IR	CC6IE	CC6INT	00'0058h	16h
CAPCOM Register 7	CC7IR	CC7IE	CC7INT	00'005Ch	17h
CAPCOM Register 8	CC8IR	CC8IE	CC8INT	00'0060h	18h
CAPCOM Register 9	CC9IR	CC9IE	CC9INT	00'0064h	19h
CAPCOM Register 10	CC10IR	CC10IE	CC10INT	00'0068h	1Ah
CAPCOM Register 11	CC11IR	CC11IE	CC11INT	00'006Ch	1Bh
CAPCOM Register 12	CC12IR	CC12IE	CC12INT	00'0070h	1Ch
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	00'0074h	1Dh
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	00'0078h	1Eh
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	00'007Ch	1Fh
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	00'00C0h	30h
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	00'00C4h	31h
CAPCOM Register 18	CC18IR	CC18IE	CC18INT	00'00C8h	32h
CAPCOM Register 19	CC19IR	CC19IE	CC19INT	00'00CCh	33h
CAPCOM Register 20	CC20IR	CC20IE	CC20INT	00'00D0h	34h
CAPCOM Register 21	CC21IR	CC21IE	CC21INT	00'00D4h	35h
CAPCOM Register 22	CC22IR	CC22IE	CC22INT	00'00D8h	36h
CAPCOM Register 23	CC23IR	CC23IE	CC23INT	00'00DCh	37h
CAPCOM Register 24	CC24IR	CC24IE	CC24INT	00'00E0h	38h
CAPCOM Register 25	CC25IR	CC25IE	CC25INT	00'00E4h	39h
CAPCOM Register 26	CC26IR	CC26IE	CC26INT	00'00E8h	3Ah
CAPCOM Register 27	CC27IR	CC27IE	CC27INT	00'00ECh	3Bh
CAPCOM Register 28	CC28IR	CC28IE	CC28INT	00'00F0h	3Ch
CAPCOM Register 29	CC29IR	CC29IE	CC29INT	00'0110h	44h
CAPCOM Register 30	CC30IR	CC30IE	CC30INT	00'0114h	45h
CAPCOM Register 31	CC31IR	CC31IE	CC31INT	00'0118h	46h
CAPCOM Timer 0	T0IR	T0IE	T0INT	00'0080h	20h
CAPCOM Timer 1	T1IR	T1IE	T1INT	00'0084h	21h
CAPCOM Timer 7	T7IR	T7IE	T7INT	00'00F4h	3Dh
CAPCOM Timer 8	T8IR	T8IE	T8INT	00'00F8h	3Eh
GPT1Timer 2	T2IR	T2IE	T2INT	00'0088h	22h
GPT1 Timer 3	T3IR	T3IE	T3INT	00'008Ch	23h
GPT1 Timer 4	T4IR	T4IE	T4INT	00'0090h	24h
GPT2Timer 5	T5IR	T5IE	T5INT	00'0094h	25h

Table 31. X-Interrupt detailed mapping (continued)

Interrupt source	XP0INT	XP1INT	XP2INT	XP3INT
PLL Unlock / OWD				x
PWM1 Channel 3...0			x	x

9.2 Exception and error traps list

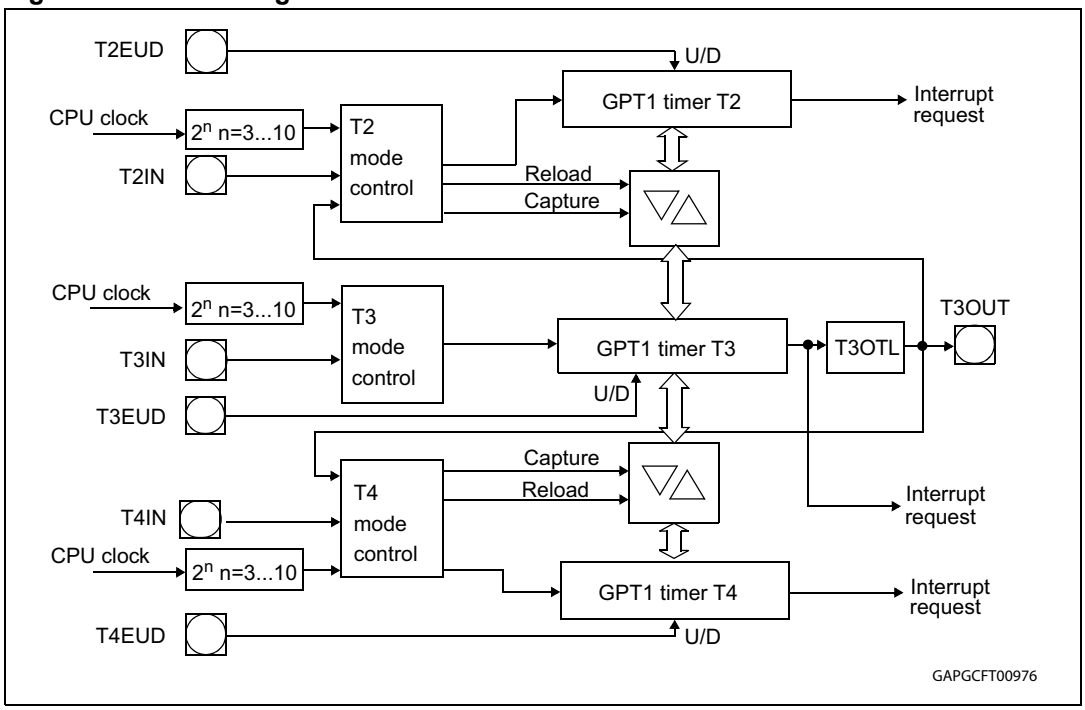
Table 32 shows all of the possible exceptions or error conditions that can arise during run-time.

Table 32. Trap priorities

Exception condition	Trap flag	Trap vector	Vector location	Trap number	Trap priority(1)
Reset Functions: Hardware Reset Software Reset Watchdog Timer Overflow		 RESET RESET RESET	 00'0000h 00'0000h 00'0000h	 00h 00h 00h	 III III III
Class A Hardware Traps: Non-Maskable Interrupt Stack Overflow Stack Underflow	 NMI STKOF STKUF	 NMITRAP STOTRAP STUTRAP	 00'0008h 00'0010h 00'0018h	 02h 04h 06h	 II II II
Class B Hardware Traps: Undefined Opcode MAC Interruption Protected Instruction Fault Illegal word Operand Access Illegal Instruction Access Illegal External Bus Access	 UNDOPC MACTRP PRTFLT ILLOPA ILLINA ILLBUS	 BTRAP BTRAP BTRAP BTRAP BTRAP BTRAP	 00'0028h 00'0028h 00'0028h 00'0028h 00'0028h 00'0028h	 0Ah 0Ah 0Ah 0Ah 0Ah 0Ah	 I I I I I I
Reserved			[002Ch - 003Ch]	[0Bh - 0Fh]	
Software Traps TRAP Instruction			Any 0000h – 01FCh in steps of 4h	Any [00h - 7Fh]	Current CPU Priority

1. - All the class B traps have the same trap number (and vector) and the same lower priority compared to the class A traps and to the resets.
   - Each class A trap has a dedicated trap number (and vector). They are prioritized in the second priority level.
   - The resets have the highest priority level and the same trap number.
   - The PSW.ILVL CPU priority is forced to the highest level (15) when these exceptions are serviced.

Figure 11. Block diagram of GPT1

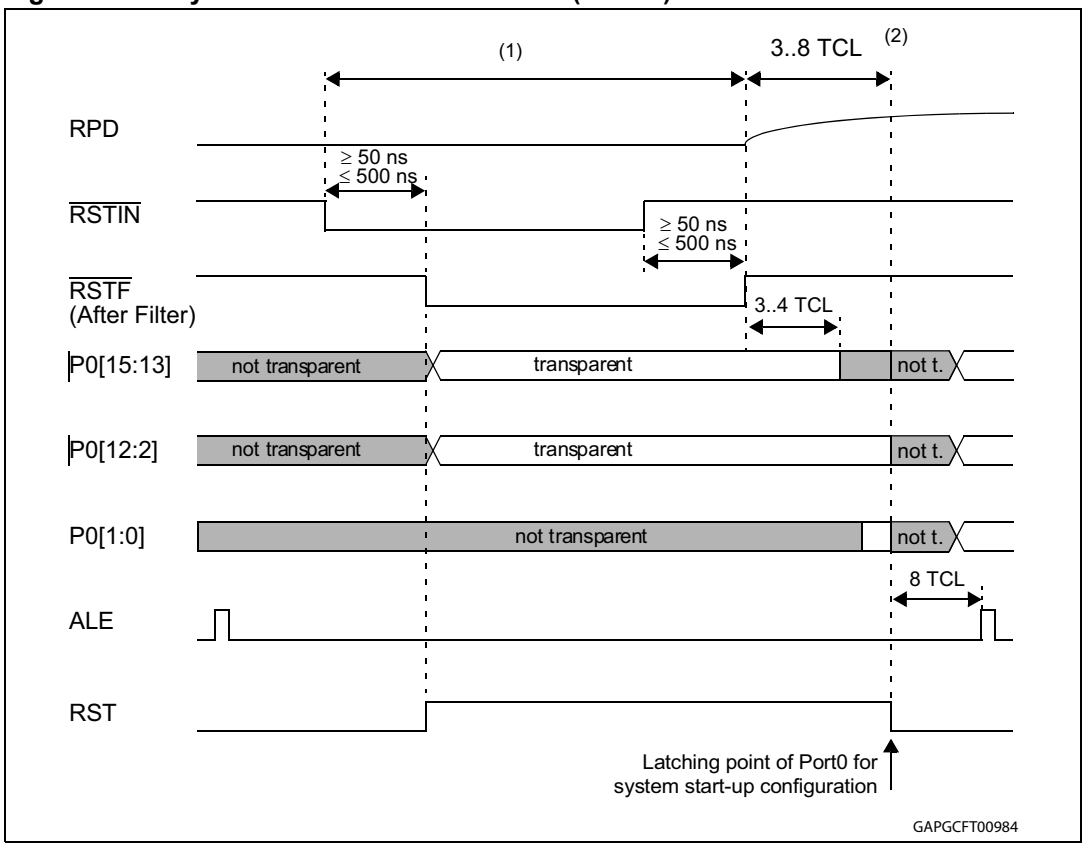


In any case, a maximum of 100nF on V_{18} pin should not generate problems of over-current (higher value is allowed if current is limited by the external hardware). External current limitation is nevertheless also recommended to avoid risks of damage in case of a temporary short between V_{18} and ground: The internal 1.8V drivers are sized to drive currents of several tens of amps, so the current must be limited by the external hardware.
The limit of current is imposed by power dissipation considerations (refer to *Section 24: Electrical characteristics*).

In Figures *18* and *19* Asynchronous Power-on timing diagrams are shown, respectively with boot from internal or external memory, highlighting the reset phase extension introduced by the embedded IFlash module when selected.

Caution: Never power the device without keeping the RSTIN pin grounded: The device could enter into unpredictable states, risking also permanent damage.

Figure 21. Asynchronous hardware RESET ($\overline{EA}$ = 0)



1. Longer than Port0 settling time + PLL synchronization (if needed, that is P0(15:13) changed). Longer than 500ns to take into account of Input Filter on RSTIN pin.
2. 3 to 8 TCL depending on clock source selection.

Exit from asynchronous reset state

When the $\overline{RSTIN}$ pin is pulled high, the device restarts: As already mentioned, if internal Flash is used, the restarting occurs after the embedded Flash initialization routine is completed. The system configuration is latched from Port0: ALE, $\overline{RD}$ and $\overline{WR}$/$\overline{WRL}$ pins are driven to their inactive level. The ST10F273M starts program execution from memory location 00'0000h in code segment 0. This starting location will typically point to the general initialization routine. The timings of asynchronous Hardware Reset sequence are summarized in *Figure 20* and *Figure 21*.

20.3 Synchronous reset (warm reset)

A synchronous reset is triggered when $\overline{RSTIN}$ pin is pulled low while RPD pin is at high level. In order to properly activate the internal reset logic of the device, the $\overline{RSTIN}$ pin must be held low, at least, during 4 TCL (two periods of CPU clock): refer also to *Section 20.1* for details on minimum reset pulse duration. The I/O pins are set to high impedance and $\overline{RSTOUT}$ pin is driven low. After $\overline{RSTIN}$ level is detected, a short duration of a maximum of 12 TCL (six periods of CPU clock) elapses, during which pending internal hold states are cancelled and the current internal access cycle if any is completed. External bus cycle is aborted. The internal pull-down of $\overline{RSTIN}$ pin is activated if bit BDRSTEN of SYSCON

Figure 29. SW / WDT bidirectional RESET ($\overline{EA}$ = 0)

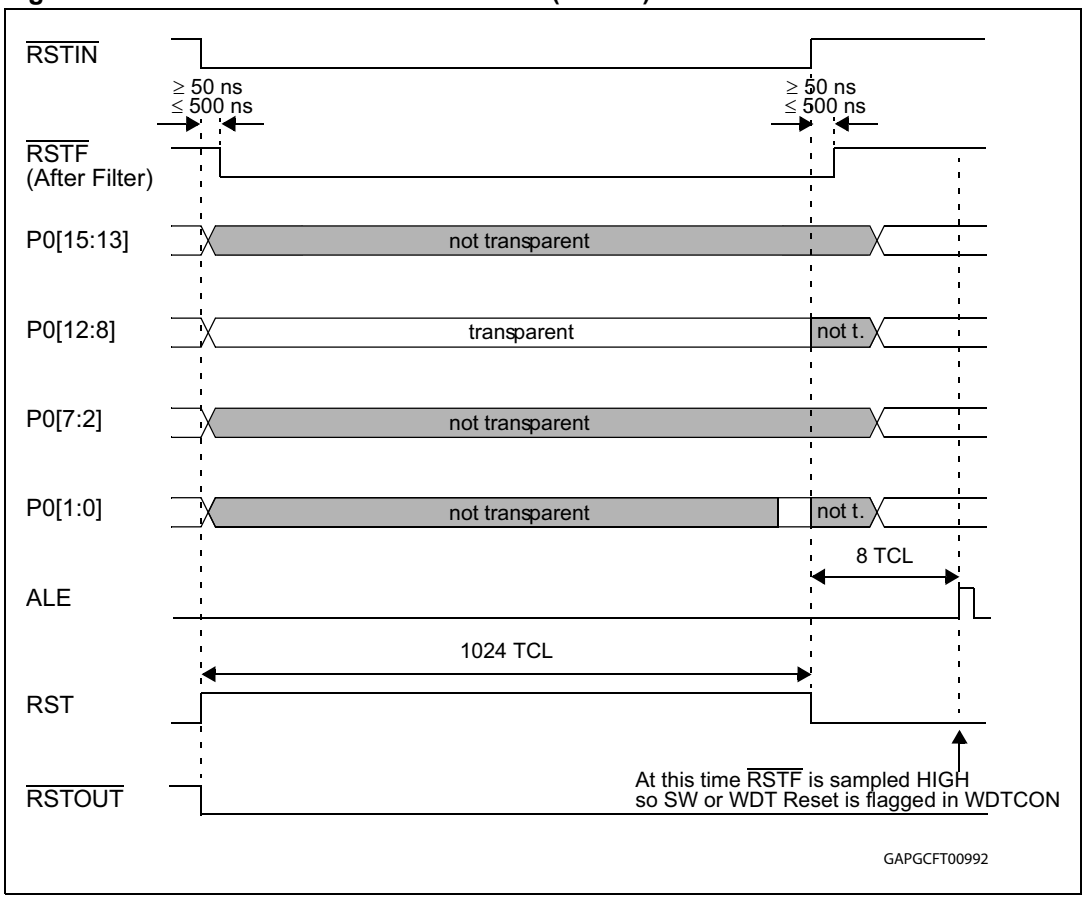


Table 46. List of special function registers (continued)

Name	Physical address	8-bit address	Description	Reset value
CC21	FE6Ah	35h	CAPCOM register 21	0000h
CC21IC b	F16Ah E	B5h	CAPCOM register 21 interrupt control register	- - 00h
CC22	FE6Ch	36h	CAPCOM register 22	0000h
CC22IC b	F16Ch E	B6h	CAPCOM register 22 interrupt control register	- - 00h
CC23	FE6Eh	37h	CAPCOM register 23	0000h
CC23IC b	F16Eh E	B7h	CAPCOM register 23 interrupt control register	- - 00h
CC24	FE70h	38h	CAPCOM register 24	0000h
CC24IC b	F170h E	B8h	CAPCOM register 24 interrupt control register	- - 00h
CC25	FE72h	39h	CAPCOM register 25	0000h
CC25IC b	F172h E	B9h	CAPCOM register 25 interrupt control register	- - 00h
CC26	FE74h	3Ah	CAPCOM register 26	0000h
CC26IC b	F174h E	BAh	CAPCOM register 26 interrupt control register	- - 00h
CC27	FE76h	3Bh	CAPCOM register 27	0000h
CC27IC b	F176h E	BBh	CAPCOM register 27 interrupt control register	- - 00h
CC28	FE78h	3Ch	CAPCOM register 28	0000h
CC28IC b	F178h E	BCh	CAPCOM register 28 interrupt control register	- - 00h
CC29	FE7Ah	3Dh	CAPCOM register 29	0000h
CC29IC b	F184h E	C2h	CAPCOM register 29 interrupt control register	- - 00h
CC30	FE7Ch	3Eh	CAPCOM register 30	0000h
CC30IC b	F18Ch E	C6h	CAPCOM register 30 interrupt control register	- - 00h
CC31	FE7Eh	3Fh	CAPCOM register 31	0000h
CC31IC b	F194h E	CAh	CAPCOM register 31 interrupt control register	- - 00h
CCM0 b	FF52h	A9h	CAPCOM Mode Control register 0	0000h
CCM1 b	FF54h	AAh	CAPCOM Mode Control register 1	0000h
CCM2 b	FF56h	ABh	CAPCOM Mode Control register 2	0000h
CCM3 b	FF58h	ACh	CAPCOM Mode Control register 3	0000h
CCM4 b	FF22h	91h	CAPCOM Mode Control register 4	0000h
CCM5 b	FF24h	92h	CAPCOM Mode Control register 5	0000h
CCM6 b	FF26h	93h	CAPCOM Mode Control register 6	0000h
CCM7 b	FF28h	94h	CAPCOM Mode Control register 7	0000h
CP	FE10h	08h	CPU Context Pointer register	FC00h
CRIC b	FF6Ah	B5h	GPT2 CAPREL interrupt control register	- - 00h
CSP	FE08h	04h	CPU Code Segment Pointer register (read only)	0000h
DP0L b	F100h E	80h	P0L direction control register	- - 00h

Table 47. List of XBus registers (continued)

Name	Physical address	Description	Reset value
CAN2IF2CM	EE42h	CAN2: IF2 command mask	0000h
CAN2IF2CR	EE40h	CAN2: IF2 command request	0001h
CAN2IF2DA1	EE4Eh	CAN2: IF2 data A 1	0000h
CAN2IF2DA2	EE50h	CAN2: IF2 data A 2	0000h
CAN2IF2DB1	EE52h	CAN2: IF2 data B 1	0000h
CAN2IF2DB2	EE54h	CAN2: IF2 data B 2	0000h
CAN2IF2M1	EE44h	CAN2: IF2 mask 1	FFFFh
CAN2IF2M2	EE46h	CAN2: IF2 mask 2	FFFFh
CAN2IF2MC	EE4Ch	CAN2: IF2 message control	0000h
CAN2IP1	EEA0h	CAN2: interrupt pending 1	0000h
CAN2IP2	EEA2h	CAN2: interrupt pending 2	0000h
CAN2IR	EE08h	CAN2: interrupt register	0000h
CAN2MV1	EEB0h	CAN2: message valid 1	0000h
CAN2MV2	EEB2h	CAN2: message valid 2	0000h
CAN2ND1	EE90h	CAN2: new data 1	0000h
CAN2ND2	EE92h	CAN2: new data 2	0000h
CAN2SR	EE02h	CAN2: status register	0000h
CAN2TR	EE0Ah	CAN2: test register	00x0h
CAN2TR1	EE80h	CAN2: transmission request 1	0000h
CAN2TR2	EE82h	CAN2: Transmission request 2	0000h
I2CCCR1	EA06h	I2C clock control register 1	0000h
I2CCCR2	EA0Eh	I2C clock control register 2	0000h
I2CCR	EA00h	I2C control register	0000h
I2CDR	EA0Ch	I2C data register	0000h
I2COAR1	EA08h	I2C own address register 1	0000h
I2COAR2	EA0Ah	I2C own address register 2	0000h
I2CSR1	EA02h	I2C status register 1	0000h
I2CSR2	EA04h	I2C status register 2	0000h
RTCAH	ED14h	RTC alarm register high byte	XXXXh
RTCAL	ED12h	RTC alarm register low byte	XXXXh
RTCCON	ED00H	RTC control register	000Xh
RTCDH	ED0Ch	RTC divider counter high byte	XXXXh
RTCDL	ED0Ah	RTC divider counter low byte	XXXXh
RTCH	ED10h	RTC programmable counter high byte	XXXXh

absolute accuracy of the A/D conversion is the deviation between the input analog value and the output digital value. It includes the following errors:

- Offset error (OFS)
- Gain error (GE)
- Quantization error
- Non-linearity error (Differential and Integral)

These four error quantities are explained below using *Figure 40*.

Offset error

Offset error is the deviation between actual and ideal A/D conversion characteristics when the digital output value changes from the minimum (zero voltage) 00 to 01 (*Figure 40*, see OFS).

Gain error

Gain error is the deviation between the actual and ideal A/D conversion characteristics when the digital output value changes from the 3FEh to the maximum 3FFh once offset error is subtracted. Gain error combined with offset error represents the so-called full-scale error (*Figure 40*, OFS + GE).

Quantization error

Quantization error is the intrinsic error of the A/D converter and is expressed as 1/2 LSB.

Non-linearity error

Non-linearity error is the deviation between actual and the best-fitting A/D conversion characteristics (see *Figure 40*):

- Differential non-linearity error is the actual step dimension versus the ideal one (1 LSB_{IDEAL}).
- Integral non-linearity error is the distance between the center of the actual step and the center of the bisector line, in the actual characteristics. Note that for integral non-linearity error, the effect of offset, gain and quantization errors is not included.

Note: Bisector characteristic is obtained drawing a line from 1/2 LSB before the first step of the real characteristic, and 1/2 LSB after the last step again of the real characteristic.

24.7.3 Total unadjusted error

The total unadjusted error specifies the maximum deviation from the ideal characteristic: The number provided in the datasheet represents the maximum error with respect to the entire characteristic. It is a combination of the offset, gain and integral linearity errors. The different errors may compensate each other depending on the relative sign of the offset and gain errors. Refer to *Figure 40*, see TUE.

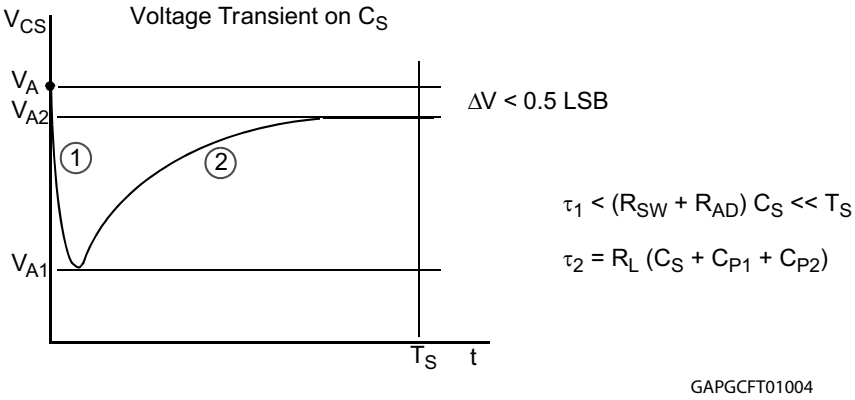
(sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the following relation:

$$V_A \cdot \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB$$

The formula above provides constraints for external network design, in particular on a resistive path.

A second aspect involving the capacitance network must be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} initially charged at the source voltage V_A (refer to the equivalent circuit reported in *Figure 41*), when the sampling phase is started (A/D switch close), a charge-sharing phenomena is installed.

Figure 42. Charge-sharing timing diagram during sampling phase



In particular two different transient periods can be distinguished (see *Figure 42*):

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is:

$$\tau_1 = (R_{SW} + R_{AD}) \cdot \frac{C_P \cdot C_S}{C_P + C_S}$$

- This relation can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

$$\tau_1 < (R_{SW} + R_{AD}) \cdot C_S \ll T_S$$

- The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to the following equation:

$$V_{A1} \cdot (C_S + C_{P1} + C_{P2}) = V_A \cdot (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

$$\tau_2 < R_L \cdot (C_S + C_{P1} + C_{P2})$$

- In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraint on R_L sizing is obtained:

$$10 \cdot \tau_2 = 10 \cdot R_L \cdot (C_S + C_{P1} + C_{P2}) \leq T_S$$

- Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). C_F being definitively bigger than C_{P1}, C_{P2} and C_S, the final voltage V_{A2} (at the end of the charge transfer transient) will then be much higher than V_{A1}. The following equation must be respected (charge balance assuming now C_S already charged at V_{A1}):

$$V_{A2}(C_S + C_{P1} + C_{P2} + C_F) = V_A \cdot C_F + V_{A1}(C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing (see *Figure 43*).

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): In conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

the accuracy error introduced by the switched capacitance equivalent resistance is in this case:

$$R_{EQ} = \frac{1}{f_C C_S} = 10M\Omega$$

So the error due to the voltage partitioning between the real resistive path and C_S is less then half a count (considering the worst case when V_A = 5V):

$$V_A \cdot \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} = 2.35mV < \frac{1}{2}LSB$$

The other condition to be verified is if the time constants of the transients are really and significantly shorter than the sampling period duration T_S:

$$\tau_1 = (R_{SW} + R_{AD}) \cdot C_S = 2.8ns \quad T_S = 1\mu s$$

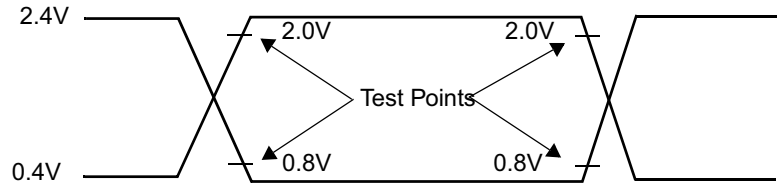
$$10\,\tau_2 = 10\,R_L(C_S + C_{P1} + C_{P2}) = 290ns \quad T_S = 1\mu s$$

For the complete set of parameters characterizing the ST10F273M A/D converter equivalent circuit, refer to *Section 24.7: A/D converter characteristics on page 139*.

24.8 AC characteristics

24.8.1 Test waveforms

Figure 44. Input/output waveforms



AC inputs during testing are driven at 2.4V for a logic '1' and 0.4V for a logic '0'.
Timing measurements are made at V_{IH} Min. for a logic '1' and V_{IL} max for a logic '0'.

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Table 64. PLL characteristics (V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = -40°C to +125°C)

Symbol	Parameter	Conditions	Value		Unit
			Min	Max	
T_{PSUP}	PLL start-up time(1)	Stable V_{DD} and reference clock	–	300	µs
T_{LOCK}	PLL lock-in time	Stable V_{DD} and reference clock, starting from free-running mode	–	250	
T_{JIT}	Single period jitter(1) (cycle to cycle = 2 TCL)	6 sigma time period variation (peak to peak)	-500	+500	ps
F_{free}	PLL free running frequency	Multiplication factors: 3, 4	250	2000	kHz
		Multiplication factors: 5, 8, 10	500	4000	

1. Not 100% tested, guaranteed by design characterization.

24.8.11 Main oscillator specifications

$_{DD}$ = 5V ± 10%, V_{SS} = 0V, T_A = -40 to +125°C

Table 65. Main oscillator characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
g_m	Oscillator transconductance	–	8	17	35	mA/V
V_{OSC}	Oscillation amplitude(1)	Peak to peak	–	V_{DD} – 0.4	–	V
V_{AV}	Oscillation voltage level(1)	Sine wave middle		V_{DD} / 2 – 0.25	–	
t_{STUP}	Oscillator start-up time(1)	Stable V_{DD} - crystal		3	4	ms
		Stable V_{DD} - resonator		2	3	

1. Not 100% tested, guaranteed by design characterization.

Figure 48. Crystal oscillator and resonator connection diagram

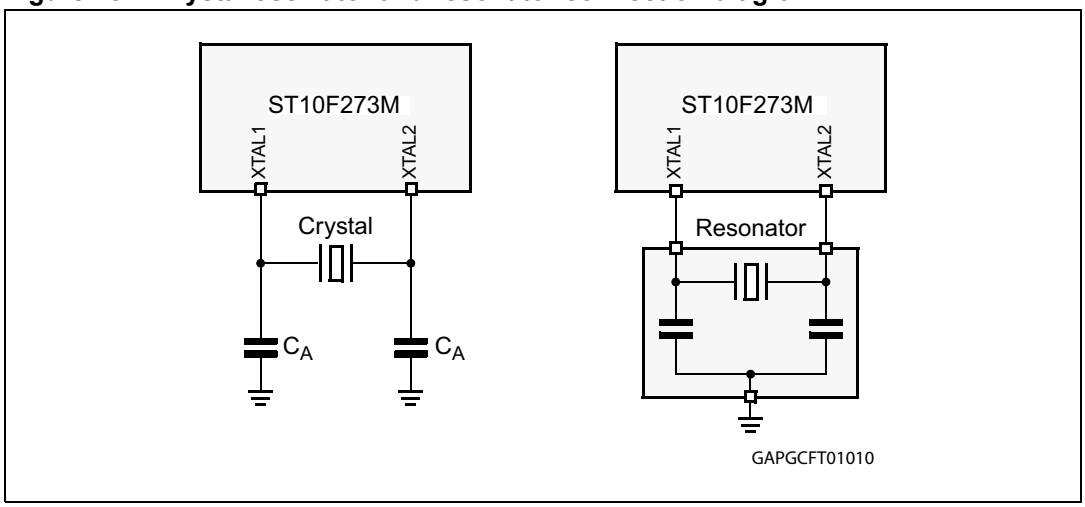

Figure 64. PQFP144 package dimensions