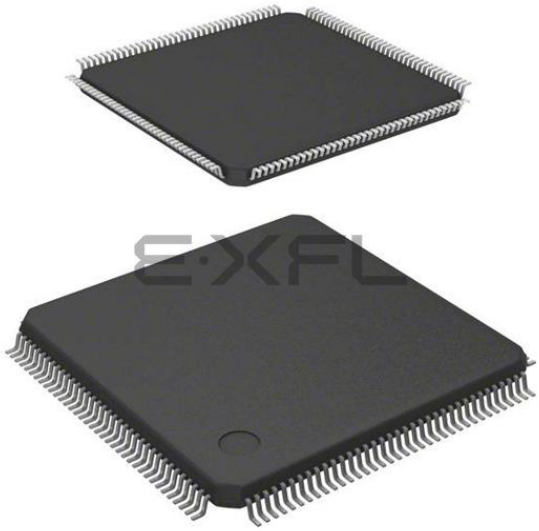

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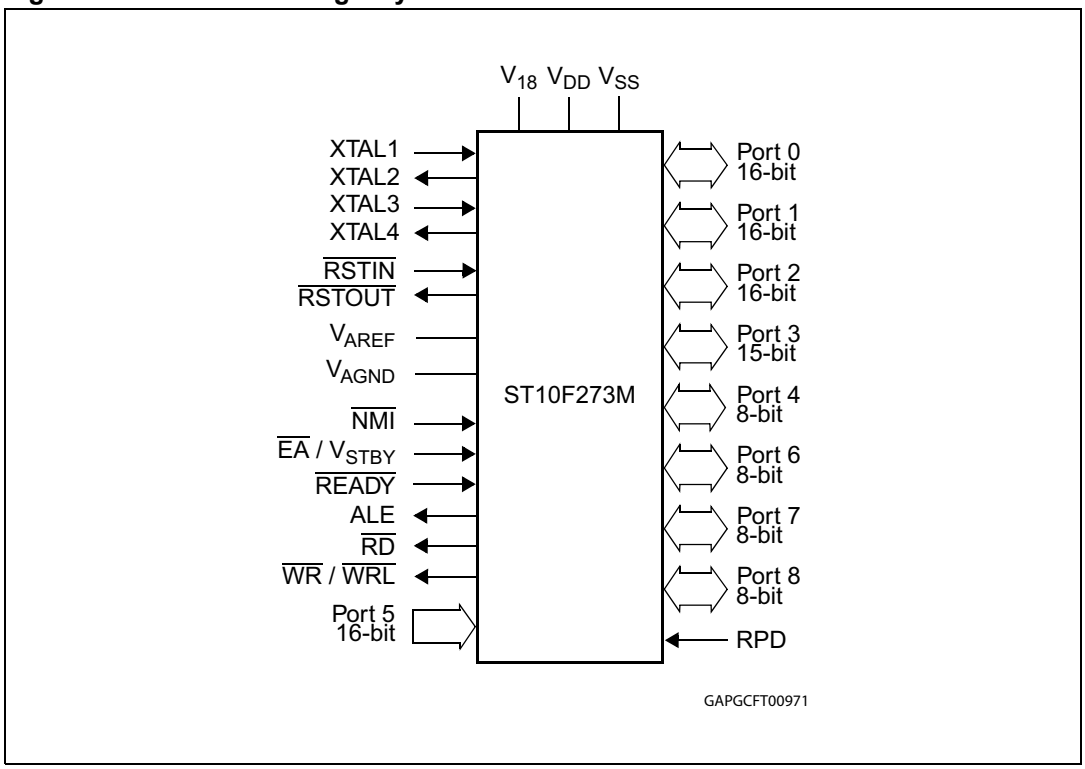
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ST10
Core Size	16-Bit
Speed	40MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f273m-4t3

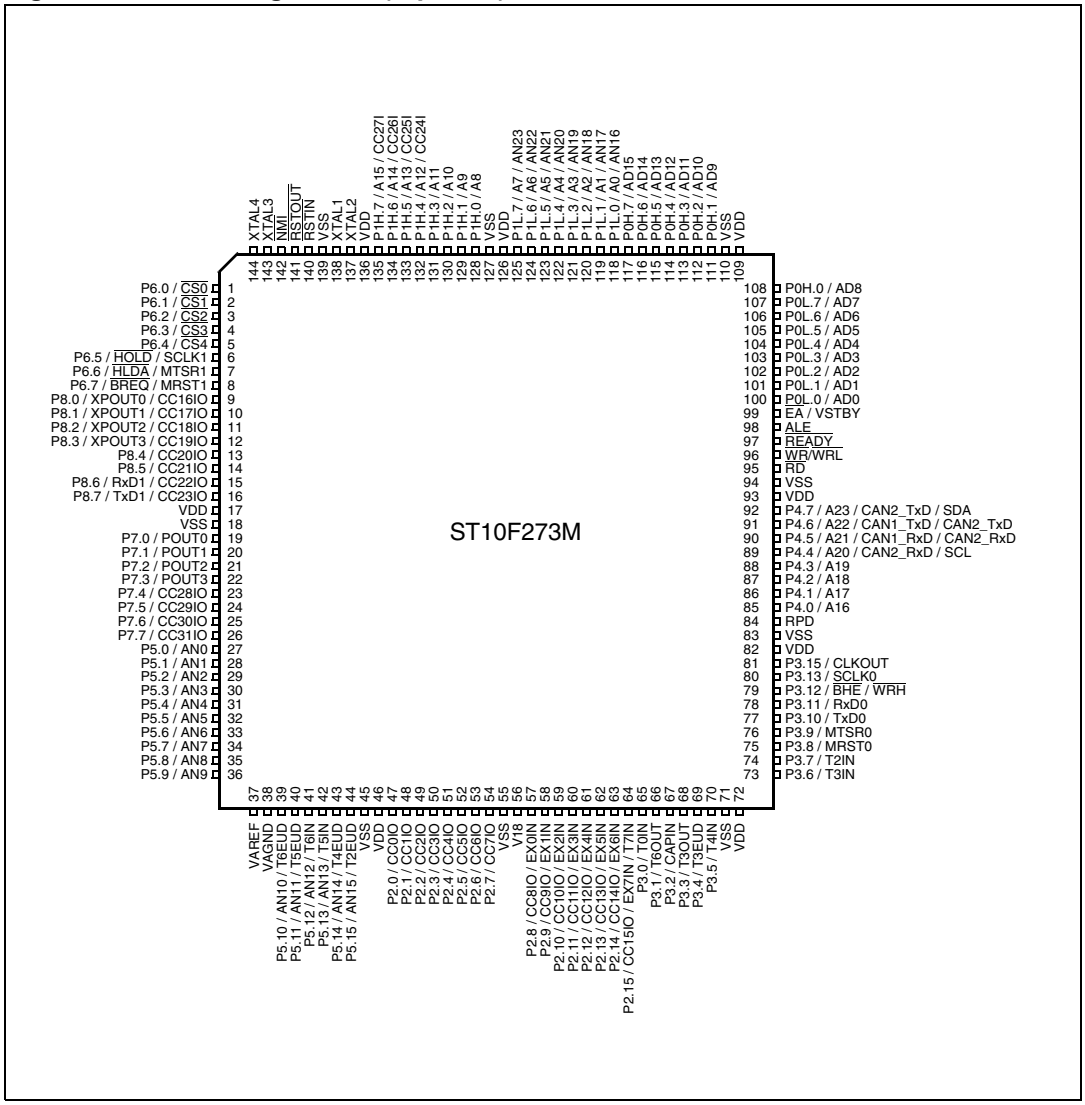
Contents

Figure 1. ST10F273M logic symbol



2 Pin data

Figure 2. Pin configuration (top view)



PWM1: Address range 00'EC00h - 00'ECFFh is reserved for the PWM1 Module access. The PWM1 is enabled by setting XPEN bit 2 of the SYSCON register and bit 6 of the XPERCON register. Accesses to the PWM1 Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two waitstates give an access time of 100ns at 40 MHz CPU clock. No tristate waitstate is used. Only word access is allowed.

ASC1: Address range 00'E900h - 00'E9FFh is reserved for the ASC1 Module access. The ASC1 is enabled by setting XPEN bit 2 of the SYSCON register and bit 7 of the XPERCON register. Accesses to the ASC1 Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two waitstates give an access time of 100ns at 40 MHz CPU clock. No tristate waitstate is used.

SSC1: Address range 00'E800h - 00'E8FFh is reserved for the SSC1 Module access. The SSC1 is enabled by setting XPEN bit 2 of the SYSCON register and bit 8 of the XPERCON register. Accesses to the SSC1 Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two waitstates give an access time of 100ns at 40 MHz CPU clock. No tristate waitstate is used.

I2C: Address range 00'EA00h - 00'EAFFh is reserved for the I2C Module access. The I2C is enabled by setting XPEN bit 2 of the SYSCON register and bit 9 of the XPERCON register. Accesses to the I2C Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two waitstates give an access time of 100ns at 40 MHz CPU clock. No tristate waitstate is used.

X-Miscellaneous: Address range 00'EB00h - 00'EBFFh is reserved for the access to a set of XBUS additional features. They are enabled by setting XPEN bit 2 of the SYSCON register and bit 10 of the XPERCON register. Accesses to this additional features use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two waitstates give an access time of 100ns at 40 MHz CPU clock. No tristate waitstate is used. The following set of features are provided:

- CLKOUT programmable divider
- XBUS interrupt management registers
- ADC multiplexing on P1L register
- Port1L digital disable register for extra ADC channels
- CAN2 multiplexing on P4.5/P4.6
- CAN1-2 main clock prescaler
- Main Voltage Regulator disable for power-down mode
- TTL / CMOS threshold selection for Port0, Port1 and Port5

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16 Mbytes of external memory can be connected to the microcontroller.

Visibility of XBUS peripherals

In order to keep the ST10F273M compatible with the ST10F168 / ST10F269, the XBUS peripherals can be selected to be visible on the external address / data bus. Different bits for X-Peripheral enabling in XPERCON register must be set. If these bits are cleared before the global enabling with XPEN bit in SYSCON register, the corresponding address space, port pins and interrupts are not occupied by the peripherals, thus the peripheral is not visible and not available. Refer to *Chapter 23: Register set on page 115*.

The Addresses from 0x0E 0000 to 0x0E FFFF are reserved for the Control Register Interface and other internal service memory space used by the Flash Program/Erase controller.

The following tables show the memory mapping of the Flash when it is accessed in read mode (*Table 4: Flash module sectorization (read operations)*), and when accessed in write or erase mode (*Table 5: Flash module sectorization (write operations, or ROMS1 = '1')*).

Note: With this second mapping, the first four sectors are remapped into code segment 1 (same as obtained setting bit ROMS1 in SYSCON register).

Table 4. Flash module sectorization (read operations)

Bank	Description	Addresses	Size (bytes)
B0	Bank 0 Flash 0 (B0F0)	0x00 0000 - 0x00 1FFF	8 K
	Bank 0 Flash 1 (B0F1)	0x00 2000 - 0x00 3FFF	8 K
	Bank 0 Flash 2 (B0F2)	0x00 4000 - 0x00 5FFF	8 K
	Bank 0 Flash 3 (B0F3)	0x00 6000 - 0x00 7FFF	8 K
	Bank 0 Flash 4 (B0F4)	0x01 8000 - 0x01 FFFF	32 K
	Bank 0 Flash 5 (B0F5)	0x02 0000 - 0x02 FFFF	64 K
	Bank 0 Flash 6 (B0F6)	0x03 0000 - 0x03 FFFF	64 K
	Bank 0 Flash 7 (B0F7)	0x04 0000 - 0x04 FFFF	64 K
	Bank 0 Flash 8 (B0F8)	0x05 0000 - 0x05 FFFF	64 K
	Bank 0 Flash 9 (B0F9)	0x06 0000 - 0x06 FFFF	64 K
	Bank 0 Flash 10 (B0F10 / B1F0) (1)	0x07 0000 - 0x07 FFFF	64 K
	Bank 0 Flash 11 (B0F11 / B1F1) (1)	0x08 0000 - 0x08 FFFF	64 K

1. A single bank is implemented but the last two sectors can be seen as a Bank 1 in order to maintain compatibility with the Flash Programming routines developed for the ST10F273E (based on ST10F276E). This means that the Control and Status flags for the blocks B0F10 and B0F11 are duplicated to also be accessible as blocks B1F0 and B1F1.

6.3 Alternate and selective boot mode (ABM and SBM)

6.3.1 Activation of the ABM and SBM

Alternate boot is activated with the combination ‘01’ on Port0L[5..4] at the rising edge of $\overline{\text{RSTIN}}$.

6.3.2 User mode signature integrity check

The behavior of the Selective Boot mode is based on the computing of a signature between the content of two memory locations and a comparison with a reference signature. This requires that users who use Selective Boot have reserved and programmed the Flash memory locations.

6.3.3 Selective boot mode

When the user signature is not correct, instead of executing the Standard Bootstrap Loader (triggered by P0L.4 low at reset), additional check is made.

Depending on the value at the User key location, the following behavior occurs:

- A jump is performed to the Standard Bootstrap Loader
- Only UART is enabled for bootstrapping
- Only CAN1 is enabled for bootstrapping
- The device enters an infinite loop

Table 28. Standard instruction set summary (continued)

Mnemonic	Description	Bytes
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software Reset	4
IDLE	Enter Idle mode	4
PWRDN	Enter Power-down mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT	Disable Watchdog Timer	4
EINIT	Signify End-of-Initialization on RSTOUT-pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4
NOP	Null operation	2

7.3 MAC co-processor specific instructions

Table 29 lists the MAC instructions of the ST10F273M. The detailed description of each instruction can be found in the *ST10 Family Programming Manual*. Note that all MAC instructions are encoded on 4 bytes.

Table 29. MAC instruction set summary

Mnemonic	Description
CoABS	Absolute value of the accumulator
CoADD(2)	Addition
CoASHR(rnd)	Accumulator arithmetic shift right & optional round
CoCMP	Compare accumulator with operands
CoLOAD(-,2)	Load accumulator with operands
CoMAC(R,u,s,-,rnd)	(Un)signed/(Un)Signed Multiply-Accumulate & Optional Round
CoMACM(R)(u,s,-,rnd)	(Un)Signed/(Un)signed multiply-accumulate with parallel data move & optional round
CoMAX / CoMIN	maximum / minimum of operands and accumulator
CoMOV	Memory to memory move
CoMUL(u,s,-,rnd)	(Un)signed/(Un)signed multiply & optional round
CoNEG(rnd)	Negate accumulator & optional round
CoNOP	No-operation
CoRND	Round accumulator
CoSHL / CoSHR	Accumulator logical shift left / right
CoSTORE	Store a MAC unit register
CoSUB(2,R)	Subtraction

10 Capture / compare (CAPCOM) units

The ST10F273M has two 16-channel CAPCOM units which support generation and control of timing sequences on up to 32 channels with a maximum resolution of 200ns at 40 MHz CPU clock.

The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), digital to analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2.

This provides a wide range of variation for the timer period and resolution and allows precise adjustments to application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Each of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare functions. Each of the 32 registers has one associated port pin which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (captured) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated.

Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture / compare register, specific actions will be taken based on the selected compare mode.

The input frequencies f_{Tx}, for the timer input selector Tx, are determined as a function of the CPU clocks. The timer input frequencies, resolution and periods which result from the selected prescaler option in TxI when using a 40 MHz CPU clock are listed in *Table 34*.

The numbers for the timer periods are based on a reload value of 0000h. Note that some numbers may be rounded off to three significant figures.

Table 33. Compare modes

Compare modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated

This is done by setting or clearing the direction control bit DPx.y of the pin before enabling the alternate function.

There are port lines, however, where the direction of the port line is switched automatically.

For instance, in the multiplexed external bus modes of PORT0, the direction must be switched several times for an instruction fetch in order to output the addresses and to input the data.

Obviously, this cannot be done through instructions. In these cases, the direction of the port line is switched automatically by hardware if the alternate function of such a pin is enabled.

To determine the appropriate level of the port output latches, check how the alternate data output is combined with the respective port latch output.

There is one basic structure for all port lines with only an alternate input function. Port lines with only an alternate output function, however, have different structures due to the way the direction of the pin is switched and depending on whether the pin is accessible by the user software or not in the alternate function mode.

All port lines that are not used for these alternate functions may be used as general purpose I/O lines.

register. The data can be transferred to the RAM by interrupt software management or using the PEC data transfer.

- **Wait for ADDAT read mode**: When using continuous modes, in order to avoid to overwrite the result of the current conversion by the next one, the ADWR bit of ADCON control register must be activated. Then, until the ADDAT register is read, the new result is stored in a temporary buffer and the conversion is on hold.
- **Channel injection mode**: When using continuous modes, a selected channel can be converted in between without changing the current operating mode. The 10-bit data of the conversion are stored in ADRES field of ADDAT2. The current continuous mode remains active after the single conversion is completed.

A full calibration sequence is performed after a reset. This full calibration lasts up to 40630 CPU clock cycles. During this time, the busy flag ADBSY is set to indicate the operation. It compensates the capacitance mismatch, so the calibration procedure does not need any update during normal operation.

No conversion can be performed during this time: The bit ADBSY shall be polled to verify when the calibration is over, and the module is able to start a conversion.

17 CAN modules

The two integrated CAN modules (CAN1 and CAN2) are identical and handle the completely autonomous transmission and reception of CAN frames according to the CAN specification V2.0 part B (active). It is based on the C-CAN specification.

Each on-chip CAN module can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Because of duplication of the CAN controllers, the following adjustments are to be considered:

- Same internal register addresses of both CAN controllers, but with base addresses differing in address bit A8; separate chip select for each CAN module. Refer to *Section 4: Memory organization on page 21*.
- The CAN1 transmit line (CAN1_TxD) is the alternate function of the Port P4.6 pin and the receive line (CAN1_RxD) is the alternate function of the Port P4.5 pin.
- The CAN2 transmit line (CAN2_TxD) is the alternate function of the Port P4.7 pin and the receive line (CAN2_RxD) is the alternate function of the Port P4.4 pin.
- Interrupt request lines of the CAN1 and CAN2 modules are connected to the XBUS interrupt lines together with other X-Peripherals sharing the four vectors.
- The CAN modules must be selected with corresponding CANxEN bit of XPERCON register before the bit XPEN of SYSCON register is set.
- The reset default configuration is: CAN1 enabled, CAN2 disabled.

Note: If one or both CAN modules is used, Port 4 cannot be programmed to output all eight segment address lines. Thus, only four segment address lines can be used, reducing the external memory space to 5 Mbytes (1 Mbyte per $\overline{CS}$ line).

17.1 Configuration support

It is possible that both CAN controllers are working on the same CAN bus, supporting together up to 64 message objects. In this configuration, both receive signals and both transmit signals are linked together when using the same CAN transceiver. This configuration is especially supported by providing open drain outputs for the CAN1_Txd and CAN2_TxD signals. The open drain function is controlled with the ODP4 register for port P4: in this way it is possible to connect together P4.4 with P4.5 (receive lines) and P4.6 with P4.7 (transmit lines configured to be configured as Open-Drain).

The user may also map internally both CAN modules on the same pins P4.5 and P4.6. In this way, P4.4 and P4.7 can be used either as general purpose I/O lines, or used for I^2C interface. This is possible by setting bit CANPAR of the XMISC register. To access this register it is necessary to set bit XMISCEN of the XPERCON register and bit XPEN of the SYSCON register.

17.2 CAN bus configurations

Depending on the application, CAN bus configuration may be one single bus with a single or multiple interfaces or a multiple bus with a single or multiple interfaces. The ST10F273M can support both configurations.

booting from internal or external memory respectively. *Figure 24* and *Figure 25* report the timing of a typical synchronous Long Reset, again when booting from internal or external memory.

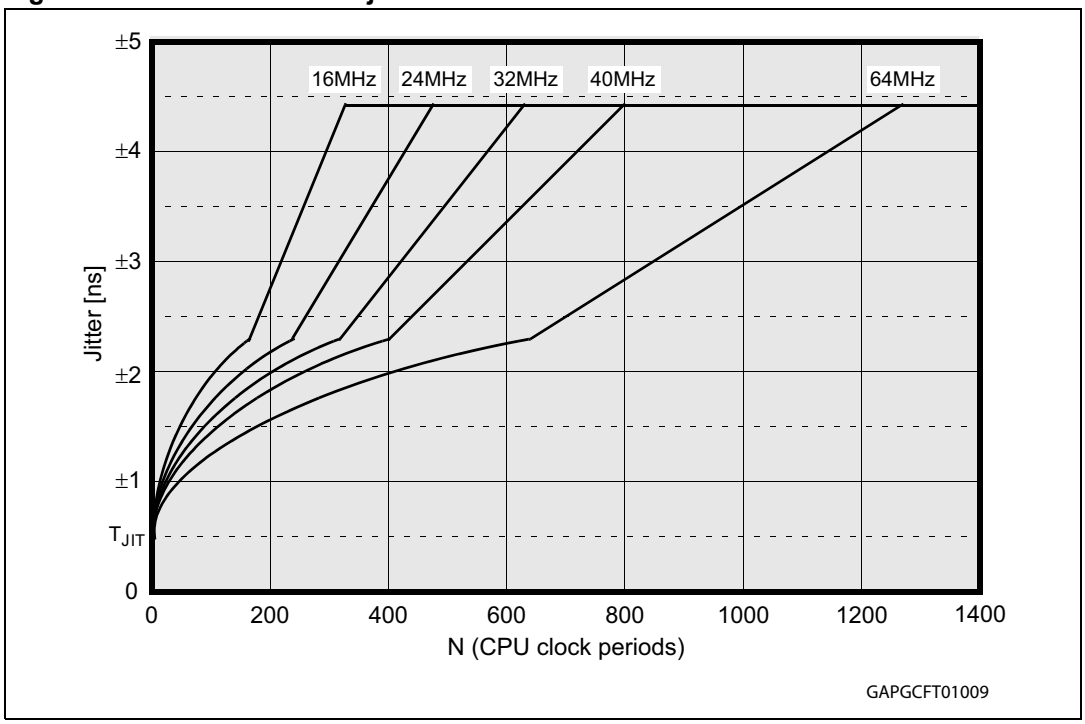
Synchronous reset and RPD pin

Whenever the $\overline{\text{RSTIN}}$ pin is pulled low (by external hardware or as a consequence of a Bidirectional reset), the RPD internal weak pull-down is activated. The external capacitance (if any) on RPD pin is slowly discharged through the internal weak pull-down. If the voltage level on RPD pin reaches the input low threshold (around 2.5V), the reset event becomes immediately asynchronous. In case of hardware reset (short or long) the situation goes immediately to the one illustrated in *Figure 20*. There is no effect if RPD comes again above the input threshold: the asynchronous reset is completed coherently. To grant the normal completion of a synchronous reset, the value of the capacitance shall be big enough to maintain the voltage on RPD pin sufficient high along the duration of the internal reset sequence.

For a Software or Watchdog reset events, an active synchronous reset is completed regardless of the RPD status.

It is important to highlight that the signal that makes RPD status transparent under reset is the internal $\overline{\text{RSTF}}$ (after the noise filter).

Figure 47. ST10F273M PLL jitter



24.8.10 PLL lock / unlock

During normal operation, if the PLL gets unlocked for any reason, an interrupt request to the CPU is generated, and the reference clock (oscillator) is automatically disconnected from the PLL input: in this way, the PLL goes into free-running mode, providing the system with a backup clock signal (free running frequency f_{free}). This feature allows to recover from a crystal failure occurrence without risking to go into an undefined configuration: The system is provided with a clock allowing the execution of the PLL unlock interrupt routine in a safe mode.

The path between reference clock and PLL input can be restored only by a hardware reset, or by a bidirectional software or watchdog reset event that forces the $\overline{\text{RSTIN}}$ pin low.

Note: The external RC circuit on $\overline{\text{RSTIN}}$ pin shall be properly sized in order to extend the duration of the low pulse to grant the PLL gets locked before the level at $\overline{\text{RSTIN}}$ pin is recognized high: bidirectional reset internally drives $\overline{\text{RSTIN}}$ pin low for just 1024 TCL (definitively not sufficient to get the PLL locked starting from free-running mode).

Table 68. Minimum values of negative resistance (module) for 32 kHz oscillator

Frequency	C_A = 6pF	C_A = 12pF	C_A = 15pF	C_A = 18pF	C_A = 22pF	C_A = 27pF	C_A = 33pF
32 kHz	-	-	-	-	150 kΩ	120 kΩ	90 kΩ

The given values of C_A do not include the stray capacitance of the package and of the printed circuit board: The negative resistance values are calculated assuming additional 5pF to the values in the table. The crystal shunt capacitance (C_0) and the package capacitance between XTAL3 and XTAL4 pins is globally assumed equal to 4pF. The external resistance between XTAL3 and XTAL4 is not necessary, since already present on the silicon.

Warning: Direct driving on XTAL3 pin is not supported. Always use a 32 kHz crystal oscillator.

24.8.13 External clock drive XTAL1

When Direct Drive configuration is selected during reset, it is possible to drive the CPU clock directly from the XTAL1 pin, without particular restrictions on the maximum frequency, since the on-chip oscillator amplifier is bypassed. The speed limit is imposed by internal logic that targets a maximum CPU frequency of 40 MHz.

In all other clock configurations (Direct Drive with Prescaler or PLL usage) the on-chip oscillator amplifier is not bypassed, so it determines the input clock speed limit. Then, when the on-chip oscillator is enabled it is forbidden to use any external clock source different from crystal or ceramic resonator.

Table 69. External clock drive XTAL1 timing

Parameter	Symbol		Direct drive $f_{CPU} = f_{XTAL}$		Direct drive with prescaler $f_{CPU} = f_{XTAL} / 2$		PLL usage $f_{CPU} = f_{XTAL} \times F$		Unit
			Min	Max	Min	Max	Min	Max	
XTAL1 period(1)(2)	t_{OSC}	SR	25	–	10	250	100	250	ns
High time(3)	t_1	SR	6	–	3	–	6	–	
Low time(3)	t_2	SR	6	–	3	–	6	–	
Rise time(3)	t_3	SR	–	2	–	2	–	2	
Fall time(3)	t_4	SR	–	2	–	2	–	2	

1. The minimum value for the XTAL1 signal period shall be considered as the theoretical minimum. The real minimum value depends on the duty cycle of the input clock signal.
2. 4 to 12 MHz is the input frequency range when using an external clock source. 40 MHz can be applied with an external clock source only when Direct Drive mode is selected: in this case, the oscillator amplifier is bypassed so it does not limit the input frequency.
3. The input clock signal must reach the defined levels V_{IL2} and V_{IH2}.

Table 71. Multiplexed bus timings (continued)

Symbol		Parameter	f_{CPU} = 40 MHz TCL = 12.5ns		Variable CPU clock 1/2 TCL = 1 to 40 MHz		Unit
			Min	Max	Min	Max	
t_{45}	CC	Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	–	14	–	TCL + 1.5	ns
t_{46}	SR	$\overline{RdCS}$ to Valid Data in (with RW delay)	–	4 + t_C	–	2TCL - 21 + t_C	ns
t_{47}	SR	$\overline{RdCS}$ to Valid Data in (no RW delay)	–	16.5 + t_C	–	3TCL - 21 + t_C	ns
t_{48}	CC	$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW delay)	15.5 + t_C	–	2TCL - 9.5 + t_C	–	ns
t_{49}	CC	$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW delay)	28 + t_C	–	3TCL - 9.5 + t_C	–	ns
t_{50}	CC	Data valid to $\overline{WrCS}$	10 + t_C	–	2TCL - 15 + t_C	–	ns
t_{51}	SR	Data hold after $\overline{RdCS}$	0	–	0	–	ns
t_{52}	SR	Data float after $\overline{RdCS}$	–	16.5 + t_F	–	2TCL - 8.5 + t_F	ns
t_{54}	CC	Address hold after $\overline{RdCS}$, $\overline{WrCS}$	6 + t_F	–	2TCL - 19 + t_F	–	ns
t_{56}	CC	Data hold after $\overline{WrCS}$	6 + t_F	–	2TCL - 19 + t_F	–	ns

Figure 54. External memory cycle: multiplexed bus, with/ without read/ write delay, extended ALE, read/ write chip select