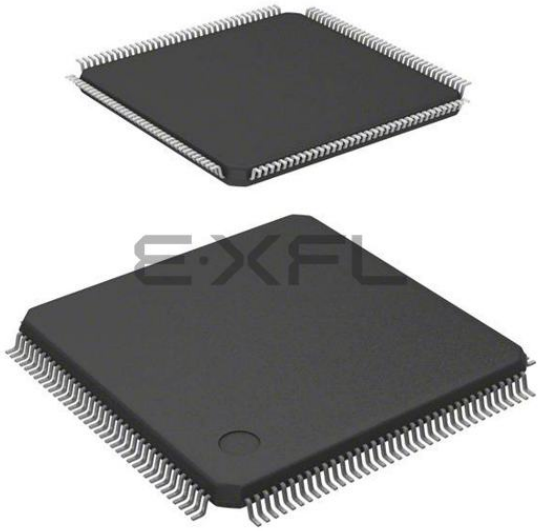

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	40MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f273m-4tr3

Contents

Table 1. Pin description (continued)

Symbol	Pin	Type	Function		
P3.0 - P3.5 P3.6 - P3.13, P3.15	65-70, 73-80, 81	I/O I/O I/O	15-bit (P3.14 is missing) bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 3 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or CMOS). The following Port 3 pins have alternate functions:		
	65	I	P3.0	T0IN	CAPCOM1: timer T0 count input
	66	O	P3.1	T6OUT	GPT2: timer T6 toggle latch output
	67	I	P3.2	CAPIN	GPT2: register CAPREL capture input
	68	O	P3.3	T3OUT	GPT1: timer T3 toggle latch output
	69	I	P3.4	T3EUD	GPT1: timer T3 external up/down control input
	70	I	P3.5	T4IN	GPT1; timer T4 input for count/gate/reload/capture
	73	I	P3.6	T3IN	GPT1: timer T3 count/gate input
	74	I	P3.7	T2IN	GPT1: timer T2 input for count/gate/reload / capture
	75	I/O	P3.8	MRST0	SSC0: master-receiver/slave-transmitter I/O
	76	I/O	P3.9	MTSR0	SSC0: master-transmitter/slave-receiver O/I
	77	O	P3.10	TxD0	ASC0: clock / data output (asynchronous/synchronous)
	78	I/O	P3.11	RxD0	ASC0: data input (asynchronous) or I/O (synchronous)
	79	O	P3.12	$\overline{BHE}$	External memory high byte enable signal
				$\overline{WRH}$	External memory high byte write strobe
	80	I/O	P3.13	SCLK0	SSC0: master clock output / slave clock input
	81	O	P3.15	CLKOUT	System clock output (programmable divider on CPU clock)

Table 1. Pin description (continued)

Symbol	Pin	Type	Function		
P4.0 –P4.7	85-92	I/O	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. The input threshold is selectable (TTL or CMOS). Port 4.4, 4.5, 4.6 and 4.7 outputs can be configured as push-pull or open drain drivers. In case of an external bus configuration, Port 4 can be used to output the segment address lines:		
	85	O	P4.0	A16	Segment address line
	86	O	P4.1	A17	Segment address line
	87	O	P4.2	A18	Segment address line
	88	O	P4.3	A19	Segment address line
	89	O	P4.4	A20	Segment address line
		I		CAN2_RxD	CAN2: receive data input
		I/O		SCL	I^2C Interface: serial clock
	90	O	P4.5	A21	Segment address line
		I		CAN1_RxD	CAN1: receive data input
		I		CAN2_RxD	CAN2: receive data input
	91	O	P4.6	A22	Segment address line
		O		CAN1_TxD	CAN1: transmit data output
		O		CAN2_TxD	CAN2: transmit data output
	92	O	P4.7	A23	Most significant segment address line
		O		CAN2_TxD	CAN2: transmit data output
		I/O		SDA	I^2C Interface: serial data
$\overline{RD}$	95	O	External memory read strobe. $\overline{RD}$ is activated for every external instruction or data read access.		
$\overline{WR}/\overline{WRL}$	96	O	External memory write strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$ mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in the SYSCON register for mode selection.		
READY/ $\overline{READY}$	97	I	Ready input. The active level is programmable. When the ready function is enabled, the selected inactive level at this pin, during an external memory access, will force the insertion of waitstate cycles until the pin returns to the selected active level.		
ALE	98	O	Address latch enable output. In case of use of external addressing or of multiplexed mode, this signal is the latch command of the address lines.		

Table 1. Pin description (continued)

Symbol	Pin	Type	Function	
XTAL1	138	I	XTAL1	Main oscillator amplifier circuit and/or external clock input.
XTAL2	137	O	XTAL2	Main oscillator amplifier circuit output.
			To clock the device from an external source, drive XTAL1 while leaving XTAL2 unconnected. Minimum and maximum high / low and rise / fall times specified in the AC Characteristics must be observed.	
XTAL3	143	I	XTAL3	32 kHz oscillator amplifier circuit input
XTAL4	144	O	XTAL4	32 kHz oscillator amplifier circuit output
			When 32 kHz oscillator amplifier is not used, to avoid spurious consumption, XTAL3 shall be tied to ground while XTAL4 shall be left open. Besides, bit OFF32 in RTCCON register shall be set. 32 kHz oscillator can only be driven by an external crystal, and not by a different clock source.	
$\overline{\text{RSTIN}}$	140	I	Reset Input with CMOS Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running resets the ST10F273M. An internal pull-up resistor permits power-on reset using only a capacitor connected to V_{SS}. In bidirectional reset mode (enabled by setting bit BDRSTEN in SYSCON register), the $\overline{\text{RSTIN}}$ line is pulled low for the duration of the internal reset sequence.	
$\overline{\text{RSTOUT}}$	141	O	Internal Reset Indication Output. This pin is driven to a low level during hardware, software or watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.	
$\overline{\text{NMI}}$	142	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. If bit PWDCFG = '0' in SYSCON register, when the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the ST10F273M to go into power down mode. If $\overline{\text{NMI}}$ is high and PWDCFG = '0', when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.	
V_{AREF}	37	-	A/D converter reference voltage and analog supply	
V_{AGND}	38	-	A/D converter reference and analog ground	
RPD	84	-	Timing pin for the return from interruptible power down mode and synchronous / asynchronous reset selection.	
V_{DD}	17, 46, 72,82,93, 109, 126, 136	-	Digital supply voltage = + 5V during normal operation, idle and power down modes. It can be turned off when Standby RAM mode is selected.	
V_{SS}	18,45, 55,71, 83,94, 110, 127, 139	-	Digital ground	
V_{18}	56	-	1.8V decoupling pin: a decoupling capacitor (typical value of 10nF, max 100nF) must be connected between this pin and nearest V_{SS} pin.	

IRAM: 2 Kbytes of on-chip internal RAM (dual-port) is provided as a storage for data, system stack, general purpose register banks and code. A register bank is 16 Wordwide (R0 to R15) and / or Bytewide (RL0, RH0, …, RL7, RH7) general purpose registers group.

XRAM: 34 Kbytes of on-chip extension RAM (single port XRAM) is provided as a storage for data, user stack and code.
The XRAM is divided into two areas, the first 2 Kbytes named XRAM1 and the second 32 Kbytes named XRAM2, connected to the internal XBUS and are accessed like an external memory in 16-bit demultiplexed bus-mode without wait state or read/write delay (50ns access at 40 MHz CPU clock). Byte and Word accesses are allowed.

The XRAM1 address range is 00'E000h - 00'E7FFh if XPEN (bit 2 of SYSCON register), and XRAM1EN (bit 2 of XPERCON register) are set.
If XRAM1EN or XPEN is cleared, then any access in the address range 00'E000h - 00'E7FFh will be directed to external memory interface, using the BUSCONx register corresponding to address matching ADDRSELx register.

The XRAM2 address range is F'0000h - F'7FFFFh if XPEN (bit 2 of SYSCON register), and XRAM2EN (bit 3 of XPERCON register) are set.
If bit XPEN is cleared, then any access in the address range programmed for XRAM2 will be directed to external memory interface, using the BUSCONx register corresponding to address matching ADDRSELx register.

The 16 kbytes lower portion of the XRAM2 (address range F'0000h - F'3FFFFh) represents also the Standby RAM, which can be maintained biased through $\overline{EA}$ / V_{STBY} pin when the main supply V_{DD} is turned off.
As the XRAM appears like external memory, it cannot be used as system stack or as register banks. The XRAM is not provided for single bit storage and therefore is not bit addressable.

SFR/ESFR: 1024 bytes (2 x 512 bytes) of address space is reserved for the special function register (SFR) areas. SFRs are Wordwide registers which are used to control and to monitor the function of the different on-chip units.

CAN1: Address range 00'EF00h - 00'EFFFh is reserved for the CAN1 Module access. The CAN1 is enabled by setting XPEN bit 2 of the SYSCON register and by setting CAN1EN bit 0 of the XPERCON register. Accesses to the CAN Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two wait states give an access time of 100ns at 40 MHz CPU clock. No tri-state wait states are used.

CAN2: Address range 00'EE00h - 00'EEFFh is reserved for the CAN2 Module access. The CAN2 is enabled by setting XPEN bit 2 of the SYSCON register and by setting CAN2EN bit 1 of the new XPERCON register. Accesses to the CAN Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two wait states give an access time of 100ns at 40 MHz CPU clock. No tri-state wait states are used.

Note: If one or the two CAN modules are used, Port 4 cannot be programmed to output all eight segment address lines. Thus, only four segment address lines can be used, reducing the external memory space to 5 Mbytes (1 Mbyte per CS line).

RTC: Address range 00'ED00h - 00'EDFFh is reserved for the RTC Module access. The RTC is enabled by setting XPEN bit 2 of the SYSCON register and bit 4 of the XPERCON register. Accesses to the RTC Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two waitstates give an access time of 100ns at 40 MHz CPU clock. No tristate waitstate is used.

PWM1: Address range 00'EC00h - 00'ECFFh is reserved for the PWM1 Module access. The PWM1 is enabled by setting XPEN bit 2 of the SYSCON register and bit 6 of the XPERCON register. Accesses to the PWM1 Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two waitstates give an access time of 100ns at 40 MHz CPU clock. No tristate waitstate is used. Only word access is allowed.

ASC1: Address range 00'E900h - 00'E9FFh is reserved for the ASC1 Module access. The ASC1 is enabled by setting XPEN bit 2 of the SYSCON register and bit 7 of the XPERCON register. Accesses to the ASC1 Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two waitstates give an access time of 100ns at 40 MHz CPU clock. No tristate waitstate is used.

SSC1: Address range 00'E800h - 00'E8FFh is reserved for the SSC1 Module access. The SSC1 is enabled by setting XPEN bit 2 of the SYSCON register and bit 8 of the XPERCON register. Accesses to the SSC1 Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two waitstates give an access time of 100ns at 40 MHz CPU clock. No tristate waitstate is used.

I2C: Address range 00'EA00h - 00'EAFFh is reserved for the I2C Module access. The I2C is enabled by setting XPEN bit 2 of the SYSCON register and bit 9 of the XPERCON register. Accesses to the I2C Module use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two waitstates give an access time of 100ns at 40 MHz CPU clock. No tristate waitstate is used.

X-Miscellaneous: Address range 00'EB00h - 00'EBFFh is reserved for the access to a set of XBUS additional features. They are enabled by setting XPEN bit 2 of the SYSCON register and bit 10 of the XPERCON register. Accesses to this additional features use demultiplexed addresses and a 16-bit data bus (only word accesses are possible). Two waitstates give an access time of 100ns at 40 MHz CPU clock. No tristate waitstate is used. The following set of features are provided:

- CLKOUT programmable divider
- XBUS interrupt management registers
- ADC multiplexing on P1L register
- Port1L digital disable register for extra ADC channels
- CAN2 multiplexing on P4.5/P4.6
- CAN1-2 main clock prescaler
- Main Voltage Regulator disable for power-down mode
- TTL / CMOS threshold selection for Port0, Port1 and Port5

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16 Mbytes of external memory can be connected to the microcontroller.

Visibility of XBUS peripherals

In order to keep the ST10F273M compatible with the ST10F168 / ST10F269, the XBUS peripherals can be selected to be visible on the external address / data bus. Different bits for X-Peripheral enabling in XPERCON register must be set. If these bits are cleared before the global enabling with XPEN bit in SYSCON register, the corresponding address space, port pins and interrupts are not occupied by the peripherals, thus the peripheral is not visible and not available. Refer to *Chapter 23: Register set on page 115*.

Table 5. Flash module sectorization (write operations, or ROMS1 = '1')

Bank	Description	Addresses	Size (bytes)
B0	Bank 0 Test-Flash (B0TF)	0x00 0000 - 0x00 0FFF	4 K
	Bank 0 Flash 0 (B0F0)	0x01 0000 - 0x01 1FFF	8 K
	Bank 0 Flash 1 (B0F1)	0x01 2000 - 0x01 3FFF	8 K
	Bank 0 Flash 2 (B0F2)	0x01 4000 - 0x01 5FFF	8 K
	Bank 0 Flash 3 (B0F3)	0x01 6000 - 0x01 7FFF	32 K
	Bank 0 Flash 4 (B0F4)	0x01 8000 - 0x01 FFFF	64 K
	Bank 0 Flash 5 (B0F5)	0x02 0000 - 0x02 FFFF	64 K
	Bank 0 Flash 6 (B0F6)	0x03 0000 - 0x03 FFFF	64 K
	Bank 0 Flash 7 (B0F7)	0x04 0000 - 0x04 FFFF	64 K
	Bank 0 Flash 8 (B0F8)	0x05 0000 - 0x05 FFFF	64 K
	Bank 0 Flash 9 (B0F9)	0x06 0000 - 0x06 FFFF	64 K
	Bank 0 Flash 10 (B0F10 / B1F0) (1)	0x07 0000 - 0x07 FFFF	64 K
	Bank 0 Flash 11 (B0F11 / B1F1) (1)	0x08 0000 - 0x08 FFFF	8 K

1. A single bank is implemented but the last two sectors can be seen as a Bank 1 in order to maintain compatibility with the Flash Programming routines developed for the ST10F273E (based on ST10F276E). This means that the Control and Status flags for the blocks B0F10 and B0F11 are duplicated to also be accessible as blocks B1F0 and B1F1.

Table 5 above refers to the configuration when bit ROMS1 of SYSCON register is set.

When Bootstrap mode is entered:

- Test-Flash is seen and available for code fetches (address 0x00 0000)
- User IFlash is only available for read and write accesses
- Write accesses must be made with addresses starting in segment 1 from 0x01 0000, whatever ROMS1 bit in SYSCON value
- Read accesses are made in segment 0 or in segment 1 depending of ROMS1 value.

In Bootstrap mode, by default ROMS1 = 0, so the first 32 Kbytes of IFlash are mapped in segment 0.

Example 1:
In default configuration, to program address 0, the user must put the value 0x01 0000 in the FARL and FARH registers but to verify the content of the address 0, a read to 0x00 0000 must be performed.

The next *Table 6* shows the Control Register interface composition: This set of registers can be addressed by the CPU .

Table 7. FCR0L register description (continued)

Bit	Name	Function
5	BSY0	Bank0 Busy This bits indicate that a write operation is running in the Bank0. It is automatically set when bit WMS is set. When this bit is set every read access to the Bank0 will output invalid data (software trap 009Bh), while every write access will be ignored. At the end of the write operation or during a Program or Erase Suspend this bit is automatically reset and Flash Bank returns to read mode. After a Program or Erase Resume this bit is automatically set again.
4	LOCK	Flash registers access locked When this bit is set, it means that the access to the Flash Control Registers FCR0H/-FCR1H/L, FDR0H/L-FDR1H/L, FARH/L and FER is locked by the FPEC: any read access to the registers will output invalid data (software trap 009Bh) and any write access will be ineffective. LOCK bit is automatically set when the Flash bit WMS is set. This is the only bit the user can always access to detect the status of the Flash: once it is found low, the rest of FCR0L and all the other Flash registers are accessible by the user as well. Note that FER content can be read when LOCK is low, but its content is updated only when also BSYx bits are reset.
3:2	-	Reserved. These bits must be left to their reset value (0).
1	BSYNVR	Busy of Non-Volatile Registers This bit indicate that a write operation is running in the corresponding on “Non-volatile registers”. They are automatically set when bit WMS is set. When this bit is set every read access to the IFlash will output the value 009Bh (software trap), while every write access to the IFlash will be ignored. At the end of the write operation or during a Program Suspend this bit is automatically reset and the IFlash returns to read mode. After a Program this bit is automatically set again.
0	-	Reserved. This bit must be left to its reset value (0).

5.4.3 Flash control register 1 low (FCR1L)

The Flash Control Register 1 Low (FCR1L), together with Flash Control Register 1 High (FCR1H), is used to select the sectors to erase or during any write operation, to monitor the status of each sector and bank.

FCR1L (0x0E 0004) FCR Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				B0F 11	B0F 10	B0F 9	B0F 8	B0F 7	B0F 6	B0F 5	B0F 4	B0F 3	B0F 2	B0F 1	B0F 0
-				RS	RS	RS	RS	RS	RS	RS	RS	RS	RS	RS	RS

Table 9. FCR1L register description

Bit	Name	Function
15:12	-	Reserved. These bits must be kept to their default value (0).
11:10	B0F11 B0F10	Bank0 IFlash sector 11:10 status These bits are a copy of bits B0F10 and B0F11 in FCR1H. It is possible use these bits as well as the bits B0F10/B1F0 and B0F11/B1F1 in FCR1H. To preserve compatibility with the ST10F273E, these bits must be left at their default value '0' and the FCR1H register must be used.
9:0	B0F9 ... B0F0	Bank 0 IFlash sector 9:0 status These bits must be set during a Sector Erase operation to select the sectors to erase in Bank 0. Besides, during any erase operation, these bits are automatically set and give the status of the first 10 sectors of Bank 0 (B0F9-B0F0). The meaning of B0Fy bit for Sector y of Bank 0 is given by *Table 11: Bank (BxS) and sectors (BxFy) status bits meaning*. These bits are automatically reset at the end of a Write operation if no errors are detected.

```
FDR0L       = 0xFFFE;      /*Load Data in FDR0L for clearing PDS0*/
FCR0H      |= 0x8000;      /*Operation start*/
```

Example 4: Enable again in a permanent way Access and Debug Protection, after having disabled them.

```
FCR0H|= 0x0100;       /*Set SPR in FCR0H*/
FARL   = 0xDFBC;      /*Load Add register FNVAPR1H in FARL*/
FARH   = 0x000E;      /*Load Add register FNVAPR1H in FARH*/
FDR0H = 0xFFFE;       /*Load Data in FDR0H to clear PEN0*/
FCR0H|= 0x8000;       /*Operation start*/
```

Disable and re-enable of Access and Debug Protection in a permanent way (as shown by examples 3 and 4) can be done for a maximum of 16 times.

register was previously set by software. Note that this bit is always cleared on power-on or after a reset sequence.

Short and long synchronous reset

Once the first maximum 16 TCL are elapsed (4+12TCL), the internal reset sequence starts. It is 1024 TCL cycles long: at the end of it, and after other 8TCL the level of $\overline{\text{RSTIN}}$ is sampled (after the filter, see $\overline{\text{RSTF}}$ in the drawings): if it is already at high level, only Short Reset is flagged (refer to *Chapter 19* for details on reset flags); if it is recognized still low, the Long reset is flagged as well. The major difference between Long and Short reset is that during the Long reset, also P0(15:13) become transparent, so it is possible to change the clock options.

Warning: In case of a short pulse on $\overline{\text{RSTIN}}$ pin, and when Bidirectional reset is enabled, the $\overline{\text{RSTIN}}$ pin is held low by the internal circuitry. At the end of the 1024 TCL cycles, the $\overline{\text{RTSIN}}$ pin is released, but due to the presence of the input analog filter the internal input reset signal ($\overline{\text{RSTF}}$ in the drawings) is released later (from 50 to 500ns). This delay is in parallel with the additional 8 TCL, at the end of which the internal input reset line ($\overline{\text{RSTF}}$) is sampled, to decide if the reset event is Short or Long. In particular:

- If 8 TCL > 500ns (f_{CPU} < 8 MHz), the reset event is always recognized as Short
- If 8 TCL < 500ns (f_{CPU} > 8 MHz), the reset event could be recognized either as Short or Long, depending on the real filter delay (between 50 and 500ns) and the CPU frequency ($\overline{\text{RSTF}}$ sampled High means Short reset, $\overline{\text{RSTF}}$ sampled Low means Long reset). Note that in case a Long Reset is recognized, once the 8 TCL are elapsed, the P0(15:13) pins becomes transparent, so the system clock can be reconfigured. The port returns not transparent 3-4TCL after the internal $\overline{\text{RSTF}}$ signal becomes high.

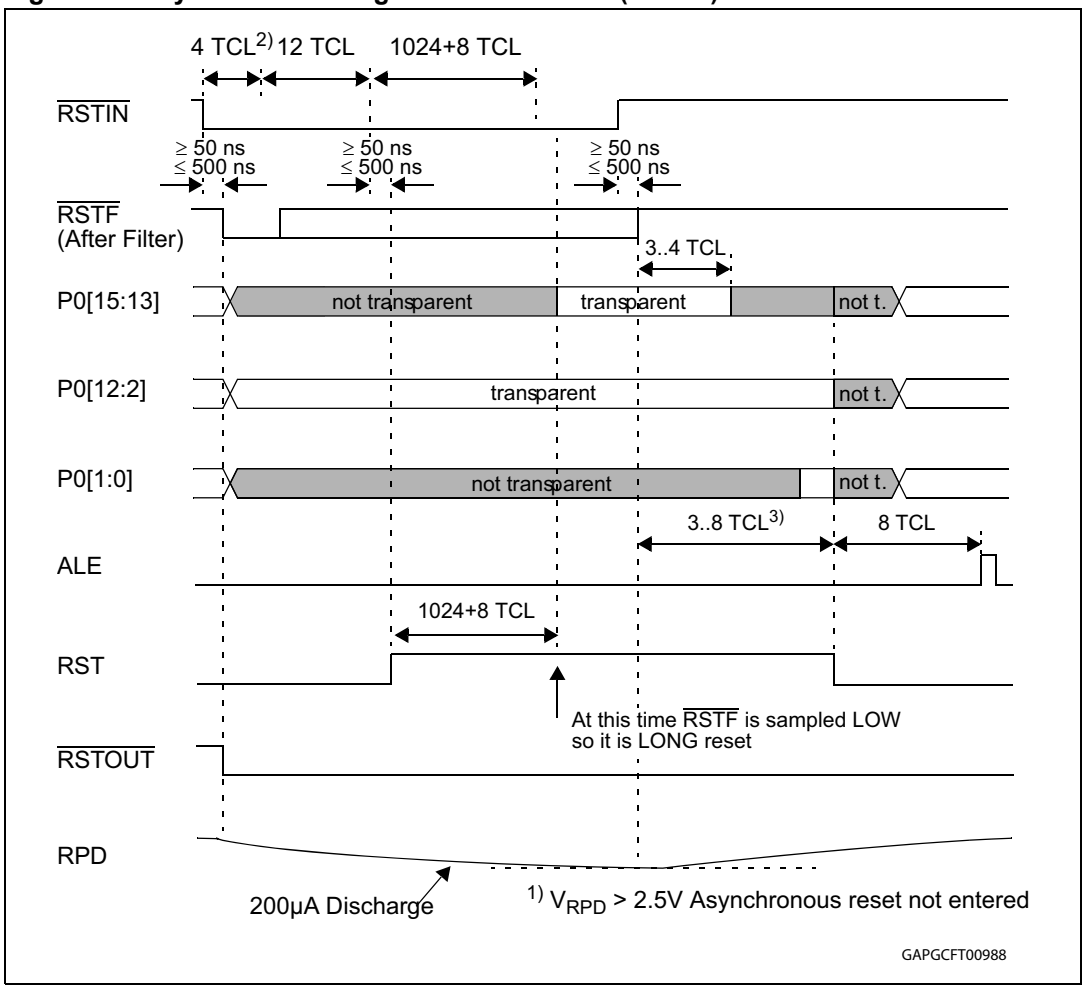
The same behavior just described, occurs also when unidirectional reset is selected and $\overline{\text{RSTIN}}$ pin is held low till the end of the internal sequence (exactly 1024TCL + max 16 TCL) and released exactly at that time.

Note: When running with CPU frequency lower than 40 MHz, the minimum valid reset pulse to be recognized by the CPU (4 TCL) could be longer than the minimum analog filter delay (50ns); so it might happen that a short reset pulse is not filtered by the analog input filter, but on the other hand it is not long enough to trigger a CPU reset (shorter than 4 TCL): this would generate a Flash reset but not a system reset. In this condition, the Flash answers always with FFFFh, which leads to an illegal opcode and consequently a trap event is generated.

Exit from synchronous reset state

The reset sequence is extended until $\overline{\text{RSTIN}}$ level becomes high. Besides, it is internally prolonged by the Flash initialization when $\overline{\text{EA}}$ = 1 (internal memory selected). Then, the code execution restarts. The system configuration is latched from Port0, and ALE, $\overline{\text{RD}}$ and $\overline{\text{WR}}$/$\overline{\text{WRL}}$ pins are driven to their inactive level. The ST10F273M starts program execution from memory location 00'0000h in code segment 0. This starting location will typically point to the general initialization routine. Timing of synchronous reset sequence are summarized in *Figure 22* and *Figure 23* where a Short Reset event is shown, with particular emphasis on the fact that it can degenerate into Long Reset: The two figures show the behavior when

Figure 25. Synchronous long hardware RESET ($\overline{EA}$ = 0)



1. If during the reset condition ($\overline{RSTIN}$ low), RPD voltage drops below the threshold voltage (about 2.5V for 5V operation), the asynchronous reset is then immediately entered.
2. Minimum $\overline{RSTIN}$ low pulse duration shall also be longer than 500ns to guarantee the pulse is not masked by the internal filter (refer to *Section 21.1*).
3. 3 to 8 TCL depending on clock source selection.

20.4 Software reset

A software reset sequence can be triggered at any time by the protected SRST (software reset) instruction. This instruction can be deliberately executed within a program, for example, to leave bootstrap loader mode, or on a hardware trap that reveals system failure.

On execution of the SRST instruction, the internal reset sequence is started. The microcontroller behavior is the same as for a synchronous short reset, except that only bits P0.12...P0.8 are latched at the end of the reset sequence, while previously latched, bits P0.7...P0.2 are cleared (that is written at '1').

A Software reset is always taken as synchronous: there is no influence on Software Reset behavior with RPD status. In case Bidirectional Reset is selected, a Software Reset event pulls $\overline{RSTIN}$ pin low: this occurs only if RPD is high; if RPD is low, $\overline{RSTIN}$ pin is not pulled low even though Bidirectional Reset is selected.

Warning: **During power-off phase, it is important that the external hardware maintains a stable ground level on RSTIN pin, without any glitch, in order to avoid spurious exiting from reset status with unstable power supply.**

21.3.2 Exiting standby mode

After the system has entered the Standby mode, the procedure to exit this mode consists of a standard Power-on sequence, with the only difference that the RAM is already powered through V_{18SB} internal reference (derived from V_{STBY} pin external voltage).

It is recommended to held the device under RESET ($\overline{RSTIN}$ pin forced low) until external V_{DD} voltage pin is stable. Even though, at the very beginning of the power-on phase, the device is maintained under reset by the internal low voltage detector circuit (implemented inside the main voltage regulator) till the internal V_{18} becomes higher than about 1.0V, there is no guaranty that the device stays under reset status if $\overline{RSTIN}$ is at high level during power ramp up. So, it is important the external hardware is able to guarantee a stable ground level on $\overline{RSTIN}$ along the power-on phase, without any temporary glitch.

The external hardware shall be responsible to drive low the $\overline{RSTIN}$ pin until the V_{DD} is stable, even though the internal LVD is active.

Once the internal Reset signal goes low, the RAM (still frozen) power supply is switched to the main V_{18}.

At this time, everything becomes stable, and the execution of the initialization routines can start: XRAM2EN bit can be set, enabling the RAM.

21.3.3 Real time clock and standby mode

When Standby mode is entered (turning off the main supply V_{DD}), the Real Time Clock counting can be maintained running in case the on-chip 32 kHz oscillator is used to provide the reference to the counter. This is not possible if the main oscillator is used as reference for the counter: Being the main oscillator powered by V_{DD}, once this is switched off, the oscillator is stopped.

21.3.4 Power reduction modes summary

The different Power reduction modes are summarized in the following *Table 45*.

Table 45. Power reduction modes summary

Mode	V_{DD}	V_{STBY}	CPU	Peripherals	RTC	Main OSC	32 kHz OSC	STBY XRAM	XRAM
Idle	on	on	off	on	off	run	off	biased	biased
	on	on	off	on	on	run	on	biased	biased
Power-down	on	on	off	off	off	off	off	biased	biased
	on	on	off	off	on	on	off	biased	biased
	on	on	off	off	on	off	on	biased	biased
Standby	off	on	off	off	off	off	off	biased	off
	off	on	off	off	on	off	on	biased	off

23 Register set

This section summarizes all registers implemented in the ST10F273M, ordered by name.

23.1 Special function registers

The following table lists all SFRs which are implemented in the ST10F273M in alphabetical order.

Bit-addressable SFRs are marked with the letter "**b**" in column "Name".

SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter "**E**" in column "Physical Address".

Table 46. List of special function registers

Name	Physical address	8-bit address	Description	Reset value
ADCIC b	FF98h	CCh	A/D converter end of conversion interrupt control register	- - 00h
ADCON b	FFA0h	D0h	A/D converter control register	0000h
ADDAT	FEA0h	50h	A/D converter result register	0000h
ADDAT2	F0A0h E	50h	A/D converter 2 result register	0000h
ADDRSEL1	FE18h	0Ch	Address select register 1	0000h
ADDRSEL2	FE1Ah	0Dh	Address select register 2	0000h
ADDRSEL3	FE1Ch	0Eh	Address select register 3	0000h
ADDRSEL4	FE1Eh	0Fh	Address select register 4	0000h
ADEIC b	FF9Ah	CDh	A/D converter overrun error interrupt control register	- - 00h
BUSCON0 b	FF0Ch	86h	Bus configuration register 0	0xx0h
BUSCON1 b	FF14h	8Ah	Bus configuration register 1	0000h
BUSCON2 b	FF16h	8Bh	Bus configuration register 2	0000h
BUSCON3 b	FF18h	8Ch	Bus configuration register 3	0000h
BUSCON4 b	FF1Ah	8Dh	Bus configuration register 4	0000h
CAPREL	FE4Ah	25h	GPT2 capture/reload register	0000h
CC0	FE80h	40h	CAPCOM register 0	0000h
CC0IC b	FF78h	BCh	CAPCOM register 0 interrupt control register	- - 00h
CC1	FE82h	41h	CAPCOM register 1	0000h
CC1IC b	FF7Ah	BDh	CAPCOM register 1 interrupt control register	- - 00h
CC2	FE84h	42h	CAPCOM register 2	0000h
CC2IC b	FF7Ch	BEh	CAPCOM register 2 interrupt control register	- - 00h
CC3	FE86h	43h	CAPCOM register 3	0000h
CC3IC b	FF7Eh	BFh	CAPCOM register 3 interrupt control register	- - 00h

Table 46. List of special function registers (continued)

Name	Physical address	8-bit address	Description	Reset value
CC4	FE88h	44h	CAPCOM register 4	0000h
CC4IC b	FF80h	C0h	CAPCOM register 4 interrupt control register	- - 00h
CC5	FE8Ah	45h	CAPCOM register 5	0000h
CC5IC b	FF82h	C1h	CAPCOM register 5 interrupt control register	- - 00h
CC6	FE8Ch	46h	CAPCOM register 6	0000h
CC6IC b	FF84h	C2h	CAPCOM register 6 interrupt control register	- - 00h
CC7	FE8Eh	47h	CAPCOM register 7	0000h
CC7IC b	FF86h	C3h	CAPCOM register 7 interrupt control register	- - 00h
CC8	FE90h	48h	CAPCOM register 8	0000h
CC8IC b	FF88h	C4h	CAPCOM register 8 interrupt control register	- - 00h
CC9	FE92h	49h	CAPCOM register 9	0000h
CC9IC b	FF8Ah	C5h	CAPCOM register 9 interrupt control register	- - 00h
CC10	FE94h	4Ah	CAPCOM register 10	0000h
CC10IC b	FF8Ch	C6h	CAPCOM register 10 interrupt control register	- - 00h
CC11	FE96h	4Bh	CAPCOM register 11	0000h
CC11IC b	FF8Eh	C7h	CAPCOM register 11 interrupt control register	- - 00h
CC12	FE98h	4Ch	CAPCOM register 12	0000h
CC12IC b	FF90h	C8h	CAPCOM register 12 interrupt control register	- - 00h
CC13	FE9Ah	4Dh	CAPCOM register 13	0000h
CC13IC b	FF92h	C9h	CAPCOM register 13 interrupt control register	- - 00h
CC14	FE9Ch	4Eh	CAPCOM register 14	0000h
CC14IC b	FF94h	CAh	CAPCOM register 14 interrupt control register	- - 00h
CC15	FE9Eh	4Fh	CAPCOM register 15	0000h
CC15IC b	FF96h	CBh	CAPCOM register 15 interrupt control register	- - 00h
CC16	FE60h	30h	CAPCOM register 16	0000h
CC16IC b	F160h E	B0h	CAPCOM register 16 interrupt control register	- - 00h
CC17	FE62h	31h	CAPCOM register 17	0000h
CC17IC b	F162h E	B1h	CAPCOM register 17 interrupt control register	- - 00h
CC18	FE64h	32h	CAPCOM register 18	0000h
CC18IC b	F164h E	B2h	CAPCOM register 18 interrupt control register	- - 00h
CC19	FE66h	33h	CAPCOM register 19	0000h
CC19IC b	F166h E	B3h	CAPCOM register 19 interrupt control register	- - 00h
CC20	FE68h	34h	CAPCOM register 20	0000h
CC20IC b	F168h E	B4h	CAPCOM register 20 interrupt control register	- - 00h

Table 46. List of special function registers (continued)

Name		Physical address		8-bit address	Description	Reset value
T1		FE52h		29h	CAPCOM timer 1 register	0000h
T1IC	b	FF9Eh		CFh	CAPCOM timer 1 interrupt control register	- - 00h
T1REL		FE56h		2Bh	CAPCOM timer 1 reload register	0000h
T2		FE40h		20h	GPT1 timer 2 register	0000h
T2CON	b	FF40h		A0h	GPT1 timer 2 control register	0000h
T2IC	b	FF60h		B0h	GPT1 timer 2 interrupt control register	- - 00h
T3		FE42h		21h	GPT1 timer 3 register	0000h
T3CON	b	FF42h		A1h	GPT1 timer 3 control register	0000h
T3IC	b	FF62h		B1h	GPT1 timer 3 interrupt control register	- - 00h
T4		FE44h		22h	GPT1 timer 4 register	0000h
T4CON	b	FF44h		A2h	GPT1 timer 4 control register	0000h
T4IC	b	FF64h		B2h	GPT1 timer 4 interrupt control register	- - 00h
T5		FE46h		23h	GPT2 timer 5 register	0000h
T5CON	b	FF46h		A3h	GPT2 timer 5 control register	0000h
T5IC	b	FF66h		B3h	GPT2 timer 5 interrupt control register	- - 00h
T6		FE48h		24h	GPT2 timer 6 register	0000h
T6CON	b	FF48h		A4h	GPT2 timer 6 control register	0000h
T6IC	b	FF68h		B4h	GPT2 timer 6 interrupt control register	- - 00h
T7		F050h	E	28h	CAPCOM timer 7 register	0000h
T78CON	b	FF20h		90h	CAPCOM timer 7 and 8 control register	0000h
T7IC	b	F17Ah	E	BDh	CAPCOM timer 7 interrupt control register	- - 00h
T7REL		F054h	E	2Ah	CAPCOM timer 7 reload register	0000h
T8		F052h	E	29h	CAPCOM timer 8 register	0000h
T8IC	b	F17Ch	E	BEh	CAPCOM timer 8 interrupt control register	- - 00h
T8REL		F056h	E	2Bh	CAPCOM timer 8 reload register	0000h
TFR	b	FFACh		D6h	Trap Flag register	0000h
WDT		FEAEh		57h	Watchdog timer register (read only)	0000h
WDTCON	b	FFAEh		D7h	Watchdog timer control register	00xxh(2)
XADRS3		F01Ch	E	0Eh	XPER address select register 3	800Bh
XP0IC	b	F186h	E	C3h	See *Section 9.1*	- - 00h(3)
XP1IC	b	F18Eh	E	C7h	See *Section 9.1*	- - 00h(3)
XP2IC	b	F196h	E	CBh	See *Section 9.1*	- - 00h(3)
XP3IC	b	F19Eh	E	CFh	See *Section 9.1*	- - 00h(3)

Table 47. List of XBus registers (continued)

Name	Physical address	Description	Reset value
RTCL	ED0Eh	RTC programmable counter low byte	XXXXh
RTCPH	ED08h	RTC prescaler register high byte	XXXXh
RTCPL	ED06h	RTC prescaler register low byte	XXXXh
XCLKOUTDIV	EB02h	CLKOUT divider control register	- - 00h
XEMU0	EB76h	XBUS emulation register 0 (write only)	XXXXh
XEMU1	EB78h	XBUS emulation register 1 (write only)	XXXXh
XEMU2	EB7Ah	XBUS emulation register 2 (write only)	XXXXh
XEMU3	EB7Ch	XBUS emulation register 3 (write only)	XXXXh
XIR0CLR	EB14h	X-Interrupt 0 clear register (write only)	0000h
XIR0SEL	EB10h	X-Interrupt 0 selection register	0000h
XIR0SET	EB12h	X-Interrupt 0 set register (write only)	0000h
XIR1CLR	EB24h	X-Interrupt 1 clear register (write only)	0000h
XIR1SEL	EB20h	X-Interrupt 1 selection register	0000h
XIR1SET	EB22h	X-Interrupt 1 set register (write only)	0000h
XIR2CLR	EB34h	X-Interrupt 2 clear register (write only)	0000h
XIR2SEL	EB30h	X-Interrupt 2 selection register	0000h
XIR2SET	EB32h	X-Interrupt 2 set register (write only)	0000h
XIR3CLR	EB44h	X-Interrupt 3 clear selection register (write only)	0000h
XIR3SEL	EB40h	X-Interrupt 3 selection register	0000h
XIR3SET	EB42h	X-Interrupt 3 set selection register (write only)	0000h
XMISC	EB46h	XBUS miscellaneous features register	0000h
XP1DIDIS	EB36h	Port 1 digital disable register	0000h
XPEREMU	EB7Eh	XPERCON copy for emulation (write only)	XXXXh
XPICON	EB26h	Extended port input threshold control register	- - 00h
XPOLAR	EC04h	XPWM module channel polarity register	0000h
XPP0	EC20h	XPWM module period register 0	0000h
XPP1	EC22h	XPWM module period register 1	0000h
XPP2	EC24h	XPWM module period register 2	0000h
XPP3	EC26h	XPWM module period register 3	0000h
XPT0	EC10h	XPWM module up/down counter 0	0000h
XPT1	EC12h	XPWM module up/down counter 1	0000h
XPT2	EC14h	XPWM module up/down counter 2	0000h
XPT3	EC16h	XPWM module up/down counter 3	0000h
XPW0	EC30h	XPWM module pulse width register 0	0000h

26 Ordering information

Table 79. Order codes

Order code	Package	Packing	Temperature range	CPU frequency range
ST10F273MR-4Q3	PQFP144	Tray	-40 to +125°C	1 to 40 MHz
ST10F273MR-4QR3		Tape and reel		
ST10F273MR-4T3	LQFP144	Tray		
ST10F273MR-4TX3		Tape and reel		