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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	68000
Number of Cores/Bus Width	1 Core, 16/32-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 85°C (TC)
Security Features	-
Package / Case	64-CDIP (0.900", 22.86mm)
Supplier Device Package	64-DIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts68c000vc10a

1. General Description

1.1 Introduction

This detail specification contains both a summary of the TS68C000 as well as detailed set of parametrics. The purpose is twofold to provide an instruction to the TS68C000 and support for the sophisticated user. For detail information on the TS68C000, refer to "68000 16-bit microprocessor user's manual".

1.2 Detailed Block Diagram

The functional block diagram is given in Figure 1-1 below.

Figure 1-1. Block Diagram

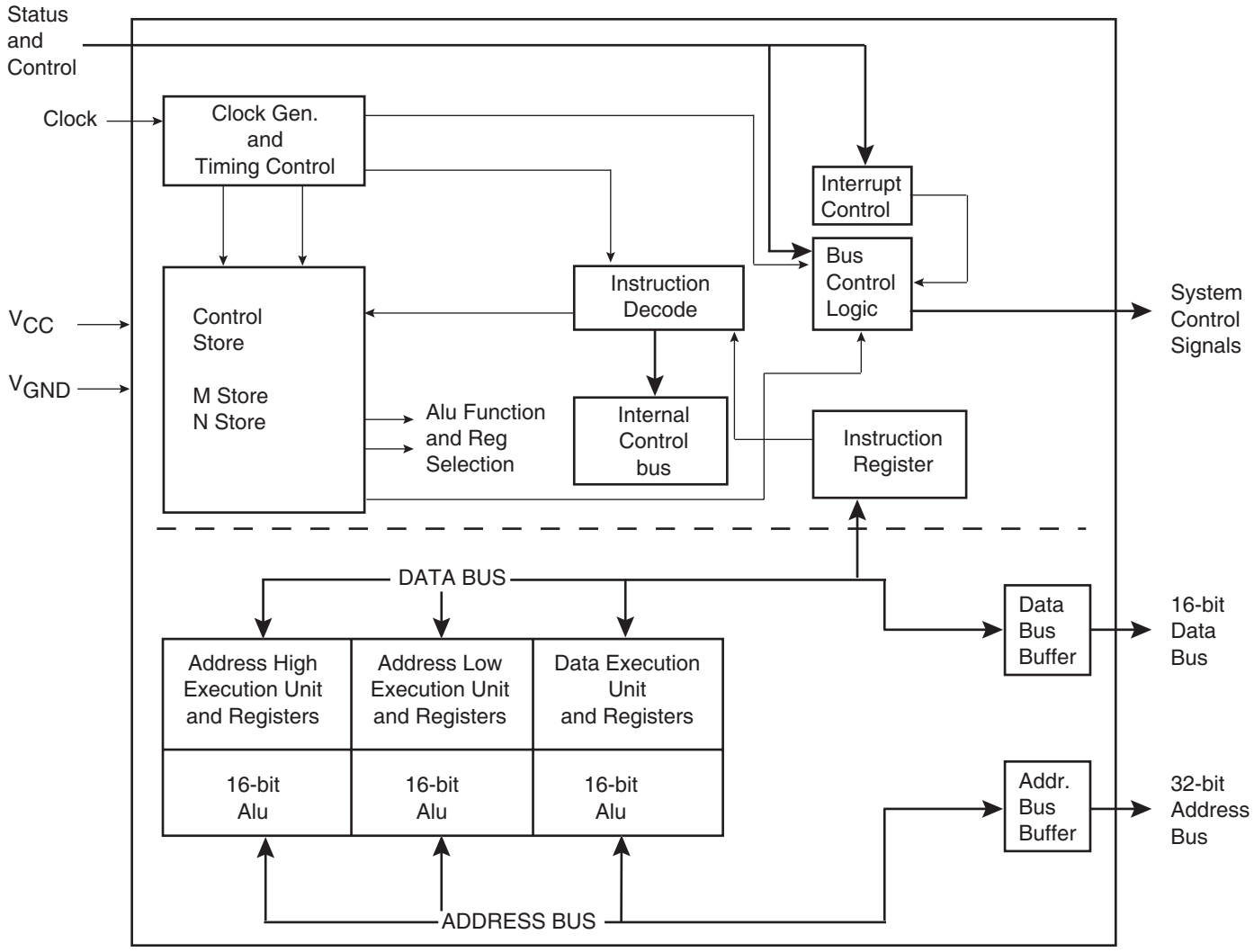


Figure 1-3. 68-terminal Pin Grid Array

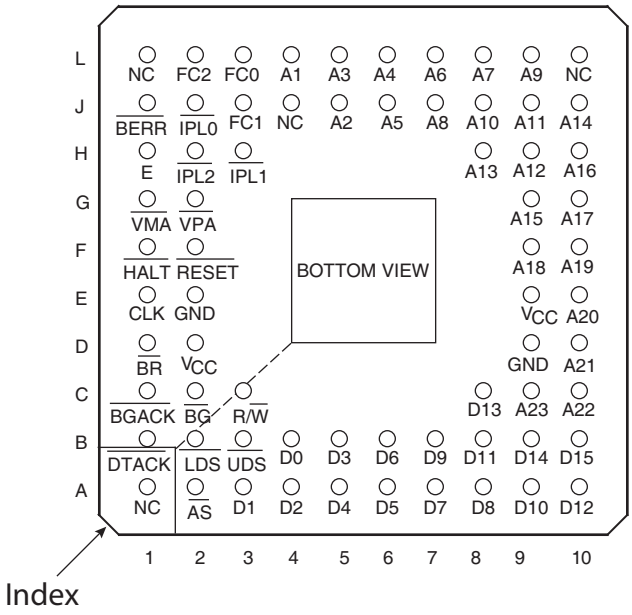


Figure 1-4. 68-lead Quad Pack

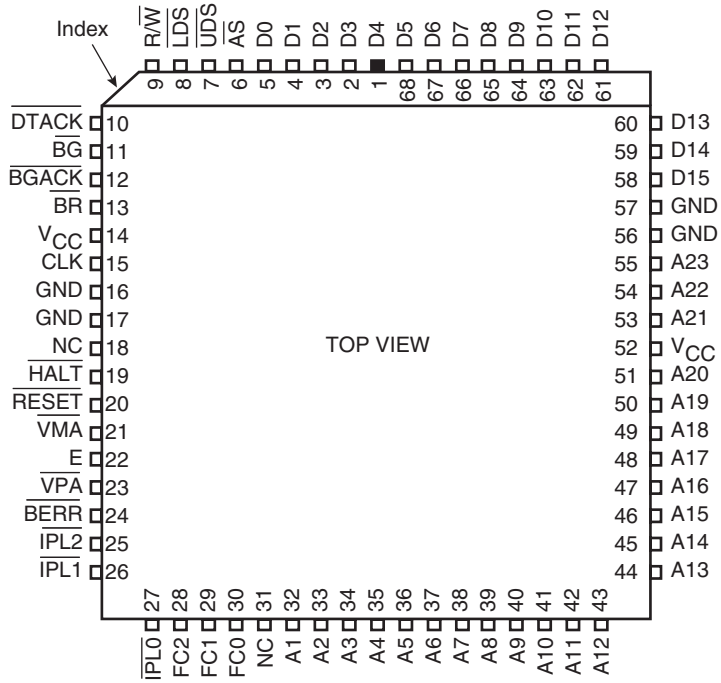
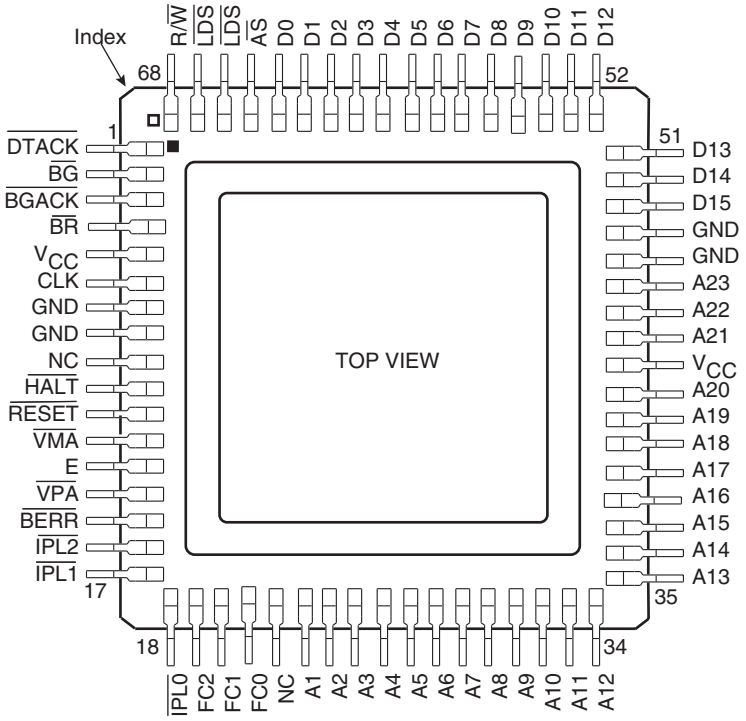


Figure 1-5. 68-ceramic Quad Flat Pack



1.4 Terminal Designations

The function, category and relevant symbol of each terminal of the device are given in the following table.

Table 1-1. Terminal Designations

Symbol	Function	Category
V_{CC}	Power supply (2 terminals)	Supply
V_{SS}[(1)]	Power supply (2 terminals)	Terminals
FC0 to FC2	Processor status	Outputs
$\overline{IPL0}$ to $\overline{IPL2}$	Interrupt control	Inputs
A1 to A23	Address bus	Outputs
AS	Asynchronous bus control	Outputs
R/$\overline{W}$		
$\overline{UDS}$		
$\overline{LDS}$		
$\overline{DTACK}$		Input
$\overline{BR}$	Bus arbitration control	Inputs
$\overline{BGACK}$		
$\overline{BG}$		Output

1.5.0.1 Address Bus (A1 through A23)

This 24-bit, unidirectional, three-state bus is capable of addressing 16 megabytes of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2 and A3 provide information about what level interrupt is being serviced while address lines A4 through A23 are set to a logic high.

1.5.0.2 Data Bus (D0 Through D15)

This 16-bit, bidirectional, three-state bus is the general-purpose data path. It can transfer and accept data in either word or byte length. During an interrupt acknowledge cycle, the external device supplies the vector number on data lines D0-07.

1.5.0.3 Asynchronous Bus Control

Asynchronous data transfers are handled using the following control signals: address strobe, read/write, upper and lower data strobes, and data transfer acknowledge. These signals are explained in the following paragraphs.

ADDRESS STROBE ($\overline{AS}$)

This signal indicates that there is a valid address on the address bus.

READ/WRITE (R/$\overline{W}$)

This signal defines the data bus transfer as a read or write cycle. The R/$\overline{W}$ signal also works in conjunction with the data strobes as explained in the following paragraph.

UPPER AND LOWER DATA STROBE ($\overline{UDS}$, $\overline{LDS}$)

These signals control the flow of data on the data bus, as shown in Table 1-2. When the R/$\overline{W}$ line is high, the processor will read from the data bus as indicated. When the R/W line is low, the processor will write to the data bus as shown.

DATA TRANSFER ACKNOWLEDGE ($\overline{DTACK}$)

This input indicates that the data transfer is completed. When the processor recognizes $\overline{DTACK}$ during a read cycle, data is latched and the bus cycle terminated. When $\overline{DTACK}$ is recognized during a write cycle, the bus cycle is terminated.

1.5.0.4 Bus Arbitration Control

The three signals, bus request, bus grant, and bus grant acknowledge, form a bus arbitration circuit to determine which device will be the bus master device.

BUS REQUEST ($\overline{BR}$)

This input is wire ORed with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master.

BUS GRANT ($\overline{BG}$)

This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

BUS GRANT ACKNOWLEDGE ($\overline{BGACK}$)

This input indicates that some other device has become the bus master.

Table 2-1. Absolute Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{CC}	Supply voltage		-0.3	+6.5	V
V_I	Input voltage		-0.3	+6.5	V
V_O	Output voltage		NA	NA	V
V_{OZ}	Off state voltage		-0.3	11.0	V
I_O	Output currents		NA	NA	mA
I_i	Input currents		NA	NA	mA
P_{DMAX}	Max power dissipation	T_{CASE} = -55°C		0.27	W
		T_{CASE} = +125°C		0.27	W
T_{STG}	Storage temperature		-55	+150	°C
T_J	Junction temperature			+150	°C
T_{LEADS}	Lead temperature	Max 5 sec. Soldering		+270	°C

2.4.4.2 Recommended Condition of Use and Guaranteed Characteristics

- Guaranteed Characteristics (Table 2-5 and Table 2-8)

  The characteristics associated to a specified measurement in the detail specification shall only be for inspection purposes.

  Such characteristic defined in this specification is guaranteed only under the conditions and within the limits which are specified for the relevant measurement. Unless otherwise specified, this guarantee applies within all the recommended operating ranges specified below.

- Recommended conditions of use (Table 2-2)

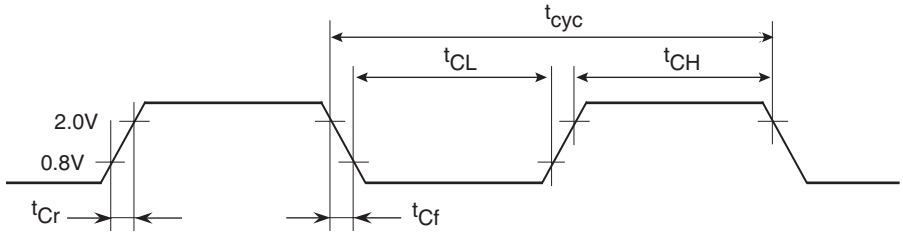
  To the correct operation of the device, the conditions of use shall be within the ranges specified below (see also above).

  These conditions shall not be for inspection purposes.

  Some recommended values may, however, be taken in other parts of this specification as detail conditions for an applicable test (Table 2-9).

- Additional Electrical Characteristics (Table 2-9), see "Additional Electrical Characteristics" on page 30.

Figure 2-1. Clock Input Timing Diagram



Note: Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside, and pass through, the range such that the rise of fall will be linear between 0.8V and 2.0V.

Unless otherwise stated, all voltages are referenced to the reference terminal (see Table 1-1).

2. CMOS Applications

- The TS68C000 completely satisfies the input/output drive requirements of CMOS logic devices.
- The HCMOS TS68C000 provides an order of magnitude power dissipation reduction when compared to the HMOS TS68000. However, the TS68C000 does not offer a "power down" or "halt" mode. The minimum operating frequency of the TS68C000 is 4 MHz.

2.4.5 Thermal Characteristics

Table 2-3. Thermal Characteristics

Package	Symbol	Parameter	Value	Unit
DIL 64	θ_{JA}	Thermal resistance junction to ambient	25	°C/W
	θ_{JC}	Thermal resistance junction to case	6	°C/W
PGA 68	θ_{JA}	Thermal resistance junction to ambient	30	°C/W
	θ_{JC}	Thermal resistance junction to case	6	°C/W
LCCC 68	θ_{JA}	Thermal resistance junction to ambient	40	°C/W
	θ_{JC}	Thermal resistance junction to case	8	°C/W
CQFP 68	θ_{JA}	Thermal resistance junction to ambient	40	°C/W
	θ_{JC}	Thermal resistance junction to case	10	°C/W

2.4.5.1 Power Considerations

The average chip-junction temperature, $T_{J,}$ in °C can be obtained from:

$T_J = T_A + (P_D \cdot \theta_{JA})$ (1)

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC,}$ Watts – Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins – User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An Approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$P_D = K: (T_J + 273)$ (2)

Solving equations (1) and (2) for K gives:

$K = P_D. (T_A + 273) + \theta_{JA} \cdot P_D^2$ (3)

where K is constant pertaining to the particular part K can be determined from the equation (3) by measuring PD (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}).

Table 2-4. Static Characteristics

V_{CC} = 5.0V V_{DC} ± 10%; GND = 0 V_{DC}; Tc = -55/+125°C and -40°C/+85°C

Test Number	Symbol	Parameter	Ref Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
1	I_{CC}	Supply current	41	V_{CC} = 5.5V F_C = 8 MHz F_C = 10 MHz F_C = 12 MHz	All		42 45 50	mA
2	V_{OL} (1)	Low level output voltage for: A1 to A23 FC0 to FC2; $\overline{BG}$	37	V_{CC} = 4.5V I_{OL} = 3.2 mA	25°C max min		0.5	V
3	V_{OL} (2)	Low level output voltage for: $\overline{HALT}$	37	V_{CC} = 4.5V I_{OL} = 1.6 mA	25°C max min		0.5	V
4	V_{OL} (3)	Low level output voltage for: $\overline{AS}$; R/$\overline{W}$: D0 to D15 UDS; $\overline{LDS}$; $\overline{VMA}$ and E	37	V_{CC} = 4.5V I_{OL} = 5.3 mA	25°C max min		0.5	V
5	V_{OL} (4)	Low level output voltage for: $\overline{RESET}$	37	V_{CC} = 4.5V I_{OL} = 5.0 mA	25°C max min		0.5	V
6	V_{OH}	High level output voltage for all outputs	37	V_{CC} = 4.5V I_{OH} = -400 µA	25°C max min	2.4	V_{CC} – 0.75	V
7	I_{IH} (1)	High level input current for all inputs excepted $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5V V_I = 5.5V	25°C max min		2.5	µA
8	I_{IL} (1)	Low level input current for all inputs excepted $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5V V_I = 0V	25°C max min	-2.5		µA
9	I_{IH} (2)	High level input current for: $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5V V_I = 5.5V	25°C max min		20	µA
10	I_{IL} (2)	Low level input current for: $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5V V_I = 0V	25°C max min	-20		µA

Table 2-5. Dynamic Characteristics – TS68C000-8 (Continued)
V_{CC} = 5.0 V_{DC} ± 10%; GND = 0 V_{DC}; Tc = -55/+125°C and Tc = -40°C/+85°C

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
11	t_{SU} (AVSL)	Set-up time Address valid to $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ low	10 – 11	Idem test 27 Load: 4	25°C max min	30(4)		ns
35	t_{PHL} (BRLGL)	Propagation time $\overline{BR}$ low to $\overline{BG}$ low	12	Idem test 27 Load: 3	25°C max min	1.5	3.5 +90	CLKS (2) ns
37	t_{PLH} (GALEH)	Propagation time $\overline{BGACK}$ low to $\overline{BG}$ high	12	Idem test 27 Load: 3	25°C max min	1.5	3.5 +90	CLKS (2) ns
48	t_{SU} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	11	Idem test 27	25°C max min	20(5)	–	ns
48	t_{SU} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	10 – 11	Idem test 27	25°C max min	20(5)	–	ns
26	t_h (DOSL)	Hold time Data-out valid to $\overline{LDS}$, $\overline{UDS}$ low	11	Idem test 27 Load: 4	25°C max min	30(4)	–	ns

Note: * Algebraic values
** Measurement method: see "General Requirements" on page 14 and "Test Conditions Specific to the Device" on page 26

Referred notes are given on page 25.

Table 2-6. Dynamic Characteristics – TS68C000-10

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
27	t_{SU} (DICL)	Set-up time Data-in to clock low(1)	10 – 11	See "Input and Output Signals for Dynamic Measurements" on page 29 (a) to (c) fc = 10 MHz	25°C max min	20(10)		ns
47	t_{SU} (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low(1)	10 – 11	Idem test 27	25°C max min	20(10)		ns

Table 2-6. Dynamic Characteristics – TS68C000-10 (Continued)

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits		Unit
						Min (*)	Max (*)	
18	t_{PLH} (CHRHX)	Propagation time CLK high to R/W high	10 – 11	Idem test 27 Load: 4	25°C		60[3]	ns
					max			
					min			
20	t_{PHL} (CHRL)	Propagation time CLK high to R/W low	10 – 11	Idem test 27 Load: 4	25°C		60[3]	ns
					max			
					min			
23	t_{PZL} t_{PZH} (CLDO)	Propagation time CLK low to Data-out valid	10 – 11	Idem test 27 Load: 4	25°C		55[3]	ns
					max			
					min			
6	t_{PZL} t_{PZH} (CLAV)	Propagation time CLK low to Address valid	10 – 11	Idem test 27 Load: 4	25°C		60	ns
					max			
					min			
32	t_{HRRF} (CHGL)	RESET/HALT input transition time	10 – 11	Idem test 27	25°C		200	ns
					max			
					min			
33	t_{PHL} (CHGL)	Propagation time CLK high to BG low	12	Idem test 27 Load: 3	25°C		60	ns
					max			
					min			
34	t_{PLH} (CHGH)	Propagation time CLK high to BG high	12	Idem test 27 Load: 3	25°C		60	ns
					max			
					min			
40	t_{PHL} (CLVM)	Propagation time CLK low to VMA low	13	Idem test 27 Load: 4	25°C		70	ns
					max			
					min			
41	t_{PHL} (CLE)	Propagation time CLK low to E low	13	Idem test 27 Load: 4	25°C		55	ns
					max			
					min			
8	t_{H} (SHAZ)	Hold time CLK high to Address	10 – 11	Idem test 27 Load: 3	25°C	0		ns
					max			
					min			
11	t_{SU} (AVSL)	Set-up time Address valid to AS, LDS, UDS low	10 – 11	Idem test 27 Load: 4	25°C	20[4]		ns
					max			
					min			

Table 2-7. Dynamic Characteristics – TS68C000-12 (Continued)

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits		Unit
						Min (*)	Max (*)	
37	t_{PLH} (GALGH)	Propagation time $\overline{BGACK}$ low to $\overline{BG}$ high	12	Idem test 27 Load: 3	25°C	1.5	3.5	CLKS (2)
					max			
					min		+70	ns
48	t_{SU} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	11	Idem test 27	25°C	20(5)		ns
					max			
					min			
48	t_{SU} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	10 – 11	Idem test 27	25°C	20(5)		ns
					max			
					min			
26	t_H (DOSL)	Hold time Data-out valid to $\overline{LDS}$, $\overline{UDS}$ low	11	Idem test 27 Load: 4	25°C	15(4)		ns
					max			
					min			

Note: * Algebraic values
** Measurement method: see "General Requirements" on page 14 and "Test Conditions Specific to the Device" on page 26

2.6.1.1 Referred notes to Table 2-4, Table 2-5, Table 2-6, Table 2-7

The following notes shall apply where referred into Table 2-4, Table 2-5, Table 2-6 and Table 2-7.

Notes:
1. If the asynchronous setup tlme (47) requirements are satisfied, the $\overline{DTACK}$ low-to-data setup time (31) requirement Gan be ignored. The data must only satisfy the data-in to clock-low setup time (27) for the following cycle.
2. Where "CLKS" is stated as unit time limit, the relevant time in nanoseconds shall be calculated as the actual cycle time of clock signal input multiply by the given number of CLKS limits.
3. For a loading capacitance of less than or equal to 50 picofarads, substrate 5 nanoseconds from the value given in the maximum columns.
4. Actual value depends on period.
5. If 47 is satisfied for bath $\overline{DTACK}$ and $\overline{BERR}$, 48 may be 0 nanoseconds.
6. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
7. The falling edge of 56 triggers bath the negation of the strobes ($\overline{AS}$, and X DS) and the falling edge of E. either of these events can occur first depending upon the loading on each signal. Specification 49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.
8. When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (±20%), substrate 10 nanoseconds from the values in these columns.
9. Each terminal of the device under test shall be tested separately against all existing VCC and VSS terminals of the device which shall be shorted together for the test. The other untested terminals shall be unconnected during the test. One cycle consists of the application of the bath limits as given in Table 2-5, Table 2-6 and Table 2-7.
10. This value should be treated as a min for design purpose. For the conformance testing the value shall be regarded as the maximum time.

Load NBR	Figure	R1	Rn	C_1 (1)	Output Application
1	5.1	–	910Ω	130 pF	$\overline{\text{RESET}}$
2	5.1	–	2.9 kΩ	70 pF	$\overline{\text{HALT}}$
3	5.2	6.0 k	1.22 kΩ	130 pF	A1 to A23, $\overline{\text{BG}}$ and FC0 to FC2
4	5.2	6.0 k	740Ω	130 pF	All other outputs

Note: 1. C_1 includes all parasitic capacitances of test machines

2.6.2.2 Time Definitions

The times specified in Table 2-5, Table 2-6 and Table 2-7 as dynamic characteristics are defined in Figure 2-4 to Figure 2-7 below by a reference number given in the column "Method" of the tables together with the relevant figure number.

Figure 2-4. Read Cycle Timing

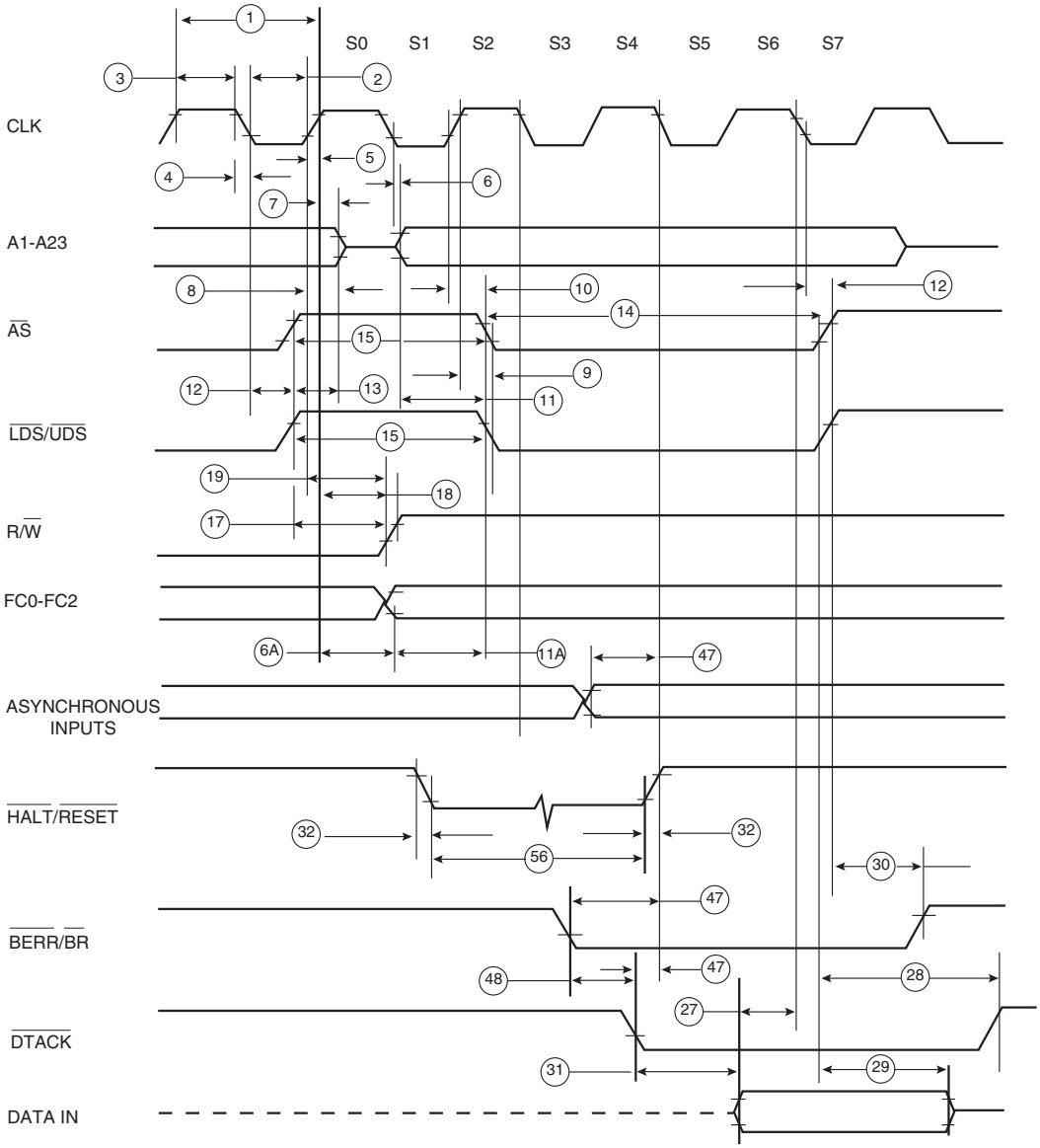


Figure 2-5. Write Cycle Timing

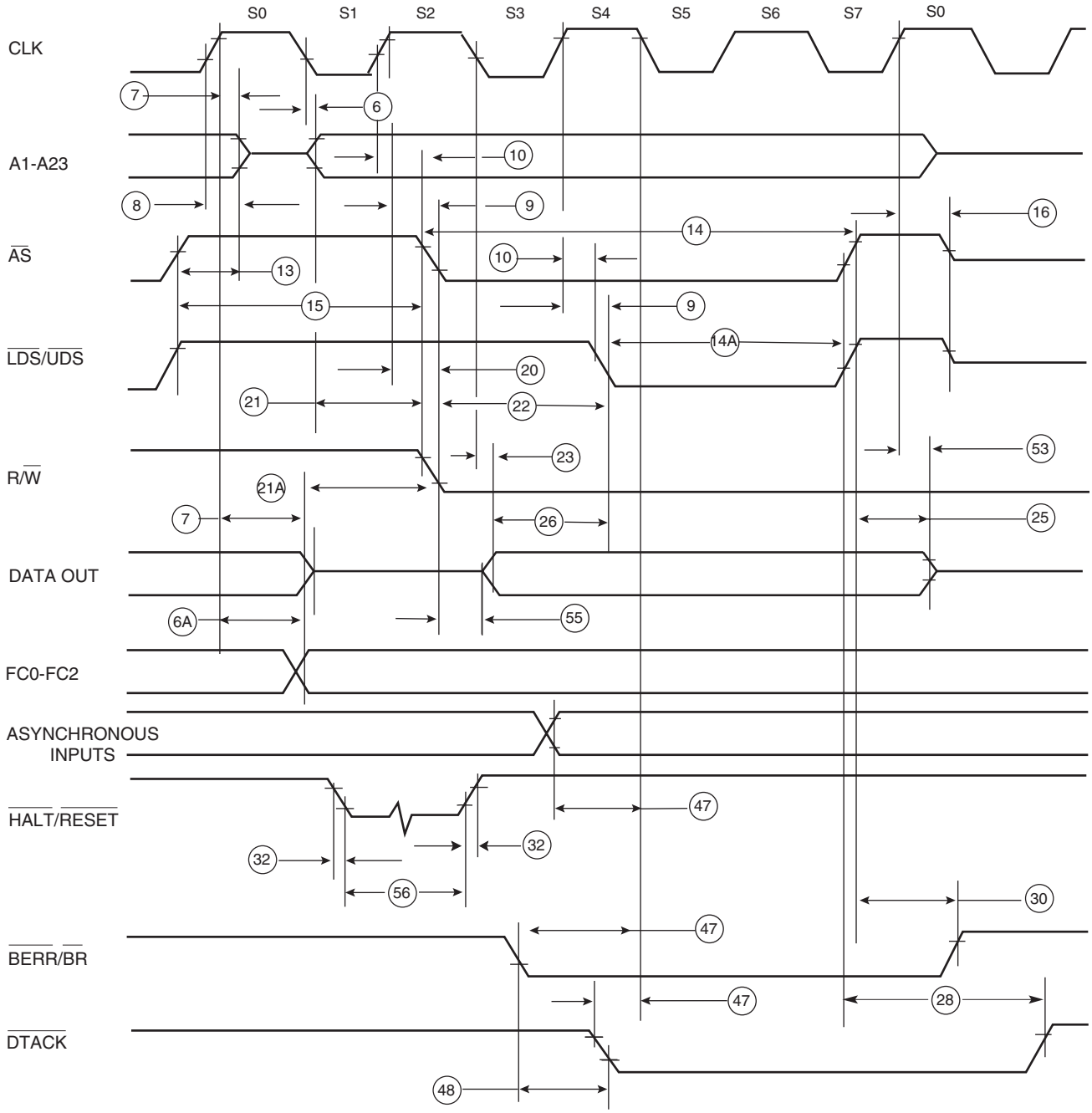


Figure 2-6. AC Electrical Waveforms – Bus Arbitration

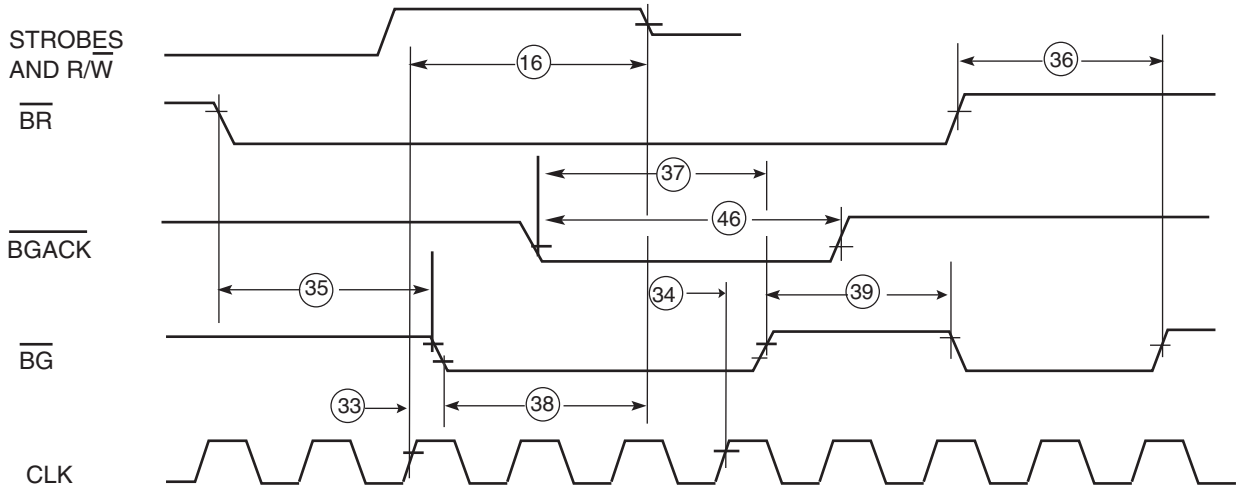
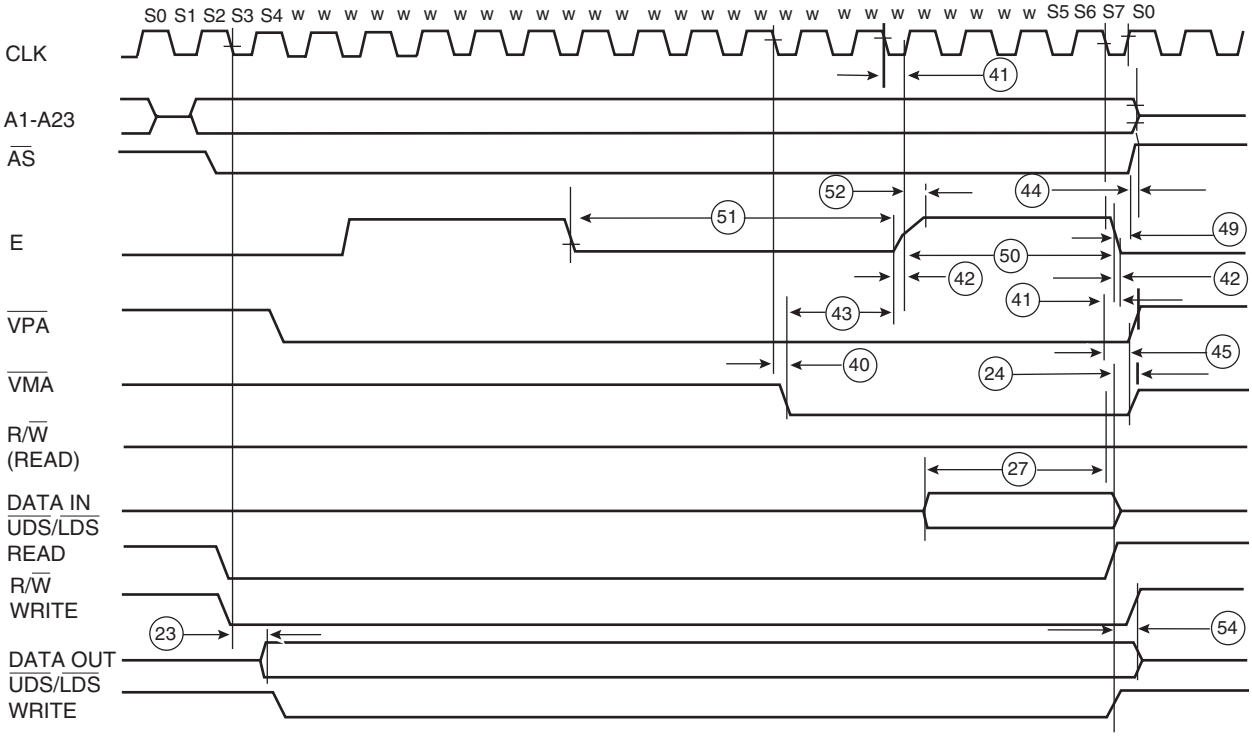


Figure 2-7. Enable/Interface Timing



2.6.2.3 Input and Output Signals for Dynamic Measurements

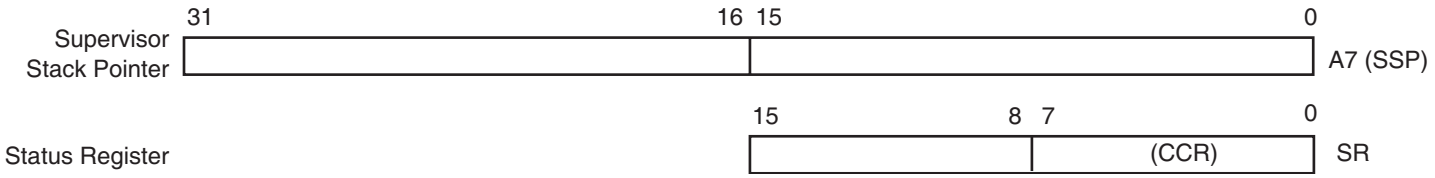
1. Input pulse characteristics

Where input pulse generator is loaded by only a 50Ω resistor, the input pulse characteristics shall be as shown in Figure 2-8.

Table 2-9. Additional Electrical Characteristics (Continued)

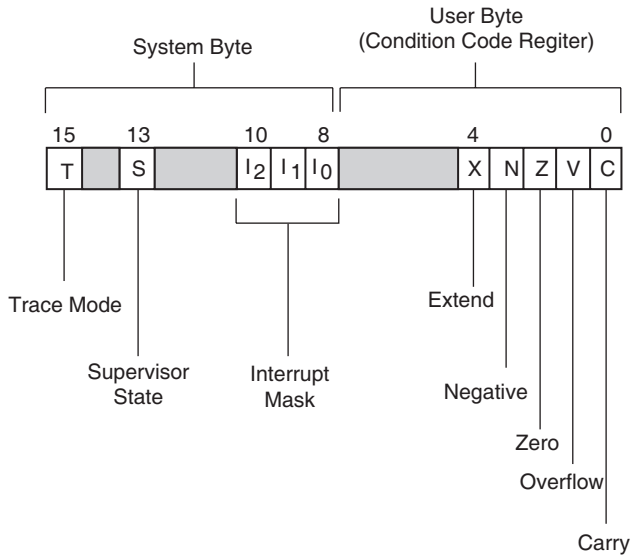
Item NO.	Symbol	Parameter	Ref Number	Load Number	TS68C000-8 Limits Min	TS68C000-8 Limits Max	TS68C000-10 Limits Min	TS68C000-10 Limits Max	TS68C000-12 Limits Min	TS68C000-12 Limits Max	Unit
54	t_{PHZ} t_{PLZ} (GLZ)	Propagation time $\overline{BG}$ low to Data and Address 3-state	Fig. 12 Ref. 36	BG, address 3 Data 4		80		70		60	ns
55	tw (GH)	$\overline{BG}$ width high	Fig. 12 Ref. 39		1.5		1.5		1.5		CLKS ns
56	t_{PLH} (VMLEH)	Propagation time $\overline{VMA}$ low to E high	Fig. 13 Ref. 43	4	200		150		90		ns
57	t_H (SHVPH)	Hold time $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ high to VPA high	Fig. 20 Ref. 44 (see "Although UDS and LDS are asserted, no data is read from the bus during the autovector cycle. The vector number is generated internally)." on page 45)	4	0	120	0	90	0	70	ns
58	t_H (ELAI)	Hold time E low to address	Fig. 13 Ref. 45	3	30		10		10		ns
59	t_w (BGL)	$\overline{BGACK}$ width low	Fig. 12 Ref. 46		1.5		1.5		1.5		CLKS (2)
61	t_w (EH)	E width high	Fig. 13 Ref. 50		450		350		280		ns
62	t_w (EL)	E width low	Fig. 13 Ref. 51		700		550		440		ns
63	t_{PHL} (FCVSL)	Propagation time FC valid to $\overline{AS}$, $\overline{DS}$ low	Fig. 10 Ref. 1A or 11A	4	60 (4)		50 (4)		40 (4)		ns
64	t_{PHL} (SHDAH)	Propagation time $\overline{AS}$, $\overline{DS}$ high to $\overline{DTACK}$ high	Fig. 10 Ref. 28	4	0	245(4)	0	190(4)	0	150(4)	ns
65	t_{PLH} (SHBEH)	Propagation time $\overline{AS}$, $\overline{DS}$ high to $\overline{BERR}$ high	Fig. 12 Ref. 30	4	0		0		0		ns
66	t_{SU} (DALDI)	Set-up time $\overline{DTACK}$ low to Data-in(1)	Fig. 10 Ref. 31			90(4)		65(4)		50(4)	ns

Figure 2-11. Supervisor Programming Model Supplement



The status register (Figure 2-12) contains the interrupt mask (eight levels available) as well as the conditions codes: extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and in a supervisor (S) or user state.

Figure 2-12. Status Register



2.7.2 Data Types and Addressing Modes

Five basic data types are supported. These data types are:

- Bits
- BCD Digits (4 bits)
- Bytes (8 bits)
- Words (16 bits)
- Long Words (32 bits)

In addition, operations on other data types such as memory addresses, status ward data, etc. are provided in the instruction set.

The 14 addressing modes, shown in Table 2-10, include six basic types:

- Register Direct
- Register Indirect
- Absolute
- program Counter Relative
- Immediate
- Implied

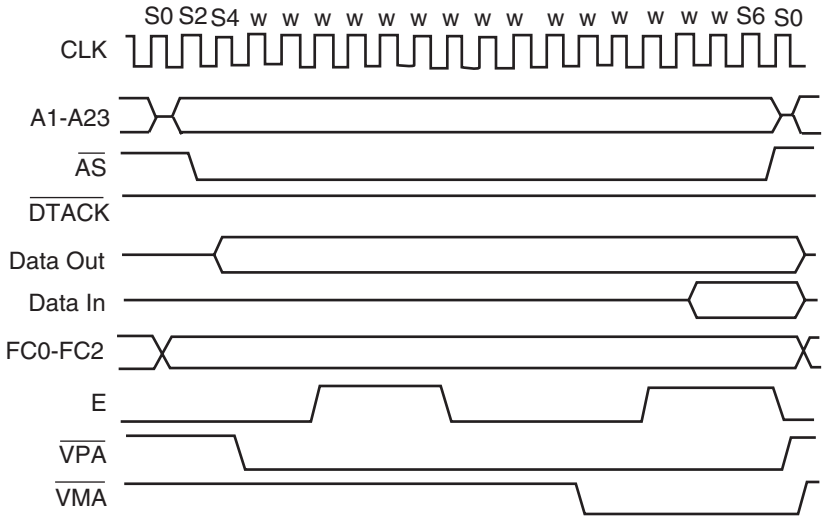
Table 2-11. Instruction Set Summary

Mnemonic	Description
ABCD	Add Decimal with Extend
ADD	Add
AND	Logical AND
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
Bcc	Branch Conditionally
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BRA	Branch Always
BSET	Bit Test and Set
BSR	Branch to Subroutine
BTST	Bit Test
CHK	Check Register Against Bounds
CLR	Clear Operand
CMP	Compare
DBcc	Test Condition, Decrement and Branch
DIVS	Signed Divide
DIVU	Unsigned Divide
EOR	Exclusive OR
EXG	Exchange Registers
EXT	Sign Extend
JMP	Jump
JSR	Jump to Subroutine
LEA	Lead Effective Address
LINK	Link Stack
LSL	Logical Shift Left
LSR	Logical Shift Right
MOVE	Move
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NOP	No Operation
NOT	One's Complement
OR	Logical OR
PEA	Push Effective Address

Table 2-12. Variations of Instruction Types

Instruction Type	Variation	Description
ADD	ADD	Add
	ADDA	Add Address
	ADDQ	Add Quick
	ADDI	Add Immediate
	ADDX	Add with Extend
AND	AND	Logical AND
	ANDI	And Immediate
	ANDI to CCR	And Immediate to Condition codes
	ANDI to SR	And Immediate to Status Register
CMP	CMP	Compare
	CMPA	Compare Address
	CMPM	Compare Memory
	CMPI	Compare Immediate
EOR	EOR	Exclusive OR
	EORI	Exclusive OR Immediate
	EORI to CCR	Exclusive OR Immediate to condition Codes
	EORI to SR	Exclusive OR Immediate to Status Register
MOVE	MOVE	Move
	MOVEA	Move Address
	MOVEM	Move Multiple Registers
	MOVEP	Move Peripheral Data
	MOVEQ	Move Quick
	MOVE from SR	Move from Status Register
	MOVE to SR	Move to Status Register
	MOVE to CCR	Move to Condition Codes
	MOVE USP	Move User Stack Pointer
NEG	NEG	Negate
	NEGX	Negate with Extend
OR	OR	Logical OR
	ORI	OR Immediate
	ORI to CCR	OR Immediate to Condition Codes
	ORI to SR	OR Immediate to Status Register
SUB	SUB	Subtract
	SUBA	Subtract Address
	SUBI	Subtract Immediate
	SUBQ	Subtract Quick
	SUBX	Subtract Extend

Figure 2-15. TS68C000 to EF6800 Peripheral Timing – Worst Case



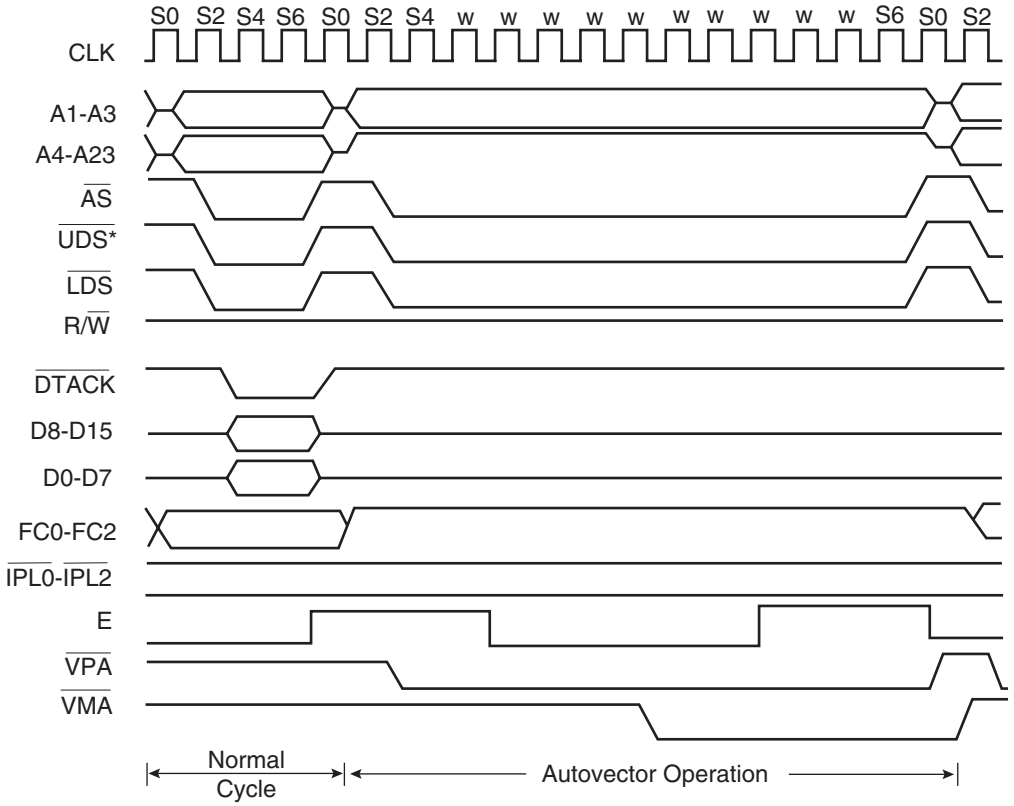
2.7.6.2 Interrupt Interface Operation

During an interrupt acknowledge cycle while the processor is fetching the vector, the $\overline{\text{VPA}}$ is asserted, the TS68C000 will assert $\overline{\text{VMA}}$ and complete a normal EF 6800 read cycle as shown in Figure 2-16. The processor will then use an internally generated vector that is a function of the interrupt being serviced. This process is know as autovectorlng. The seven autovectors are vector number 25 through 31 (decimal).

Autovectoring operates in the same fashion (but is not restricted to) the EF 6800 interrupt sequence. The basic difference is that there are six normal interrupt vectors and one NMI type vector. As with bath the EF 6800 and the TS68C(XX)'s normal vectored interrupt, the Interrupt service routine can be located any-where in the address space. This is due to the tact that while the vector numbers are fixed the contents of the vector table entries are assigned by the user.

Since $\overline{\text{VMA}}$ is asserted during autovectoring. The EF 6800 peripheral address decoding should prevent unintended accesses.

Figure 2-16. Autovector Operation Timing Diagram

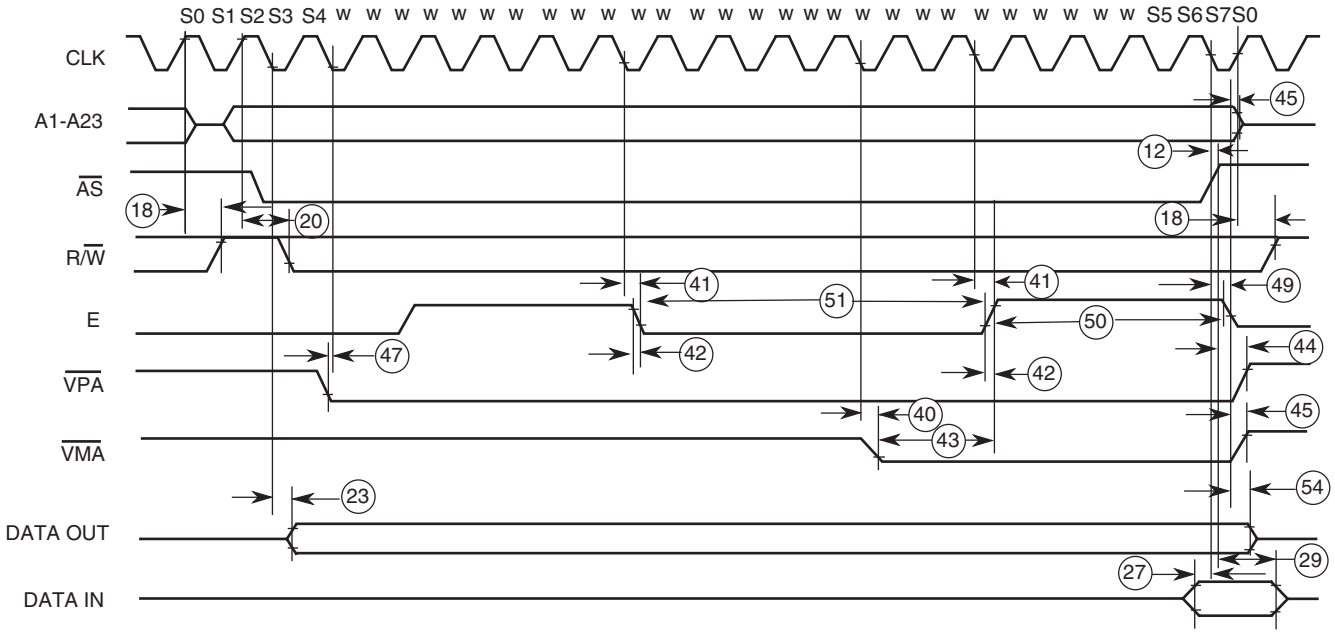


Although $\overline{UDS}$ and $\overline{LDS}$ are asserted, no data is read from the bus during the autovector cycle. The vector number is generated internally).

Table 2-13. Dynamic Electrical Characteristics TS68C000 to EF 6800 Peripheral

			8 MHz		10 MHz		12.5 MHz		
			Limits		Limits		Limits		
Number	Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit
12	CLSH	Clock low to $\overline{AS}$, $\overline{DS}$ high[1]		70		55		50	ns
18	CHRH	Clock high to R/$\overline{W}$ high[1]	0	70	0	60	0	60	ns
20	CHRL	Clock high to R/$\overline{W}$ low (write)[1]		70		60		60	ns
23	CLDO	Clock low to data out valid (write)		70		55		55	ns
27	CLDO	Data in to clock low (set up time on read)[2]	15		10		10		ns
29	SHDII	$\overline{AS}$, $\overline{DS}$ high to Data in invalid (hold time on read)	0		0		0		ns
40	CLVML	$\overline{AS}$, $\overline{DS}$ high to $\overline{VPA}$ high		70		70		70	ns
41	CLET	Clock low to E transition		70		55		45	ns
42	Erf	E output rise and fall time		25		25		25	ns
43	VMLEH	$\overline{VMA}$ low to E high	200		150		90		ns
44	SHVPH	$\overline{AS}$, $\overline{DS}$ high to $\overline{VPA}$ high	0	120	0	90	0	70	ns

Figure 2-18. TS68C000 to EF6800 Peripheral Timing Diagram – Worse Case



Note: This timing diagram is included for those who wish to design their own circuit to generate $\overline{VMA}$. It shows the worst case possibly attainable.

2.8 Preparation For Delivery

2.8.1 Packaging

Microcircuit are prepared for delivery in accordance with MIL-PRF-38535.

2.8.2 Certificate of Compliance

Atmel offers a certificate of compliance with each shipment of parts, affirming the products are in compliance with MIL-STD-883 and guarantying the parameters not tested at extreme temperatures for the entire temperature range.

2.9 Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

a) Device should be handled on benches with conductive and grounded surface.

b) Ground test equipment, tools and operator.

c) Do not handle devices by the leads.

d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

f) Maintain relative humidity above 50%, if practical.