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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	68000
Number of Cores/Bus Width	1 Core, 16/32-Bit
Speed	12MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 85°C (TC)
Security Features	-
Package / Case	64-CDIP (0.900", 22.86mm)
Supplier Device Package	64-DIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts68c000vc12a

Table 1-1. Terminal Designations (Continued)

Symbol	Function	Category
$\overline{BERR}$	System control	Input
$\overline{RESET}$		Input/Output
$\overline{HALT}$		
$\overline{VPA}$	6800 peripheral control	Input
$\overline{VMA}$		Output
E		Output
CLK	Clock	Input
D0 to D15	Data bus	Input/Output

Note: 1. V_{SS} is the reference terminal for the voltages

1.5 Signal Description

The input and output signals are illustrated functionally in Figure 1-6 and are described in the following paragraphs.

Figure 1-6. Input and Output Signals

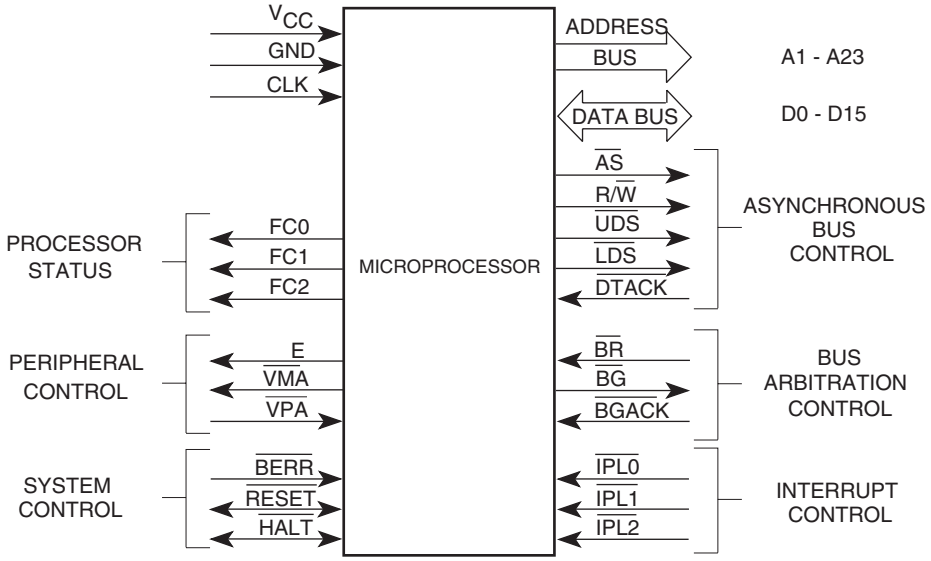


Table 1-2. Data Strobe Control of Data Bus

$\overline{UDS}$	$\overline{LDS}$	R/$\overline{W}$	D8-D15	D0-D7
High	High		No valid data	No valid data
Low	Low	High	Valid data bits 8-15	Valid data bits 0-7
High	Low	High	No valid data	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	No valid data
Low	Low	Low	Valid data bits 8-15	Valid data bits 0-7
High	Low	Low	Valid data bits 0-7	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	Valid data bits 8-15

1.5.0.1 Address Bus (A1 through A23)

This 24-bit, unidirectional, three-state bus is capable of addressing 16 megabytes of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2 and A3 provide information about what level interrupt is being serviced while address lines A4 through A23 are set to a logic high.

1.5.0.2 Data Bus (D0 Through D15)

This 16-bit, bidirectional, three-state bus is the general-purpose data path. It can transfer and accept data in either word or byte length. During an interrupt acknowledge cycle, the external device supplies the vector number on data lines D0-07.

1.5.0.3 Asynchronous Bus Control

Asynchronous data transfers are handled using the following control signals: address strobe, read/write, upper and lower data strobes, and data transfer acknowledge. These signals are explained in the following paragraphs.

ADDRESS STROBE ($\overline{AS}$)

This signal indicates that there is a valid address on the address bus.

READ/WRITE (R/$\overline{W}$)

This signal defines the data bus transfer as a read or write cycle. The R/$\overline{W}$ signal also works in conjunction with the data strobes as explained in the following paragraph.

UPPER AND LOWER DATA STROBE ($\overline{UDS}$, $\overline{LDS}$)

These signals control the flow of data on the data bus, as shown in Table 1-2. When the R/$\overline{W}$ line is high, the processor will read from the data bus as indicated. When the R/W line is low, the processor will write to the data bus as shown.

DATA TRANSFER ACKNOWLEDGE ($\overline{DTACK}$)

This input indicates that the data transfer is completed. When the processor recognizes $\overline{DTACK}$ during a read cycle, data is latched and the bus cycle terminated. When $\overline{DTACK}$ is recognized during a write cycle, the bus cycle is terminated.

1.5.0.4 Bus Arbitration Control

The three signals, bus request, bus grant, and bus grant acknowledge, form a bus arbitration circuit to determine which device will be the bus master device.

BUS REQUEST ($\overline{BR}$)

This input is wire ORed with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master.

BUS GRANT ($\overline{BG}$)

This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

BUS GRANT ACKNOWLEDGE ($\overline{BGACK}$)

This input indicates that some other device has become the bus master.

This signal should not be asserted until the following four conditions are met:

1. a bus grant has been received,
2. address strobe is inactive which indicates that the microprocessor is not using the bus,
3. data transfer acknowledge is Inactive which indicates that neither memory nor peripherals are using the bus, and
4. bus grant acknowledge is inactive which indicates that no other device is still claiming bus mastership.

1.5.0.5 Interrupt Control ($\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$)

These Input pins indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority white level zero indicates that no interrupts are requested. Level seven cannot be masked. The least significant bit is given in IPLO and the most significant bit is contained in $\overline{IPL2}$. These lines must remain stable until the processor signals interrupt acknowledge (FC0-FC2 are all high) to insure that the interrupt is recognized.

1.5.0.6 System Control

The system control inputs are used to either reset or halt the processor and to indicate to the processor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

BUS ERROR ($\overline{BERR}$)

This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of:

1. nonresponding devices,
2. interrupt vector number acquisition failure,
3. illegal access request as determined by a memory management unit, or
4. other application dependent errors.

The bus error signal interacts with the halt signal to determine if the current bus cycle should be re-executed or if exception processing should be performed.

RESET ($\overline{RESET}$)

This bidirectional signal line acts to reset (start a system initialization sequence) to processor in response to an external reset signal. An internally generated reset (result of a $\overline{RESET}$ instruction) causes all external devices to be reset and the internal of the processor is not affected. A total system reset (processor and external devices) is the result of external $\overline{HALT}$ and $\overline{RESET}$ signals applied at the same time.

HALT ($\overline{HALT}$)

When this bldirectional line is driven by an external device, it will cause the processor to stop at the completion of the current bus cycle. When the processor has been halted using this input, all control signals are inactive and all three-state lines are put in their high-impedance state.

When the processor has stopped executing Instructions, such as in a double bus fault condition, the $\overline{HALT}$ line is driven by the processor to indicate to external devices that the processor has stopped.

Table 2-2. Recommended Condition of Use

Symbol	Parameter	Operating Range			
		Model	Min	Max	Unit
V_{CC}	Supply voltage	All	4.5	5.5	V
V_{IL}	Low level input voltage	All	0	0.8	V
V_{IH}	High level input voltage (see also "Package" on page 10)	All	2.0	V_{CC}	V
T_{CASE}	Operating temperature	All	-55	+125	°C
R_L	Value of output load resistance	All	(1)		Ω
C_L	Output loading capacitance	All		(1)	pF
$t_{r(c)}$	Clock rise time (see Figure 2-1)	All		10	ns
$t_{f(c)}$	Clock fall time (see Figure 2-1)	All		10	ns
f_C	Clock frequency (see Figure 2-1)	TS68C000-8	4.0	8.0	MHz
		TS68C000-10	4.0	10.0	MHz
		TS68C000-12	4.0	12.5	MHz
t_{CYC}	Clock time (see Figure 2-1)	TS68C000-8	125	250	ns
		TS68C000-10	100	250	ns
		TS68C000-12	80	250	ns
$t_{W(CL)}$	Clock pulse width low (see Figure 2-1)	TS68C000-8	55	125	ns
		TS68C000-10	45	125	ns
		TS68C000-12	35	125	ns
$t_{W(CH)}$	Cycle pulse width high (see Figure 2-1)	TS68C000-8	55	125	ns
		TS68C000-10	45	125	ns
		TS68C000-12	35	125	ns

Note: 1. Load networks number 1 to 4 as specified in "Test Conditions Specific to the Device" on page 26 (Figure 2-2 and Figure 2-3) gives the maximum loading for the relevant output.

2.4.4.3 Special Recommended Conditions for CMOS Devices

1. CMOS Latch-up

The CMOS cell is basically composed of two complementary transistors (a P-channel and an N-channel), and, in the steady state, only one transistor is turned-on. The active P-channel transistor sources current when the output is a logic high and presents a high impedance when the output is a logic low. Thus the overall result is extremely low power consumption because there is no power loss through the active P.channel transistor. Also since only once transistor is determined by leakage currents.

Because the basic CMOS cell is composed of two complementary transistors, a virtual semiconductor controlled rectifier (SCR) may be formed when an input exceeds the supply voltage. The SCR that is formed by this high input causes the device to become "latched" in a mode that may result in excessive current drain and eventual destruction of the device. Although the device is Implemented with input protection diodes, care should be exercised to ensure that the maximum input voltages specification is not exceeded tram voltage transients; others may require no additional circuitry.

2. CMOS Applications

- The TS68C000 completely satisfies the input/output drive requirements of CMOS logic devices.
- The HCMOS TS68C000 provides an order of magnitude power dissipation reduction when compared to the HMOS TS68000. However, the TS68C000 does not offer a "power down" or "halt" mode. The minimum operating frequency of the TS68C000 is 4 MHz.

2.4.5 Thermal Characteristics

Table 2-3. Thermal Characteristics

Package	Symbol	Parameter	Value	Unit
DIL 64	θ_{JA}	Thermal resistance junction to ambient	25	°C/W
	θ_{JC}	Thermal resistance junction to case	6	°C/W
PGA 68	θ_{JA}	Thermal resistance junction to ambient	30	°C/W
	θ_{JC}	Thermal resistance junction to case	6	°C/W
LCCC 68	θ_{JA}	Thermal resistance junction to ambient	40	°C/W
	θ_{JC}	Thermal resistance junction to case	8	°C/W
CQFP 68	θ_{JA}	Thermal resistance junction to ambient	40	°C/W
	θ_{JC}	Thermal resistance junction to case	10	°C/W

2.4.5.1 Power Considerations

The average chip-junction temperature, $T_{J,}$ in °C can be obtained from:

$T_J = T_A + (P_D \cdot \theta_{JA})$ (1)

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC,}$ Watts – Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins – User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An Approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$P_D = K: (T_J + 273)$ (2)

Solving equations (1) and (2) for K gives:

$K = P_D. (T_A + 273) + \theta_{JA} \cdot P_D^2$ (3)

where K is constant pertaining to the particular part K can be determined from the equation (3) by measuring PD (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}).

These terms are related by the equation:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JA} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals $\theta_{JC.}$ Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

2.4.6 Mechanical and Environmental

The microcircuits shall meet all mechanical environmental requirements of MIL-STD-883 for class B devices.

2.4.7 Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit is legible and permanently marked with the following information as minimum:

- Atmel Logo
- Manufacturer's Part Number
- Class B Identification
- Date-code of inspection lot
- ESD Identifier if Available
- Country of Manufacturing

2.5 Quality Conformance Inspection

2.5.1 DESC/MIL-STD-883

Is in accordance with MIL-PRF-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

2.6 Electrical Characteristics

2.6.1 General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurements conditions are given below:

- Table 2-4: Static Electrical Characteristics for all electrical variants.
- Table 2-5, Table 2-6, Table 2-7 and Table 2-8: Dynamic electrical characteristics for 8 MHz, 10 MHz and 12.5 MHz.

For static characteristics (Table 2-4), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to clause "Test Conditions Specific to the Device" on page 26 of this specification (Table 2-5, Table 2-6, Table 2-7 and Table 2-8).

Indication of "min" or "max" in the column "test temperature" means minimum or maximum operating temperatures as defined in sub-clause "Recommended Condition of Use and Guaranteed Characteristics" on page 11 here above.

Table 2-5. Dynamic Characteristics – TS68C000-8 (Continued)
V_{CC} = 5.0 V_{DC} ± 10%; GND = 0 V_{DC}; Tc = -55/+125°C and Tc = -40°C/+85°C

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
47	t_{SU} (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low[1]	10 – 11	Idem test 27	25°C max min	20[10]		ns
47	t_{SU} (SBRCL)	Set-up time $\overline{BR}$ low to clock low [1]	10 – 11	Idem test 27	25°C max min	20[10]		ns
47	t_{SU} (SBGCL)	Set-up time $\overline{BGACK}$ low to clock low[1]	10 – 11	Idem test 27	25°C max min	20[10]		ns
47	t_{SU} (SVPACL)	Set-up time $\overline{VPA}$ low to clock low [1]	10 – 11	Idem test 27	25°C max min	20[10]		ns
47	t_{SU} (SBERCL)	Set-up time $\overline{BERR}$ low to clock low[1]	10 – 11	Idem test 27	25°C max min	20[10]		ns
2	t_w (CL)	Clock width low	10 – 11	Idem test 27	25°C max min	55[10]	125	ns
3	t_w (CH)	Clock width high	10 – 11	Idem test 27	25°C max min	55	125	ns
6A	t_{PLH} t_{PHL} (CHFCV)	Propagation time clock high to FC valid	10 – 11	Idem test 27 Load: 3	25°C max min		70	ns
9	t_{PHL} (CHSLX)	Propagation time clock high to $\overline{AS}$ low	10 – 11	Idem test 27 Load: 4	25°C max min		60[3]	
9	t_{PHL} (CHSL)	Propagation time CLK high to $\overline{LDS}$, $\overline{UDS}$ low	10 – 11	Idem test 27 Load: 4	25°C max min		60[3]	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to $\overline{AS}$ high	10 – 11	Idem test 27 Load: 4	25°C max min		70[3]	ns

Table 2-7. Dynamic Characteristics – TS68C000-12 (Continued)

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits		Unit
						Min (*)	Max (*)	
37	t_{PLH} (GALGH)	Propagation time $\overline{BGACK}$ low to $\overline{BG}$ high	12	Idem test 27 Load: 3	25°C	1.5	3.5	CLKS (2)
					max			
					min		+70	ns
48	t_{SU} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	11	Idem test 27	25°C	20(5)		ns
					max			
					min			
48	t_{SU} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	10 – 11	Idem test 27	25°C	20(5)		ns
					max			
					min			
26	t_H (DOSL)	Hold time Data-out valid to $\overline{LDS}$, $\overline{UDS}$ low	11	Idem test 27 Load: 4	25°C	15(4)		ns
					max			
					min			

Note: * Algebraic values
** Measurement method: see "General Requirements" on page 14 and "Test Conditions Specific to the Device" on page 26

2.6.1.1 Referred notes to Table 2-4, Table 2-5, Table 2-6, Table 2-7

The following notes shall apply where referred into Table 2-4, Table 2-5, Table 2-6 and Table 2-7.

Notes:
1. If the asynchronous setup tlme (47) requirements are satisfied, the $\overline{DTACK}$ low-to-data setup time (31) requirement Gan be ignored. The data must only satisfy the data-in to clock-low setup time (27) for the following cycle.
2. Where "CLKS" is stated as unit time limit, the relevant time in nanoseconds shall be calculated as the actual cycle time of clock signal input multiply by the given number of CLKS limits.
3. For a loading capacitance of less than or equal to 50 picofarads, substrate 5 nanoseconds from the value given in the maximum columns.
4. Actual value depends on period.
5. If 47 is satisfied for bath $\overline{DTACK}$ and $\overline{BERR}$, 48 may be 0 nanoseconds.
6. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
7. The falling edge of 56 triggers bath the negation of the strobes ($\overline{AS}$, and X DS) and the falling edge of E. either of these events can occur first depending upon the loading on each signal. Specification 49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.
8. When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (±20%), substrate 10 nanoseconds from the values in these columns.
9. Each terminal of the device under test shall be tested separately against all existing VCC and VSS terminals of the device which shall be shorted together for the test. The other untested terminals shall be unconnected during the test. One cycle consists of the application of the bath limits as given in Table 2-5, Table 2-6 and Table 2-7.
10. This value should be treated as a min for design purpose. For the conformance testing the value shall be regarded as the maximum time.

Figure 2-5. Write Cycle Timing

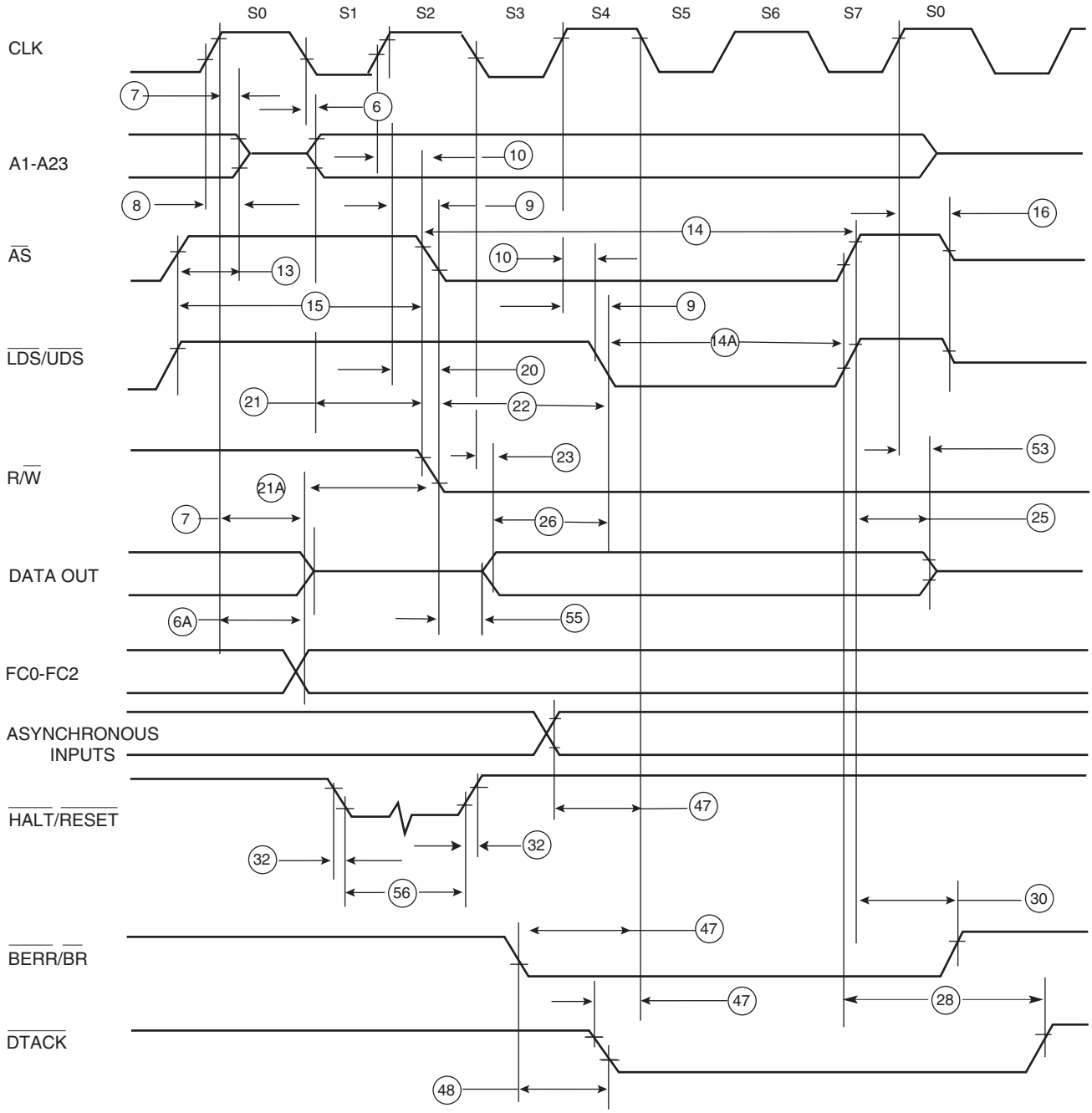


Figure 2-6. AC Electrical Waveforms – Bus Arbitration

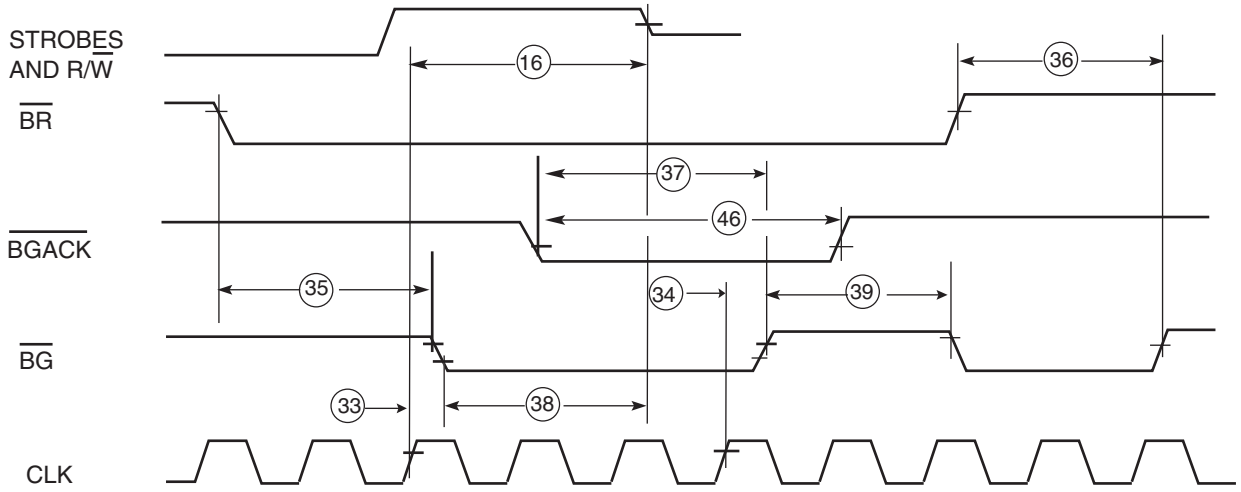
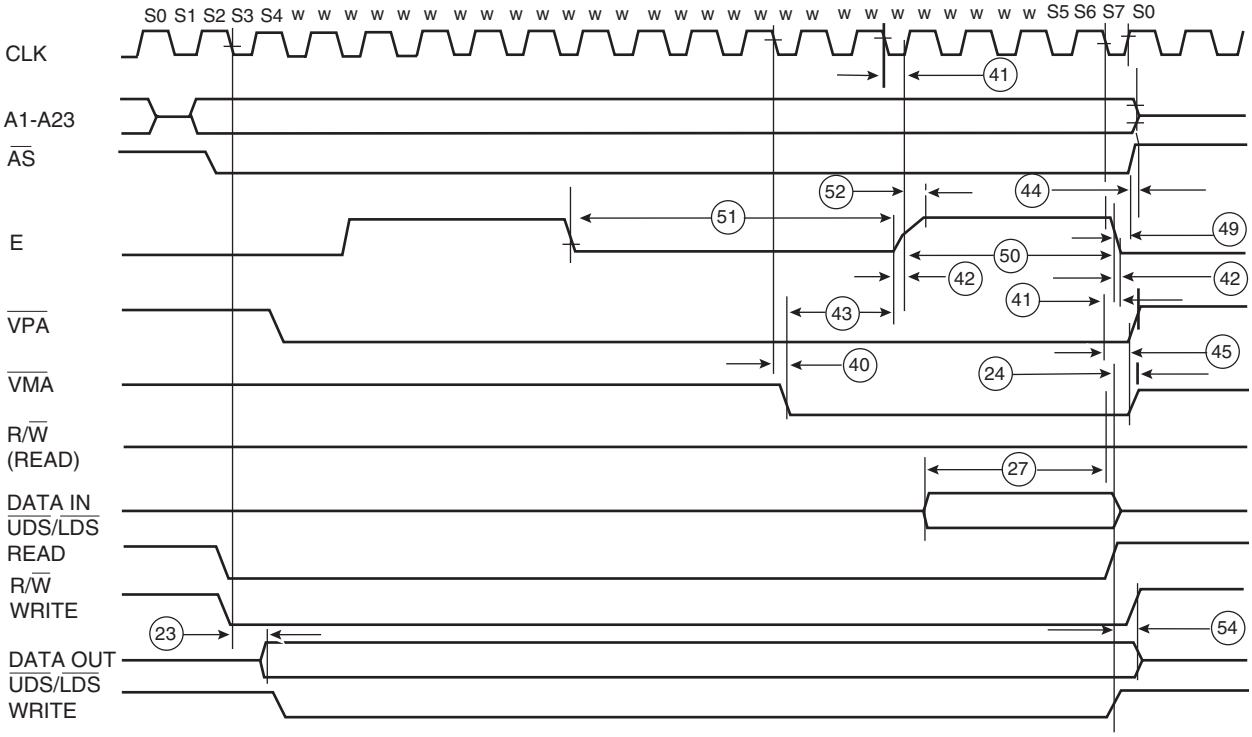


Figure 2-7. Enable/Interface Timing



2.6.2.3 Input and Output Signals for Dynamic Measurements

1. Input pulse characteristics

Where input pulse generator is loaded by only a 50Ω resistor, the input pulse characteristics shall be as shown in Figure 2-8.

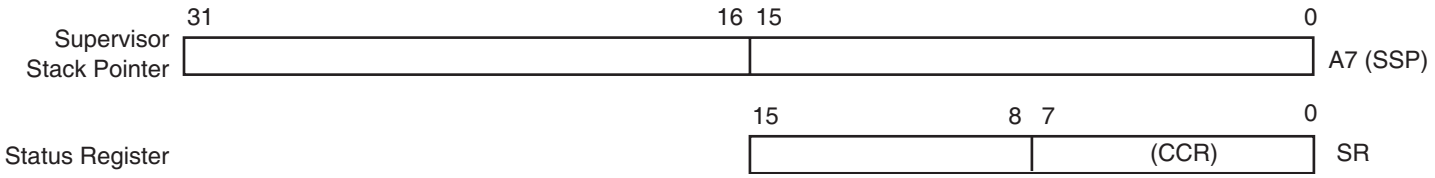
Table 2-9. Additional Electrical Characteristics

Item NO.	Symbol	Parameter	Ref Number	Load Number	TS68C000-8		TS68C000-10		TS68C000-12		Unit
					Limits		Limits		Limits		
					Min	Max	Min	Max	Min	Max	
6A	V_{OH}	High level output voltage for E with pull up R = 1.1K to V_{CC}			Min	V_{CC}-0.75	Min	V_{CC}-0.75	Min	V_{CC}-0.75	V
37	t_{PLZ} t_{PHZ} (CLAZX)	Propagation time CLK low to Address 3-state	Fig. 10 Ref. 7	3		80		70		60	ns
39	t_{PHZ} (CHSZX)	Propagation time CLK high to $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ 3-state	Fig. 11 Ref. 16	4		80		70		60	ns
40	t_{PLZ} t_{PHZ} (CHRZ)	Propagation time CLK high to R/$\overline{W}$ 3-state	Fig. 12 Ref. 16	4		80		70		60	ns
41	t_{PHZ} t_{PLZ} (CHAZX)	Propagation time CLK high to Data 3-state	Fig. 11 Ref. 7	4		80		70		60	ns
43	t_H (SHAZ)	Hold time $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ high to Address	Fig. 10 Ref. 13	3	30		20		10		ns
44	t_w (SL)	$\overline{AS}$/DS width low	Fig. 10 Ref. 14		240 (4)		195 (4)		160 (4)		ns
45	t_w (SL)	$\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ width high	Fig. 10 Ref. 15		150 (4)		105 (4)		65 (4)		ns
46	t_{SU} (SHRH)	Set-up time $\overline{LDS}$, $\overline{UDS}$ high to R/$\overline{W}$ high	Fig. 10 Ref. 17	4	40 (4)		20 (4)		10 (4)		ns
47	t_{SU} (AVRL)	Set-up time Address valid to R/$\overline{W}$ low	Fig. 10 Ref. 21	4	20 (4)		0 (4)		0 (4)		ns
48	t_{PHL} (RLSL)	Propagation time R/$\overline{W}$ low to lds, uds low	Fig. 11 Ref. 22	4	80 (4)		50 (4)		30 (4)		ns
49	t_H (SHDO)	Hold time $\overline{LDS}$, $\overline{UDS}$ high to Data-out	Fig. 11 Ref. 25	4	30 (4)		20 (4)		15 (4)		ns
50	t_H (SHDI)	Hold time $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ high to Data-in	Fig. 10 Ref. 29		0		0		0		ns
52	t_H (BRHGH)	Propagation time $\overline{BR}$ high to $\overline{BG}$ high(6)	Fig. 12 Ref. 36	3	1.5	3.5 + 90	1.5	3.5 + 80	1.5	3.5 + 70	CLKS (2) ns

Table 2-9. Additional Electrical Characteristics (Continued)

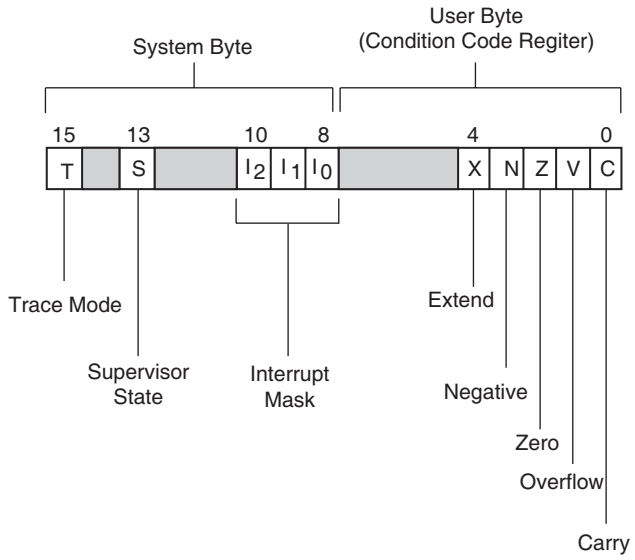
Item NO.	Symbol	Parameter	Ref Number	Load Number	TS68C000-8 Limits Min	TS68C000-8 Limits Max	TS68C000-10 Limits Min	TS68C000-10 Limits Max	TS68C000-12 Limits Min	TS68C000-12 Limits Max	Unit
54	t_{PHZ} t_{PLZ} (GLZ)	Propagation time $\overline{BG}$ low to Data and Address 3-state	Fig. 12 Ref. 36	BG, address 3 Data 4		80		70		60	ns
55	tw (GH)	$\overline{BG}$ width high	Fig. 12 Ref. 39		1.5		1.5		1.5		CLKS ns
56	t_{PLH} (VMLEH)	Propagation time $\overline{VMA}$ low to E high	Fig. 13 Ref. 43	4	200		150		90		ns
57	t_H (SHVPH)	Hold time $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ high to VPA high	Fig. 20 Ref. 44 (see "Although UDS and LDS are asserted, no data is read from the bus during the autovector cycle. The vector number is generated internally)." on page 45)	4	0	120	0	90	0	70	ns
58	t_H (ELAI)	Hold time E low to address	Fig. 13 Ref. 45	3	30		10		10		ns
59	t_w (BGL)	$\overline{BGACK}$ width low	Fig. 12 Ref. 46		1.5		1.5		1.5		CLKS (2)
61	t_w (EH)	E width high	Fig. 13 Ref. 50		450		350		280		ns
62	t_w (EL)	E width low	Fig. 13 Ref. 51		700		550		440		ns
63	t_{PHL} (FCVSL)	Propagation time FC valid to $\overline{AS}$, $\overline{DS}$ low	Fig. 10 Ref. 1A or 11A	4	60 (4)		50 (4)		40 (4)		ns
64	t_{PHL} (SHDAH)	Propagation time $\overline{AS}$, $\overline{DS}$ high to $\overline{DTACK}$ high	Fig. 10 Ref. 28	4	0	245(4)	0	190(4)	0	150(4)	ns
65	t_{PLH} (SHBEH)	Propagation time $\overline{AS}$, $\overline{DS}$ high to $\overline{BERR}$ high	Fig. 12 Ref. 30	4	0		0		0		ns
66	t_{SU} (DALDI)	Set-up time $\overline{DTACK}$ low to Data-in(1)	Fig. 10 Ref. 31			90(4)		65(4)		50(4)	ns

Figure 2-11. Supervisor Programming Model Supplement



The status register (Figure 2-12) contains the interrupt mask (eight levels available) as well as the conditions codes: extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and in a supervisor (S) or user state.

Figure 2-12. Status Register



2.7.2 Data Types and Addressing Modes

Five basic data types are supported. These data types are:

- Bits
- BCD Digits (4 bits)
- Bytes (8 bits)
- Words (16 bits)
- Long Words (32 bits)

In addition, operations on other data types such as memory addresses, status ward data, etc. are provided in the instruction set.

The 14 addressing modes, shown in Table 2-10, include six basic types:

- Register Direct
- Register Indirect
- Absolute
- program Counter Relative
- Immediate
- Implied

Table 2-10. Addressing Modes (Continued)

Addressing Modes	Syntax
Register Indirect Addressing	
Register Indirect	(An)
Postincrement Register Indirect	(An) +
Predecrement Register Indirect	- (An)
Register Indirect with Offset	d_{16} (An)
Indexed Register Indirect with Offset	d_8 (An, Xn)
Immediate Data Addressing	
Immediate	= XXX
Quick Immediate	= 1- = 8
Implied Addressing	
Implied Register	SR/USP/SP/PC

Notes:

Dn = Data Register

An = Address Register

Xn = Address of Data Register used as Index Register

SR = Status Register

PC = Program Counter

SP = Stack Pointer

USP = User Stack Pointer

( ) = Effective Address

d_8 = 8-bit Offset (Displacement)

d_{16} = 16-bit Offset (Displacement)

= xxx = Immediate Data

Table 2-12. Variations of Instruction Types

Instruction Type	Variation	Description
ADD	ADD	Add
	ADDA	Add Address
	ADDQ	Add Quick
	ADDI	Add Immediate
	ADDX	Add with Extend
AND	AND	Logical AND
	ANDI	And Immediate
	ANDI to CCR	And Immediate to Condition codes
	ANDI to SR	And Immediate to Status Register
CMP	CMP	Compare
	CMPA	Compare Address
	CMPM	Compare Memory
	CMPI	Compare Immediate
EOR	EOR	Exclusive OR
	EORI	Exclusive OR Immediate
	EORI to CCR	Exclusive OR Immediate to condition Codes
	EORI to SR	Exclusive OR Immediate to Status Register
MOVE	MOVE	Move
	MOVEA	Move Address
	MOVEM	Move Multiple Registers
	MOVEP	Move Peripheral Data
	MOVEQ	Move Quick
	MOVE from SR	Move from Status Register
	MOVE to SR	Move to Status Register
	MOVE to CCR	Move to Condition Codes
	MOVE USP	Move User Stack Pointer
NEG	NEG	Negate
	NEGX	Negate with Extend
OR	OR	Logical OR
	ORI	OR Immediate
	ORI to CCR	OR Immediate to Condition Codes
	ORI to SR	OR Immediate to Status Register
SUB	SUB	Subtract
	SUBA	Subtract Address
	SUBI	Subtract Immediate
	SUBQ	Subtract Quick
	SUBX	Subtract Extend

After recognition of $\overline{VPA}$, the processor assures that the enable (E) is low, by waiting if necessary, and subsequently asserts $\overline{VMA}$. Valid memory address is then used as part of the chip select equation of the peripheral. This ensures that the EF6800 peripherals are selected and deselected at the correct time. The peripheral now runs its cycle during the high portion of the signal. Figure 2-17 and Figure 2-18 depict the best and worst case EF6800 cycle timing. This cycle length is dependent strictly upon when $\overline{VPA}$ Is asserted in relationship to the E clock.

If it is assumed that external circuitry asserts $\overline{VPA}$ as soon as possible after the assertion of $\overline{AS}$, then $\overline{VPA}$ will be recognized as being asserted on the falling edge of 54. In this case, no "extra" wait cycles will be inserted prior to the recognition of $\overline{VPA}$ asserted and only the wait cycles inserted to synchronize with the E clock will determine the total length of the cycle. In any case, the synchronization delay will be some integral number of clock cycles within the following two extremes:

1. Best Case – $\overline{VPA}$ is recognized as being asserted on the falling edge three crack cycles before E rizes (or three clock cycles after E falls).
2. Worst Case – $\overline{VPA}$ is recognized as being asserted on the falling edge two clock cycles before E rises (or four clock cycles after E falls).

During a read cycle, the processor latches the peripheral data in state 6. For all cycles, the processor negates the address and data strobes one-half clack cycle rater in state 7 and the enable signal goes low at this time. Another half clock later, the address bus is put in the high-impedance state. During a write cycle the data bus is put in the high-impedance state and the read/write signal is switched high. The peripheral logic must remove $\overline{VPA}$ within one clock after the address strobe is negated.

$\overline{DTACK}$ should not be asserted while $\overline{VPA}$ Is asserted. Notice that the TS68C000 $\overline{VMA}$ is active low, constrasted with the active high EF 6800 $\overline{VMA}$. This allows the processor to put its buses in the high-impedance state on DMA requests without inadvertently selecting the peripherals.

Figure 2-14. TS68C000 to EF6800 Peripheral Timing – Best Case

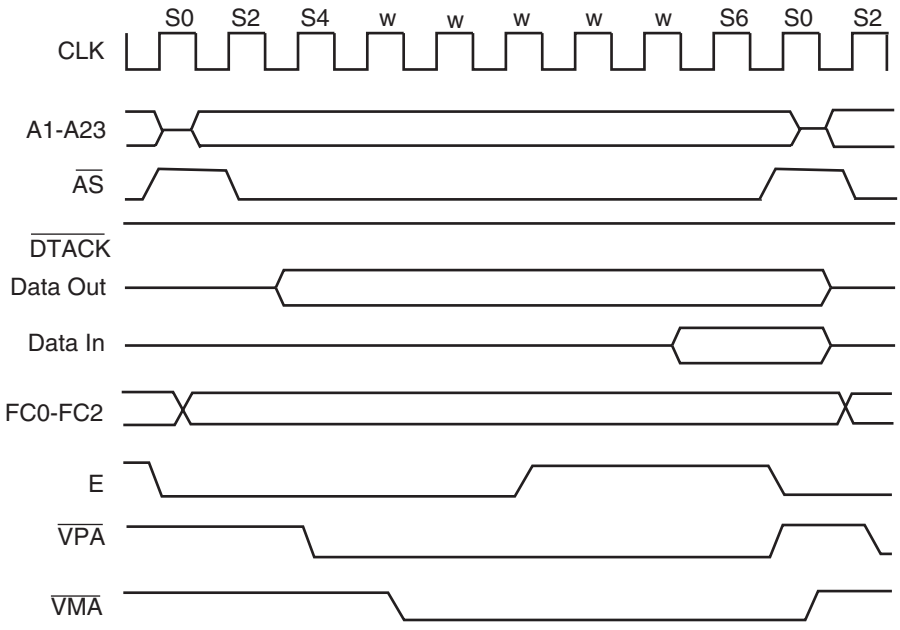
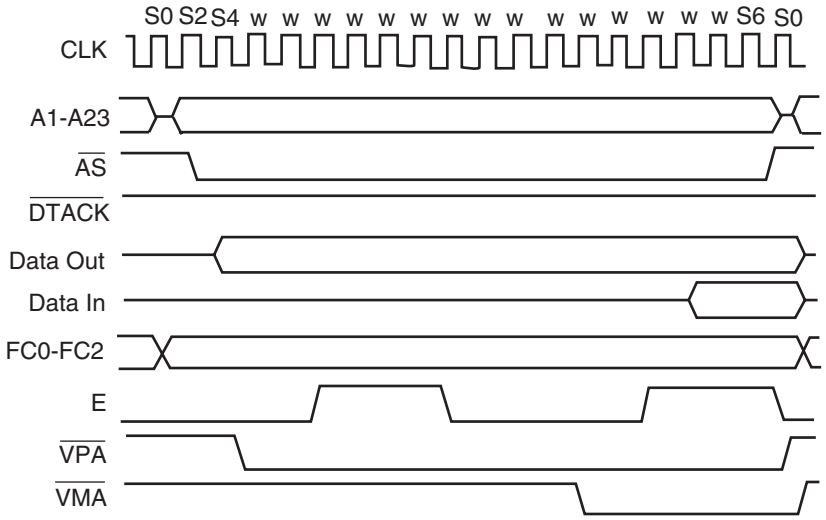


Figure 2-15. TS68C000 to EF6800 Peripheral Timing – Worst Case



2.7.6.2 Interrupt Interface Operation

During an interrupt acknowledge cycle while the processor is fetching the vector, the $\overline{\text{VPA}}$ is asserted, the TS68C000 will assert $\overline{\text{VMA}}$ and complete a normal EF 6800 read cycle as shown in Figure 2-16. The processor will then use an internally generated vector that is a function of the interrupt being serviced. This process is know as autovectorlng. The seven autovectors are vector number 25 through 31 (decimal).

Autovectoring operates in the same fashion (but is not restricted to) the EF 6800 interrupt sequence. The basic difference is that there are six normal interrupt vectors and one NMI type vector. As with bath the EF 6800 and the TS68C(XX)'s normal vectored interrupt, the Interrupt service routine can be located any-where in the address space. This is due to the tact that while the vector numbers are fixed the contents of the vector table entries are assigned by the user.

Since $\overline{\text{VMA}}$ is asserted during autovectoring. The EF 6800 peripheral address decoding should prevent unintended accesses.

2.10 Package Mechanical Data

Figure 2-19. 68-lead – Pin Grid Array

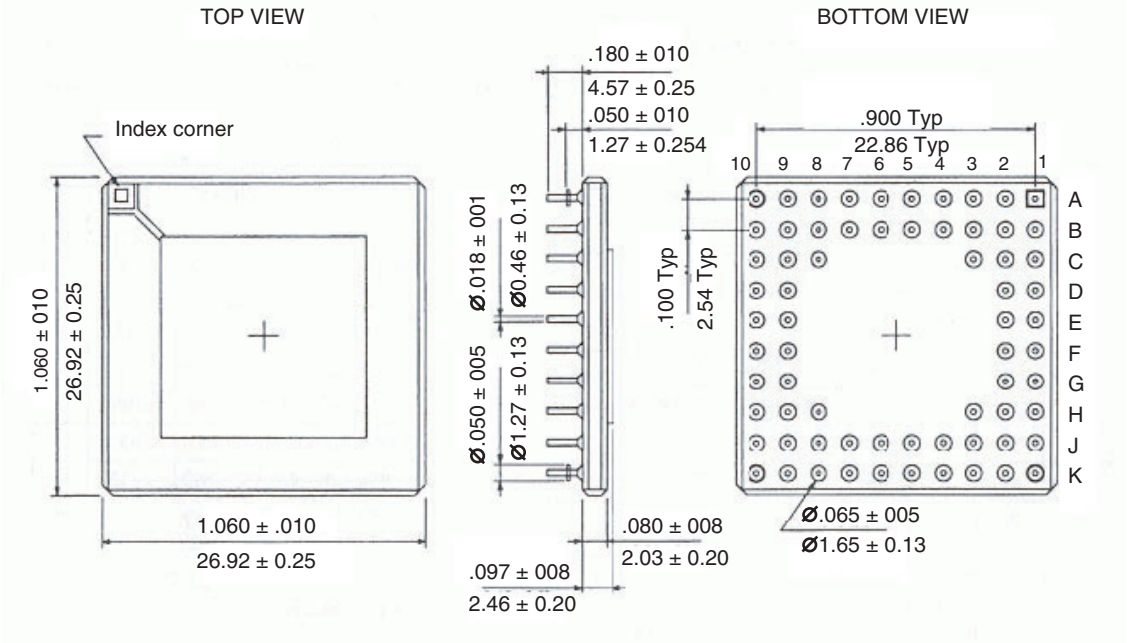
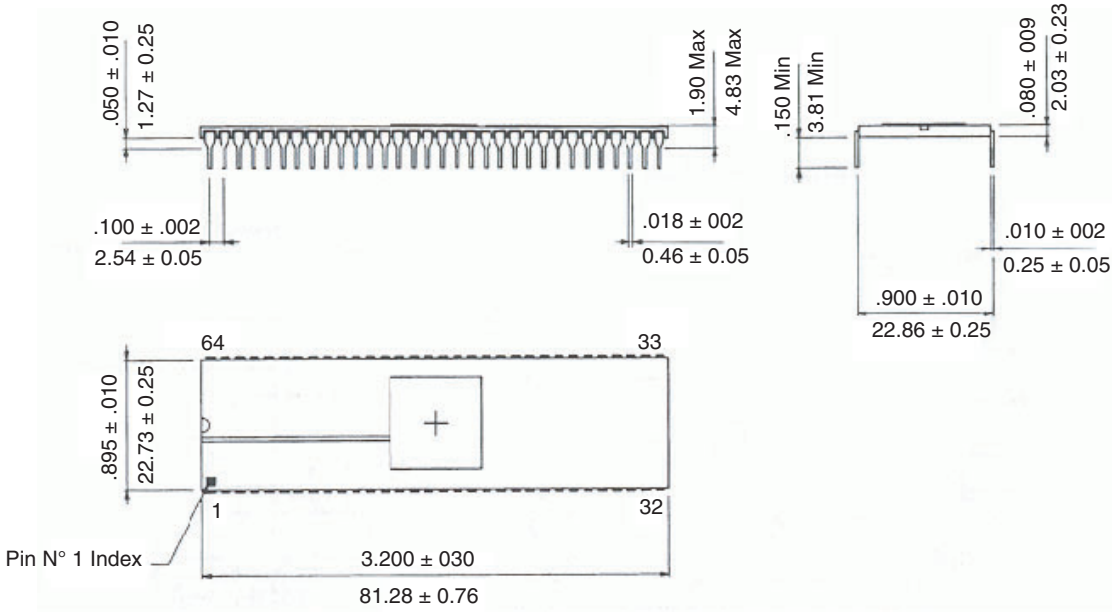
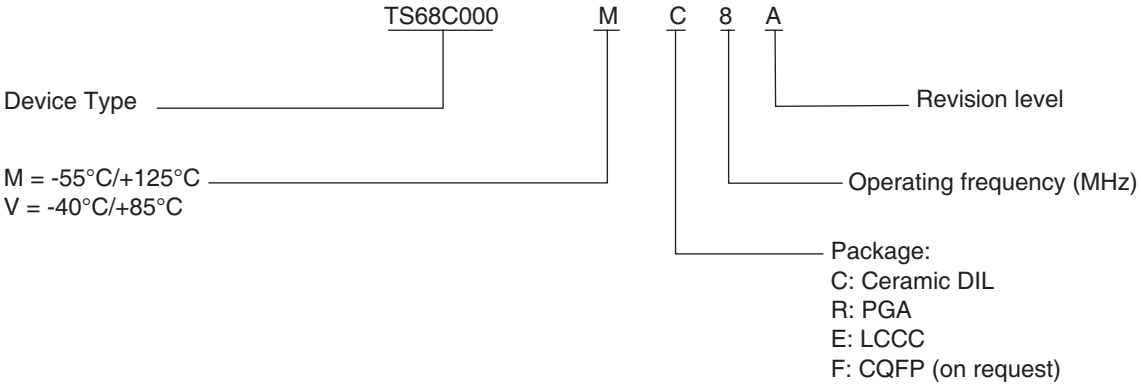


Figure 2-20. 64-lead – Ceramic Side Brazed Package



2.11.3 Standard Product



Note: 1. For availability of the different versions, contact your Atmel sale office.

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