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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	68000
Number of Cores/Bus Width	1 Core, 16/32-Bit
Speed	8MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 85°C (TC)
Security Features	-
Package / Case	68-BCPGA
Supplier Device Package	68-CPGA (26.92x26.92)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts68c000vr8a

Table 2-1. Absolute Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{CC}	Supply voltage		-0.3	+6.5	V
V_I	Input voltage		-0.3	+6.5	V
V_O	Output voltage		NA	NA	V
V_{OZ}	Off state voltage		-0.3	11.0	V
I_O	Output currents		NA	NA	mA
I_i	Input currents		NA	NA	mA
P_{DMAX}	Max power dissipation	T_{CASE} = -55°C		0.27	W
		T_{CASE} = +125°C		0.27	W
T_{STG}	Storage temperature		-55	+150	°C
T_J	Junction temperature			+150	°C
T_{LEADS}	Lead temperature	Max 5 sec. Soldering		+270	°C

2.4.4.2 Recommended Condition of Use and Guaranteed Characteristics

- Guaranteed Characteristics (Table 2-5 and Table 2-8)

  The characteristics associated to a specified measurement in the detail specification shall only be for inspection purposes.

  Such characteristic defined in this specification is guaranteed only under the conditions and within the limits which are specified for the relevant measurement. Unless otherwise specified, this guarantee applies within all the recommended operating ranges specified below.

- Recommended conditions of use (Table 2-2)

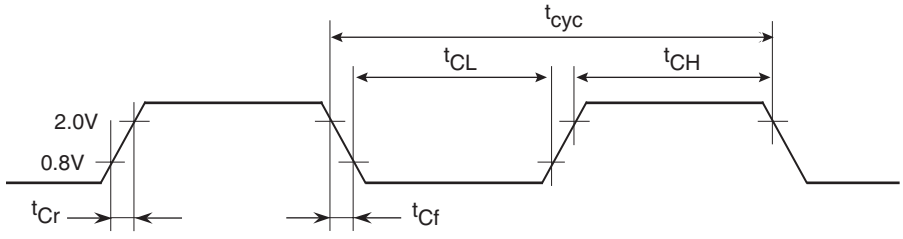
  To the correct operation of the device, the conditions of use shall be within the ranges specified below (see also above).

  These conditions shall not be for inspection purposes.

  Some recommended values may, however, be taken in other parts of this specification as detail conditions for an applicable test (Table 2-9).

- Additional Electrical Characteristics (Table 2-9), see "Additional Electrical Characteristics" on page 30.

Figure 2-1. Clock Input Timing Diagram



Note: Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside, and pass through, the range such that the rise of fall will be linear between 0.8V and 2.0V.

Unless otherwise stated, all voltages are referenced to the reference terminal (see Table 1-1).

These terms are related by the equation:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JA} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals $\theta_{JC.}$ Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

2.4.6 Mechanical and Environmental

The microcircuits shall meet all mechanical environmental requirements of MIL-STD-883 for class B devices.

2.4.7 Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit is legible and permanently marked with the following information as minimum:

- Atmel Logo
- Manufacturer's Part Number
- Class B Identification
- Date-code of inspection lot
- ESD Identifier if Available
- Country of Manufacturing

2.5 Quality Conformance Inspection

2.5.1 DESC/MIL-STD-883

Is in accordance with MIL-PRF-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

2.6 Electrical Characteristics

2.6.1 General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurements conditions are given below:

- Table 2-4: Static Electrical Characteristics for all electrical variants.
- Table 2-5, Table 2-6, Table 2-7 and Table 2-8: Dynamic electrical characteristics for 8 MHz, 10 MHz and 12.5 MHz.

For static characteristics (Table 2-4), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to clause "Test Conditions Specific to the Device" on page 26 of this specification (Table 2-5, Table 2-6, Table 2-7 and Table 2-8).

Indication of "min" or "max" in the column "test temperature" means minimum or maximum operating temperatures as defined in sub-clause "Recommended Condition of Use and Guaranteed Characteristics" on page 11 here above.

Table 2-4. Static Characteristics

V_{CC} = 5.0V V_{DC} ± 10%; GND = 0 V_{DC}; Tc = -55/+125°C and -40°C/+85°C

Test Number	Symbol	Parameter	Ref Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
1	I_{CC}	Supply current	41	V_{CC} = 5.5V F_C = 8 MHz F_C = 10 MHz F_C = 12 MHz	All		42 45 50	mA
2	V_{OL} (1)	Low level output voltage for: A1 to A23 FC0 to FC2; $\overline{BG}$	37	V_{CC} = 4.5V I_{OL} = 3.2 mA	25°C max min		0.5	V
3	V_{OL} (2)	Low level output voltage for: $\overline{HALT}$	37	V_{CC} = 4.5V I_{OL} = 1.6 mA	25°C max min		0.5	V
4	V_{OL} (3)	Low level output voltage for: $\overline{AS}$; R/$\overline{W}$: D0 to D15 UDS; $\overline{LDS}$; $\overline{VMA}$ and E	37	V_{CC} = 4.5V I_{OL} = 5.3 mA	25°C max min		0.5	V
5	V_{OL} (4)	Low level output voltage for: $\overline{RESET}$	37	V_{CC} = 4.5V I_{OL} = 5.0 mA	25°C max min		0.5	V
6	V_{OH}	High level output voltage for all outputs	37	V_{CC} = 4.5V I_{OH} = -400 µA	25°C max min	2.4	V_{CC} – 0.75	V
7	I_{IH} (1)	High level input current for all inputs excepted $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5V V_I = 5.5V	25°C max min		2.5	µA
8	I_{IL} (1)	Low level input current for all inputs excepted $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5V V_I = 0V	25°C max min	-2.5		µA
9	I_{IH} (2)	High level input current for: $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5V V_I = 5.5V	25°C max min		20	µA
10	I_{IL} (2)	Low level input current for: $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5V V_I = 0V	25°C max min	-20		µA

Table 2-4. Static Characteristics (Continued)
V_{CC} = 5.0V V_{DC} ± 10%; GND = 0 V_{DC}; Tc = -55/+125°C and -40°C/+85°C

Test Number	Symbol	Parameter	Ref Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
11	I_{OHZ}	High level output 3-state leakage current		V_{CC} = 5.5V V_{OH} = 2.4V	25°C max min		20	µA
12	I_{OLZ}	Low level output 3-state leakage current		V_{CC} = 5.5V V_{OL} = 0.4V	25°C max min		20	µA
13	V_{IH}	High level input voltage for all inputs		V_{CC} = 4.5V V_{CC} = 5.5V	25°C max min	2.0		V
14	V_{IL}	Low level input voltage for all inputs		V_{CC} = 4.5V V_{CC} = 5.5V	25°C max min		0.8 0.8 0.8	V V V
14A	C_{IN}	Input capacitance (all inputs)	11	Reverse voltage = 0V f = 1.0 MHz	25°C max min		25 NA NA	pF pF pF
14B	C_{OUT}	Output capacitance (all inputs)	11	Reverse voltage = 0V f = 1.0 MHz	25°C max min		20 NA NA	pF pF pF
14C	V_{TEST}	Internal protection Transient energy rating		See note(9) 5 cycles	25°C	-500	+500	V

Note: * Algebraic values
** Measurement method: see "General Requirements" on page 14 and "Test Conditions Specific to the Device" on page 26.

Referred notes are given on page 25.

Table 2-5. Dynamic Characteristics – TS68C000-8
V_{CC} = 5.0 V_{DC} ± 10%; GND = 0 V_{DC}; Tc = -55/+125°C and Tc = -40°C/+85°C

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
27	t_{SU} (DICL)	Set-up time Data-in to clock low(1)	10 – 11	See "Input and Output Signals for Dynamic Measurements" on page 29 (a) to (c) f_C = 8 MHz	25°C max min	20(10)		ns

Table 2-6. Dynamic Characteristics – TS68C000-10 (Continued)

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits		Unit
						Min (*)	Max (*)	
47	t_{SU} (SBRCL)	Set-up time $\overline{BR}$ low to clock low (1)	10 – 11	Idem test 27	25°C max min	20(10)		ns
47	t_{SU} (SBGCL)	Set-up time $\overline{BGACK}$ low to clock low(1)	10 – 11	Idem test 27	25°C max min	20(10)		ns
47	t_{SU} (SVPACL)	Set-up time $\overline{VPA}$ low to clock low (1)	10 – 11	Idem test 27	25°C max min	20(10)		ns
47	t_{SU} (SBERCL)	Set-up time $\overline{BERR}$ low to clock low(1)	10 – 11	Idem test 27	25°C max min	20(10)		ns
2	t_w (CL)	Clock width low	10 – 11	Idem test 27	25°C max min	45	125	ns
3	t_w (CH)	Clock width high	10 – 11	Idem test 27	25°C max min	45	125	ns
6A	t_{PLH} t_{PHL} (CHFCV)	Propagation time clock high to FC valid	10 – 11	Idem test 27 Load: 3	25°C max min		60	ns
9	t_{PHL} (CHSLX)	Propagation time clock high to AS low	10 – 11	Idem test 27 Load: 4	25°C max min		55(3)	ns
9	t_{PHL} (CHSL)	Propagation time CLK high to LDS, UDS low	10 – 11	Idem test 27 Load: 4	25°C max min		55(3)	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to AS high	10 – 11	Idem test 27 Load: 4	25°C max min		55(3)	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to LDS, UDS high	10 – 11	Idem test 27 Load: 4	25°C max min		55(3)	ns

Table 2-6. Dynamic Characteristics – TS68C000-10 (Continued)

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
35	t_{PHL} (BRLGL)	Propagation time BR low to BG low	12	Idem test 27 Load: 3	25°C	1.5	3.5	CLKS (2)
					max			
					min		+80	ns
37	t_{PLH} (GALGH)	Propagation time BGACK low to BG high	12	Idem test 27 Load: 3	25°C	1.5	3.5	CLKS (2)
					max			
					min		+80	ns
48	t_{SU} (BELDAL)	Set-up time BERR low to DTACK low	11	Idem test 27	25°C	20(5)		ns
					max			
					min			
48	t_{SU} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	10 – 11	Idem test 27	25°C	20(5)		ns
					max			
					min			
26	t_H (DOSL)	Hold time Data-out valid to $\overline{LDS}$, $\overline{UDS}$ low	11	Idem test 27 Load: 4	25°C	20(4)		ns
					max			
					min			

Note: * Algebraic values
** Measurement method: see "General Requirements" on page 14 and "Test Conditions Specific to the Device" on page 26

Referred notes are given on page 25.

Table 2-7. Dynamic Characteristics – TS68C000-12

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits Min (*)	Limits Max (*)	Unit
27	t_{SU} (DICL)	Set-up time Data-in to clock low(1)	10 – 11	See "Input and Output Signals for Dynamic Measurements" on page 29 (a) to (c) f_C = 12 MHz	25°C	10(10)		ns
					max			
					min			
47	t_{SU} (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low(1)	10 – 11	Idem test 27	25°C	20(10)		ns
					max			
					min			
47	t_{SU} (SBRCL)	Set-up time $\overline{BR}$ low to clock low(1)	10 – 11	Idem test 27	25°C	20(10)		ns
					max			
					min			

Table 2-7. Dynamic Characteristics – TS68C000-12 (Continued)

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits		Unit
						Min (*)	Max (*)	
20	t_{PHL} (CHRL)	Propagation time CLK high to R/$\overline{W}$ low	11	Idem test 27 Load: 4	25°C		60[3]	ns
					max			
					min			
23	t_{PZL} t_{PZH} (CLDO)	Propagation time CLK low to Data-out valid	11	Idem test 27 Load: 4	25°C		55[3]	ns
					max			
					min			
6	t_{PZL} t_{PZH} (CLAV)	Propagation time CLK low to Address valid	10 – 11	Idem test 27 Load: 4	25°C		55	ns
					max			
					min			
32	t_{HRRF}	$\overline{RESET}$/$\overline{HALT}$ transition time	10 – 11	Idem test 27	25°C		150	ns
					max			
					min			
33	t_{PHL} (CHGL)	Propagation time CLK high to $\overline{BG}$ low	8 – 9	Idem test 27 Load: 3	25°C		50	ns
					max			
					min			
34	t_{PLH} (CHGH)	Propagation time CLK high to $\overline{BG}$ high	12	Idem test 27 Load: 3	25°C		50	ns
					max			
					min			
40	t_{PHL} (CLVM)	Propagation time CLK low to $\overline{VMA}$ low	13	Idem test 27 Load: 4	25°C		70	ns
					max			
					min			
41	t_{PHL} (CLE)	Propagation time CLK low to E low	13	Idem test 27 Load: 4	25°C		45	ns
					max			
					min			
8	t_H (SHAZ)	Hold time CLK high to Address	10 – 11	Idem test 27 Load: 3	25°C	0		ns
					max			
					min			
11	t_{SU} (AVSL)	Set-up time Address valid to $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ low	10 – 11	Idem test 27 Load: 4	25°C	15[4]		ns
					max			
					min			
35	t_{PHL} (BRLGL)	Propagation time $\overline{BR}$ low to $\overline{BG}$ low	12	Idem test 27 Load: 3	25°C	1.5	3.5	CLKS [2]
					max			
					min		+70	ns

Table 2-7. Dynamic Characteristics – TS68C000-12 (Continued)

Test Number	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temperature	Limits		Unit
						Min (*)	Max (*)	
37	t_{PLH} (GALGH)	Propagation time $\overline{BGACK}$ low to $\overline{BG}$ high	12	Idem test 27 Load: 3	25°C	1.5	3.5	CLKS (2)
					max			
					min		+70	ns
48	t_{SU} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	11	Idem test 27	25°C	20(5)		ns
					max			
					min			
48	t_{SU} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	10 – 11	Idem test 27	25°C	20(5)		ns
					max			
					min			
26	t_H (DOSL)	Hold time Data-out valid to $\overline{LDS}$, $\overline{UDS}$ low	11	Idem test 27 Load: 4	25°C	15(4)		ns
					max			
					min			

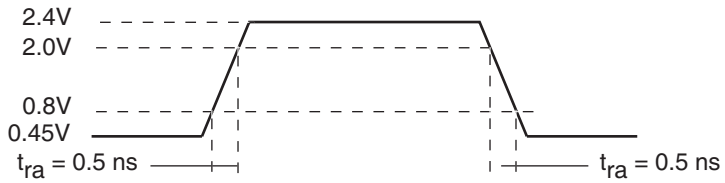
Note: * Algebraic values
** Measurement method: see "General Requirements" on page 14 and "Test Conditions Specific to the Device" on page 26

2.6.1.1 Referred notes to Table 2-4, Table 2-5, Table 2-6, Table 2-7

The following notes shall apply where referred into Table 2-4, Table 2-5, Table 2-6 and Table 2-7.

Notes:
1. If the asynchronous setup tlme (47) requirements are satisfied, the $\overline{DTACK}$ low-to-data setup time (31) requirement Gan be ignored. The data must only satisfy the data-in to clock-low setup time (27) for the following cycle.
2. Where "CLKS" is stated as unit time limit, the relevant time in nanoseconds shall be calculated as the actual cycle time of clock signal input multiply by the given number of CLKS limits.
3. For a loading capacitance of less than or equal to 50 picofarads, substrate 5 nanoseconds from the value given in the maximum columns.
4. Actual value depends on period.
5. If 47 is satisfied for bath $\overline{DTACK}$ and $\overline{BERR}$, 48 may be 0 nanoseconds.
6. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
7. The falling edge of 56 triggers bath the negation of the strobes ($\overline{AS}$, and X DS) and the falling edge of E. either of these events can occur first depending upon the loading on each signal. Specification 49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.
8. When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (±20%), substrate 10 nanoseconds from the values in these columns.
9. Each terminal of the device under test shall be tested separately against all existing VCC and VSS terminals of the device which shall be shorted together for the test. The other untested terminals shall be unconnected during the test. One cycle consists of the application of the bath limits as given in Table 2-5, Table 2-6 and Table 2-7.
10. This value should be treated as a min for design purpose. For the conformance testing the value shall be regarded as the maximum time.

Figure 2-8. Input Pulse Characteristics



2. Time measurement input voltage references

Input voltages which are taken as reference for time measurement shall be:

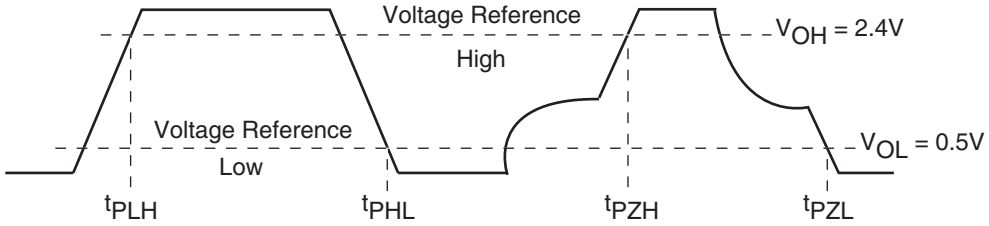
V_{IL} = 0.8V

V_{IH} = 2.0V

3. Time measurement input voltage references

Where output is (or becomes to) valid state, the output voltages which are taken as reference for time measurements, shall be as shown in Figure 2-9.

Figure 2-9. Output Voltage References



2.6.3 Additional Information

Additional information shall not be for any inspection purposes.

2.6.3.1 Power Considerations

See "Thermal Characteristics" on page 13.

2.6.3.2 Additional Electrical Characteristics

The following additional characteristics, which are obtained from circuit design, are given for Information only.

Unless otherwise stated, for dynamic additional characteristics, the given reference numbers refer to Figure 2-1 to Figure 2-7 and loading number refer to Figure 2-2 and Figure 2-3 (see "Test Conditions Specific to the Device" on page 26 of this specification).

The given limits should be valid for all operating temperature ranges as defined in "Recommended Condition of Use and Guaranteed Characteristics" on page 11 of this specification.

Included in the register indirect addressing modes is the capability to do post incrementing, predecrementing, offsetting, and indexing. The program counter relative mode can also be modified via Indexing and offsetting.

2.7.3 Data Transfer Operations

Transfer of data between devices involves the following leads:

1. address bus A1 through A23,
2. data bus 00 through D15, and
3. control signals.

The address and data buses are separate parallel buses used to transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing all signals it issues at bath the stan and end of a cycle. In addition, the bus master Is responsible for deskewing the acknowledge and data signals tram the slave device.

The following paragraphs explain the read, write, and read-modify.write cycles. The indivisible read-modify-write cycle is the method used by the TS68C000 for interlocked multiprocessor communications.

2.7.3.1 Read Cycle

During a read cycle, the processor receives data tram the memory of a peripheral devlce. The processor reads bytes of data in all cases. If the instruction specifies a ward (or double ward) operation, the processor reads both upper and lower bytes simultaneously. by asserting both upper and lower data strobes. When the instruction specifies byte operation, the processor uses an internal AO bit to determine which byte to read and then Issues the data strobe required for that byte. For byte operations, when the AO bit equals zero, the upper data strobes is issued. When the AO bit equals one, the lower data strobe is issued. When the data is received, the processor correctly positions is internally.

2.7.3.2 Write Cycle

During a write cycle, the processor sends data to either the memory of a peripheral device. The processor writes bytes of data in all cases. If the instruction specifies a ward operation, the processor writes bath bytes. When the instruction specifies a byte operation, the processor uses an internal AO bit to determine which byte to write and then issues the data strobe required for that byte. For byte operations, when the AO bit equals zero, the upper data strobe is issued. When the AO bit equals one, the lower data strobe is issued.

Table 2-10. Addressing Modes

Addressing Modes	Syntax
Register direct addressing	
Data register direct	Dn
Address register direct	An
Absolute data addressing	
Absolute short	xxx.W
Absolute long	xxx.L
Program counter relative addressing	
Relative with offset	d_{16} (PC)
Relative with index offset	d_8 (PC, Xn)

Table 2-11. Instruction Set Summary

Mnemonic	Description
ABCD	Add Decimal with Extend
ADD	Add
AND	Logical AND
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
Bcc	Branch Conditionally
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BRA	Branch Always
BSET	Bit Test and Set
BSR	Branch to Subroutine
BTST	Bit Test
CHK	Check Register Against Bounds
CLR	Clear Operand
CMP	Compare
DBcc	Test Condition, Decrement and Branch
DIVS	Signed Divide
DIVU	Unsigned Divide
EOR	Exclusive OR
EXG	Exchange Registers
EXT	Sign Extend
JMP	Jump
JSR	Jump to Subroutine
LEA	Lead Effective Address
LINK	Link Stack
LSL	Logical Shift Left
LSR	Logical Shift Right
MOVE	Move
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NOP	No Operation
NOT	One's Complement
OR	Logical OR
PEA	Push Effective Address

Table 2-11. Instruction Set Summary (Continued)

Mnemonic	Description
RESET	Rest External Devices
ROL	Rotate Left without Extend
ROR	Rotate Right without Extend
ROXL	Rotate Left with Extend
ROXR	Rotate Right with Extend
RTE	Return from Exception
RTR	Return and Restore
RTS	Return form Subroutine
SBCD	Subtract Decimal with Extend
Scc	Set Conditional
STOP	Stop
SUB	Subtract
SWAP	Swap Data Register Halves
TAS	Test and Set Operand
TRAP	Trap
TRAPV	Trap on Overflow
TST	Test
UNLK	Unlink

2.7.3.3 Read Modify Write Cycle

The read-modify-write cycle performs a read, modifies the data in the arithmetic-logic unit, and writes the data back to the same address. In the TS68C000, this cycle is indivisible in that the address strobe is asserted throughout the entire cycle. The test and set (TAS) instruction uses this cycle to provide meaningful communication between processors in a multiple processor environment. This Instruction is the only instruction that uses the read-modify-write cycles and since the test and set instruction only operates on bytes, all read-modify-write are byte operations.

2.7.4 Instruction Set Overview

The TS68C000 instruction set is shown in Table 2-11. Some additional instructions are variations, or sub-sets, of these and they appear in Table 2-12. Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the 14 addressing modes. Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned, multiply and divide, "quick" arithmetic operations, BCD arithmetic, and expanded operations (through traps).

2.7.5 Processing States

The TS68C000 is always in one of three processing states: normal, exception, or halted.

2.7.5.1 Normal Processing

The normal processing state is that associated with instruction execution; the memory references are to fetch instructions and operands, and to store results. A special case of normal state is the stopped state which the processor enters when a stop instruction is executed. In this state, no further references are made.

2.7.5.2 Exception Processing

The exception processing state is associated with interrupts, trap instructions, tracing, and other exception conditions. The exception may be internally generated by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, by a bus error, or by a reset. Exception processing is designed to provide an efficient context switch so that the processor may handle unusual conditions.

2.7.5.3 Halted Processing

The halted processing state is an Indication of catastrophic hardware failure. For example, if during the exception processing of a bus error another bus errors occurs, the processor assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a processor in the stopped state is not in the halted state, nor vice versa.

Asserting the reset and halt line for ten cycles will cause a processor reset, except when VCC is initially applied to the processor. In this case, an external reset must be applied for least 100 milliseconds.

2.7.6 Interface with EF 6800 Peripherals

Extensive line of EF6800 peripherals are directly compatible with the TS68C000.

Note: It is the own user's responsibility to verify the actual EF 6800 peripheral performances to be compatible to the actual used TS68C000 microprocessor performances.

Soma of the EF 6800 peripheral that are particularly useful are:

EF6821: Peripheral Interface Adapter

EF6840: Programmable Timer Module

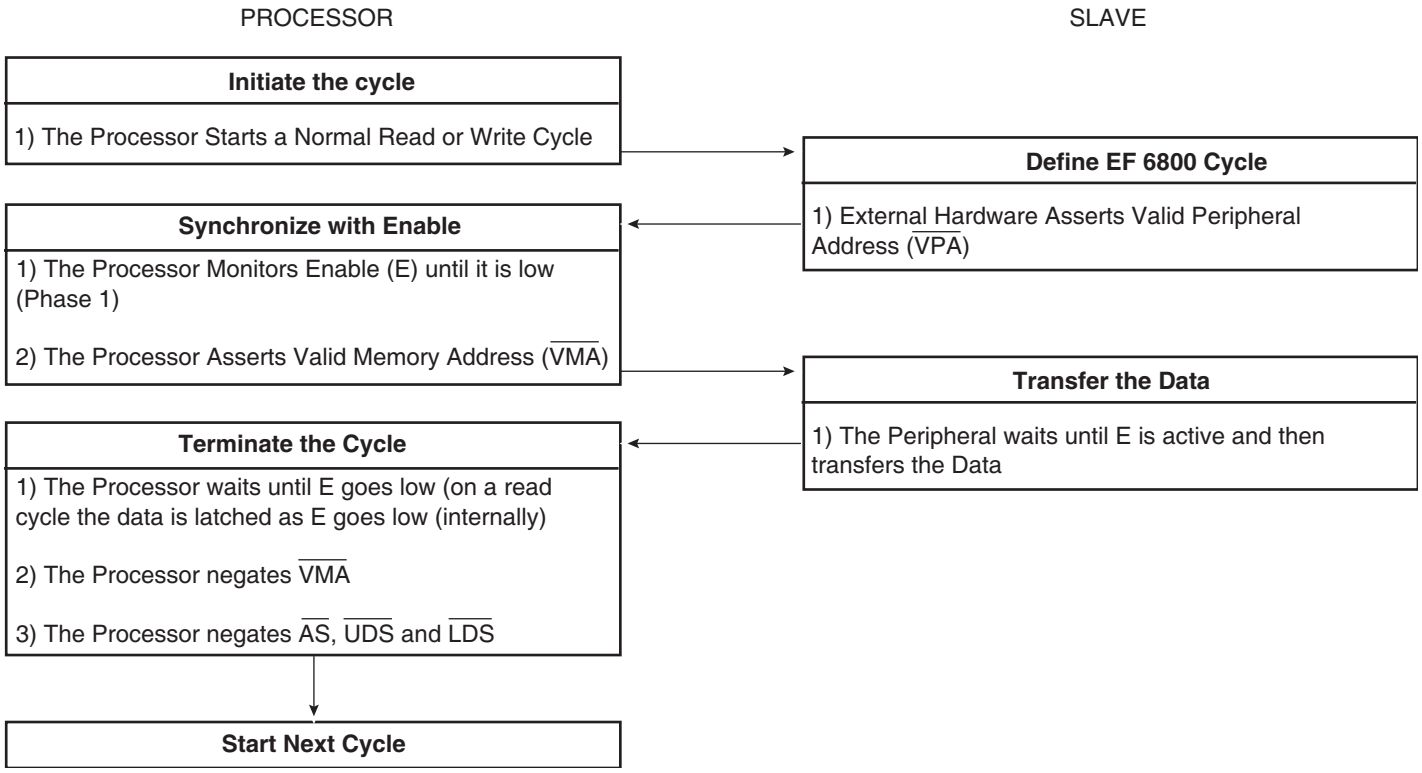
EF6850: Asynchronous Communications Interface Adapter

EF6852: Synchronous Serial Data Adapter

EF6854: Advanced Data Link Controller

To interface the synchronous EF 6800 peripherals with the asynchronous TS68C000, the processor modifies its bus cycle to meet the EF 6800 cycle requirements whenever an EF 6800 device address is detected. This is possible since both processors use memory mapped 1/0. Figure 2-13 is a flowchart of the interface operation between the processor and EF 6800 devices.

Figure 2-13. EF6800 Interfacing Flowchart



2.7.6.1 Data Transfer Operation

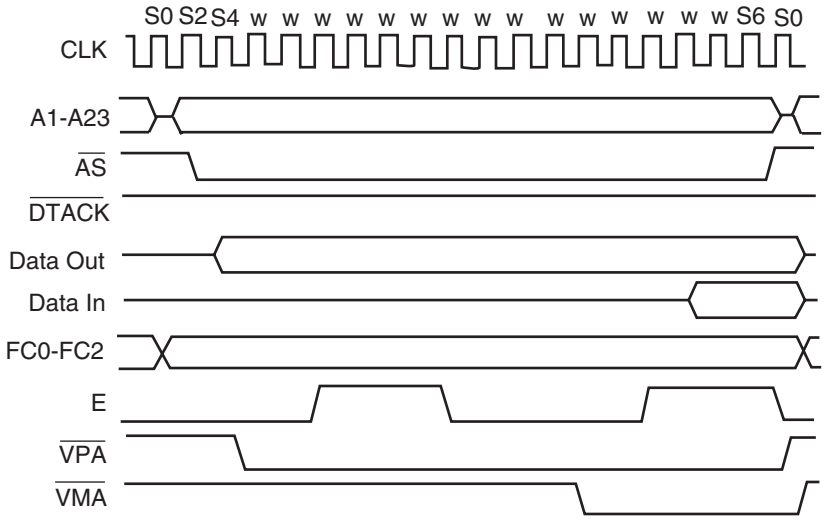
Three signals on processor provide the EF 6800 interface. They are: enable (E), valid memory address (VMA), and valid peripheral address (VPA). Enable corresponds to the E or phase 2 signal i n existing EF 6800 systems. The bus frequency is one tenth of the incoming TS68C000 clock frequency. The timing of E allows 1 MHz peripherals to be used 8 MHz TS68C000. Enable has a 60/40 duty cycle, that is, it is low for six input clocks and high for four input clocks. This duty cycle allows the processor to do successive VPA accesses on successive E pulses.

EF6800 cycle timing is given in Figure 2-17 and Figure 2-18. At state zero (50) in the cycle, the address bus is in the high-impedance state. A function code is asserted on the function code output fines. One-half clock later, in state 1, the address bus is released from the high-impedance state.

During state 2, the address strobe (AS) is asserted to indicate that there Is a valid address on the address bus. If the bus cycle is a read cycle, the upper and/or lower data strobes are also asserted in state 2. If the bus cycle is a write cycle, the read/write (R/W) signal is switched to low (write) during state 2. One-half clock later, in state 3, the write data Is placed on the data bus, and in state 4 the data strobes are issued to indicate valid data on the data bus. The processor now inserts wait states until it recognizes the assertion of VPA.

The VPA input signals the processor that the address on the bus is the address of an EF 6800 device (or an area reserved for EF6800 devices) and that the bus should conform to the phase 2 transfer characteristics of the EF 6800 bus. Valid peripheral address is derived by decoding the address bus, conditioned by the address strobe. Chip select for the EF 6800 peripherals should be derived by decoding the address bus conditioned by VMA.

Figure 2-15. TS68C000 to EF6800 Peripheral Timing – Worst Case



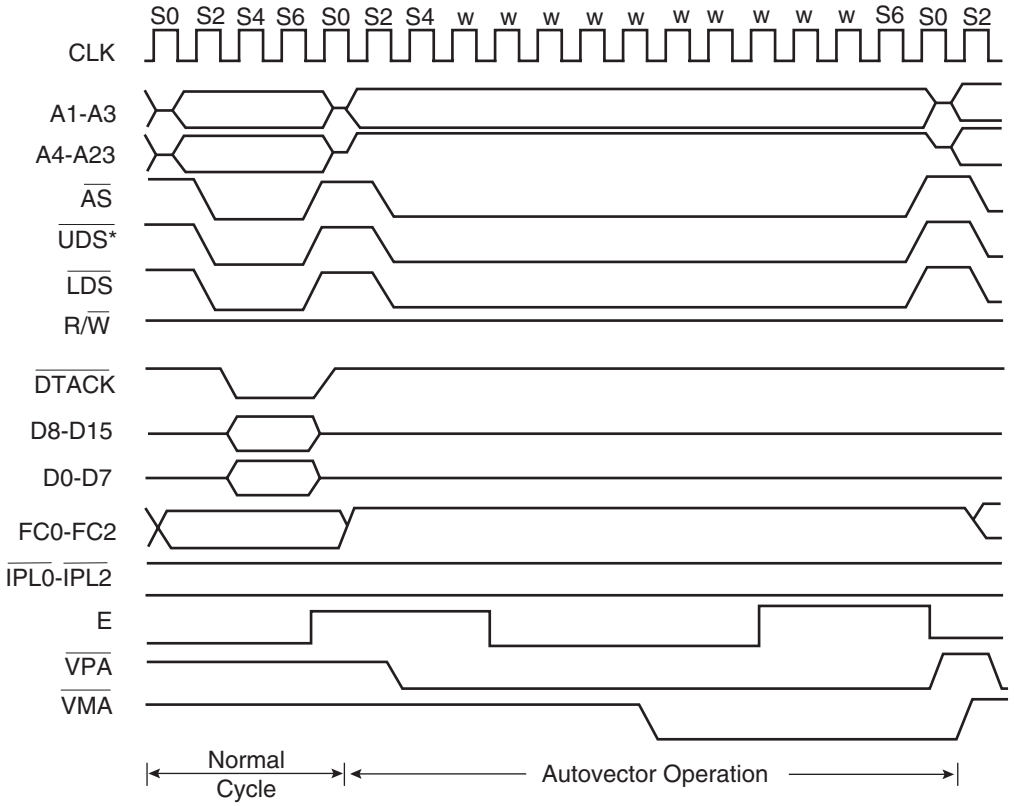
2.7.6.2 Interrupt Interface Operation

During an interrupt acknowledge cycle while the processor is fetching the vector, the $\overline{\text{VPA}}$ is asserted, the TS68C000 will assert $\overline{\text{VMA}}$ and complete a normal EF 6800 read cycle as shown in Figure 2-16. The processor will then use an internally generated vector that is a function of the interrupt being serviced. This process is know as autovectorlng. The seven autovectors are vector number 25 through 31 (decimal).

Autovectoring operates in the same fashion (but is not restricted to) the EF 6800 interrupt sequence. The basic difference is that there are six normal interrupt vectors and one NMI type vector. As with bath the EF 6800 and the TS68C(XX)'s normal vectored interrupt, the Interrupt service routine can be located any-where in the address space. This is due to the tact that while the vector numbers are fixed the contents of the vector table entries are assigned by the user.

Since $\overline{\text{VMA}}$ is asserted during autovectoring. The EF 6800 peripheral address decoding should prevent unintended accesses.

Figure 2-16. Autovector Operation Timing Diagram



Although $\overline{UDS}$ and $\overline{LDS}$ are asserted, no data is read from the bus during the autovector cycle. The vector number is generated internally).

Table 2-13. Dynamic Electrical Characteristics TS68C000 to EF 6800 Peripheral

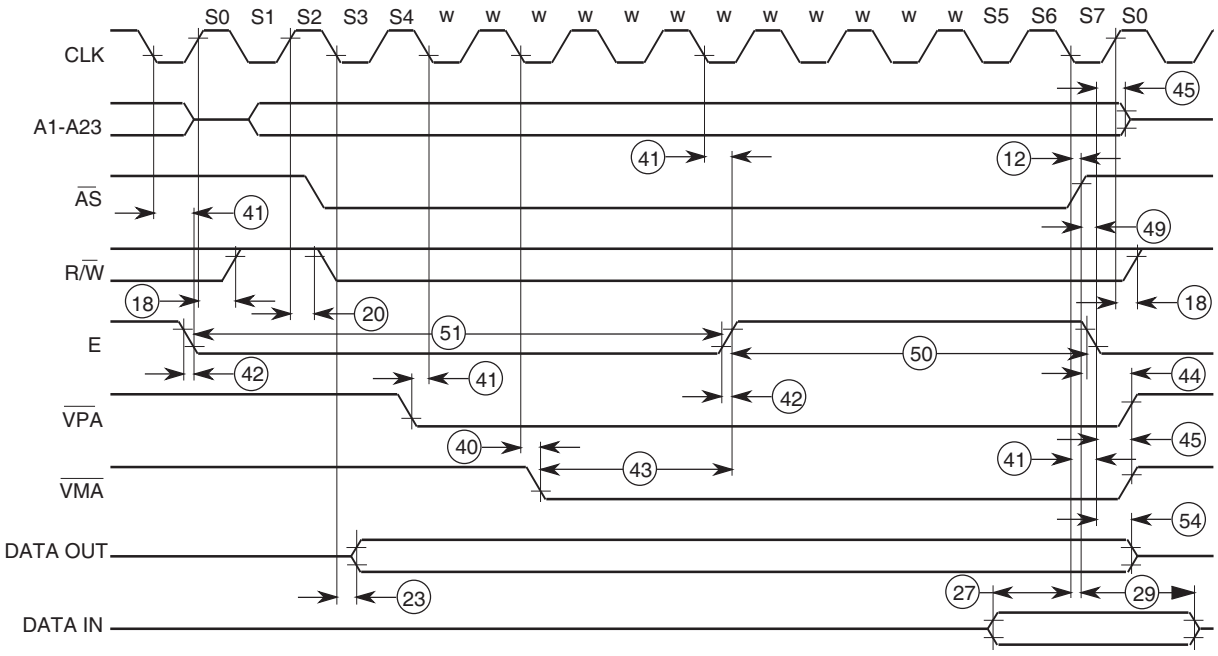
			8 MHz		10 MHz		12.5 MHz		
			Limits		Limits		Limits		
Number	Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit
12	CLSH	Clock low to $\overline{AS}$, $\overline{DS}$ high[1]		70		55		50	ns
18	CHRH	Clock high to R/$\overline{W}$ high[1]	0	70	0	60	0	60	ns
20	CHRL	Clock high to R/$\overline{W}$ low (write)[1]		70		60		60	ns
23	CLDO	Clock low to data out valid (write)		70		55		55	ns
27	CLDO	Data in to clock low (set up time on read)[2]	15		10		10		ns
29	SHDII	$\overline{AS}$, $\overline{DS}$ high to Data in invalid (hold time on read)	0		0		0		ns
40	CLVML	$\overline{AS}$, $\overline{DS}$ high to $\overline{VPA}$ high		70		70		70	ns
41	CLET	Clock low to E transition		70		55		45	ns
42	Erf	E output rise and fall time		25		25		25	ns
43	VMLEH	$\overline{VMA}$ low to E high	200		150		90		ns
44	SHVPH	$\overline{AS}$, $\overline{DS}$ high to $\overline{VPA}$ high	0	120	0	90	0	70	ns

Table 2-13. Dynamic Electrical Characteristics TS68C000 to EF 6800 Peripheral (Continued)

Number	Symbol	Parameter	8 MHz Limits		10 MHz Limits		12.5 MHz Limits		Unit
			Min	Max	Min	Max	Min	Max	
45	ELCAI	E low to control, address bus invalid (address hold time)	30		10		10		ns
47	ASI	Asynchronous input setup time[2]	20		20		20		ns
49	SHEL	$\overline{AS}$, $\overline{DS}$ high to E low[3]	-70	70	-55	55	-80		ns
50	EH	E width high	450		350		280		ns
51	EL	E width low	700		550		440		ns
54	ELDOI	E low to data out invalid	30		20		15		ns

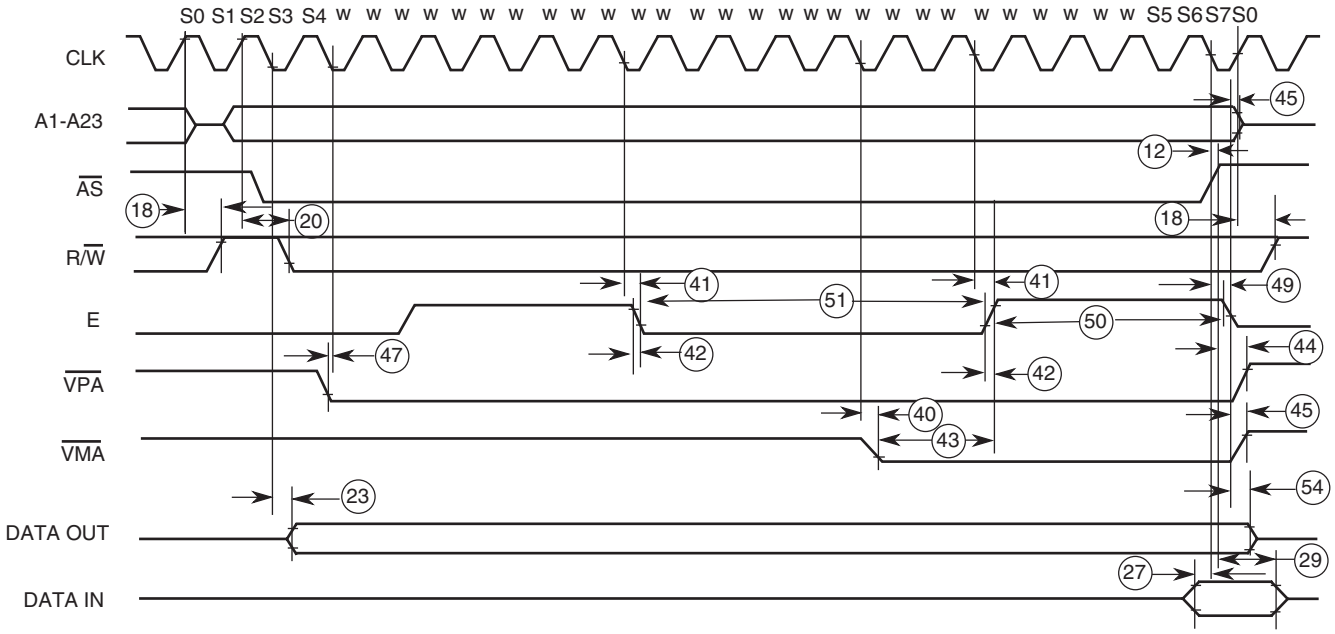
Notes: 1. For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the value given in the maximum columns.
2. If the asynchronous setup time (47) requirements are satisfied, the $\overline{DTACK}$ low-to-data setup time (31) required can be ignored. The data must only satisfy the date in clock-low setup time (27) for the following cycle.
3. The falling edge of S6 triggers both the negation of the strobes ($\overline{AS}$ and X $\overline{DS}$) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal specification 49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.

Figure 2-17. TS68C000 to EF6800 Peripheral Timing Diagram – Best Case



Note: This timing diagram is included for those who wish to design their own circuit to generate $\overline{VMA}$. It shows the worst case possibly attainable.

Figure 2-18. TS68C000 to EF6800 Peripheral Timing Diagram – Worse Case



Note: This timing diagram is included for those who wish to design their own circuit to generate $\overline{VMA}$. It shows the worst case possibly attainable.

2.8 Preparation For Delivery

2.8.1 Packaging

Microcircuit are prepared for delivery in accordance with MIL-PRF-38535.

2.8.2 Certificate of Compliance

Atmel offers a certificate of compliance with each shipment of parts, affirming the products are in compliance with MIL-STD-883 and guarantying the parameters not tested at extreme temperatures for the entire temperature range.

2.9 Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

a) Device should be handled on benches with conductive and grounded surface.

b) Ground test equipment, tools and operator.

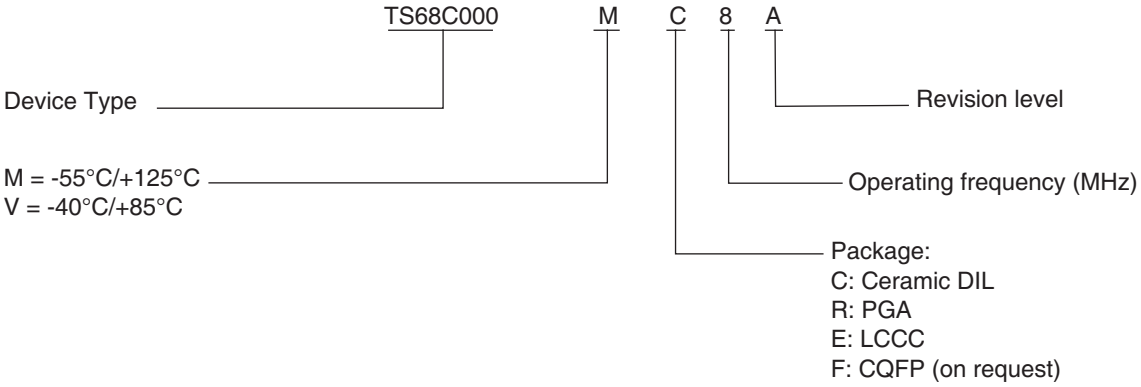
c) Do not handle devices by the leads.

d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

f) Maintain relative humidity above 50%, if practical.

2.11.3 Standard Product



Note: 1. For availability of the different versions, contact your Atmel sale office.

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