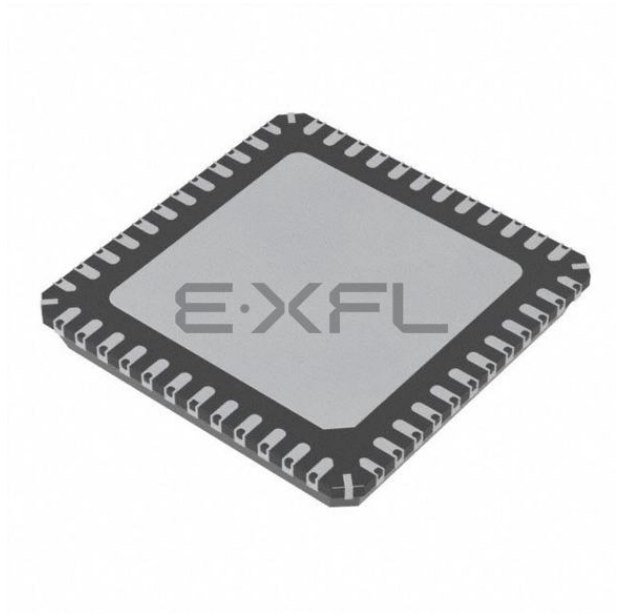

Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	ARM® Cortex®-M3
Program Memory Type	FLASH (128kB)
Controller Series	-
RAM Size	6K x 8
Interface	LIN, SSI, UART
Number of I/O	10
Voltage - Supply	5.5V ~ 28V
Operating Temperature	-40°C ~ 150°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-31
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9879qxa40xuma1

Table of Contents

4 Modes of Operation

This highly integrated circuit contains analog and digital functional blocks. An embedded 32-bit microcontroller is available for system and interface control. On-chip, low-dropout regulators are provided for internal and external power supply. An internal oscillator provides a cost effective clock that is particularly well suited for LIN communications. A LIN transceiver is available as a communication interface. Driver stages for a Motor Bridge or BLDC Motor Bridge with external MOSFET are integrated, featuring PWM capability, protection features and a charge pump for operation at low supply voltage. A 10-bit SAR ADC is implemented for high precision sensor measurement. An 8-bit ADC is used for diagnostic measurements.

The Micro Controller Unit supervision and system protection (including a reset feature) is complemented by a programmable window watchdog. A cyclic wake-up circuit, supply voltage supervision and integrated temperature sensors are available on-chip.

All relevant modules offer power saving modes in order to support automotive applications connected to terminal 30. A wake-up from power-save mode is possible via a LIN bus message, via the monitoring input or using a programmable time period (cyclic wake-up).

Featuring LTI, the integrated circuit is available in a VQFN-48-31 package with 0.5 mm pitch, and is designed to withstand the severe conditions of automotive applications.

The TLE9879QXA40 has several operation modes mainly to support low power consumption requirements.

Reset Mode

The Reset Mode is a transition mode used e.g. during power-up of the device after a power-on reset, or after wake-up from Sleep Mode. In this mode, the on-chip power supplies are enabled and all other modules are initialized. Once the core supply VDDC is stable, the device enters Active Mode. If the watchdog timer WDT1 fails more than four times, the device performs a fail-safe transition to Sleep Mode.

Active Mode

In Active Mode, all modules are activated and the TLE9879QXA40 is fully operational.

Stop Mode

Stop Mode is one of two major low power modes. The transition to the low power modes is performed by setting the corresponding bits in the mode control register. In Stop Mode the embedded microcontroller is still powered, allowing faster wake-up response times. Wake-up from this mode is possible through LIN bus activity, by using the high-voltage monitoring pin or the corresponding 5V GPIOs.

Stop Mode with Cyclic Wake-Up

The Cyclic Wake-Up Mode is a special operating mode of the Stop Mode. The transition to the Cyclic Wake-Up Mode is done by first setting the corresponding bits in the mode control register followed by the Stop Mode command. In addition to the cyclic wake-up behavior (wake-up after a programmable time period), asynchronous wake events via the activated sources (LIN and/or MON) are available, as in normal Stop Mode.

Sleep Mode

The Sleep Mode is a low-power mode. The transition to the low-power mode is done by setting the corresponding bits in the MCU mode control register or in case of failure, see below. In Sleep Mode the embedded microcontroller power supply is deactivated allowing the lowest system power consumption. A wake-up from this mode is possible by LIN bus activity, the High Voltage Monitor Input pin or Cyclic Wake-up.

Sleep Mode in Case of Failure

1) May not be switched off due to safety reasons
2) MC PLL clock disabled, MC supply reduced to 1.1 V

Wake-Up Levels and Transitions

The wake-up can be triggered by rising, falling or both signal edges for the monitor input, by LIN or by cyclic wake-up.

7 System Control Unit - Power Modules (SCU-PM)

7.1 Features

- Clock Watchdog Unit (CWU): supervision of all clocks with NMI signaling relevant to power modules
- Interrupt Control Unit (ICU): all interrupt flags and status flags with system relevance
- Power Control Unit (PCU): takes over control when device enters and exits Sleep and Stop Mode
- External Watchdog (WDT1): independent system watchdog for monitoring system activity

7.2 Introduction

7.2.1 Block Diagram

The System Control Unit of the power modules consists of the sub-modules in the figure shown below:

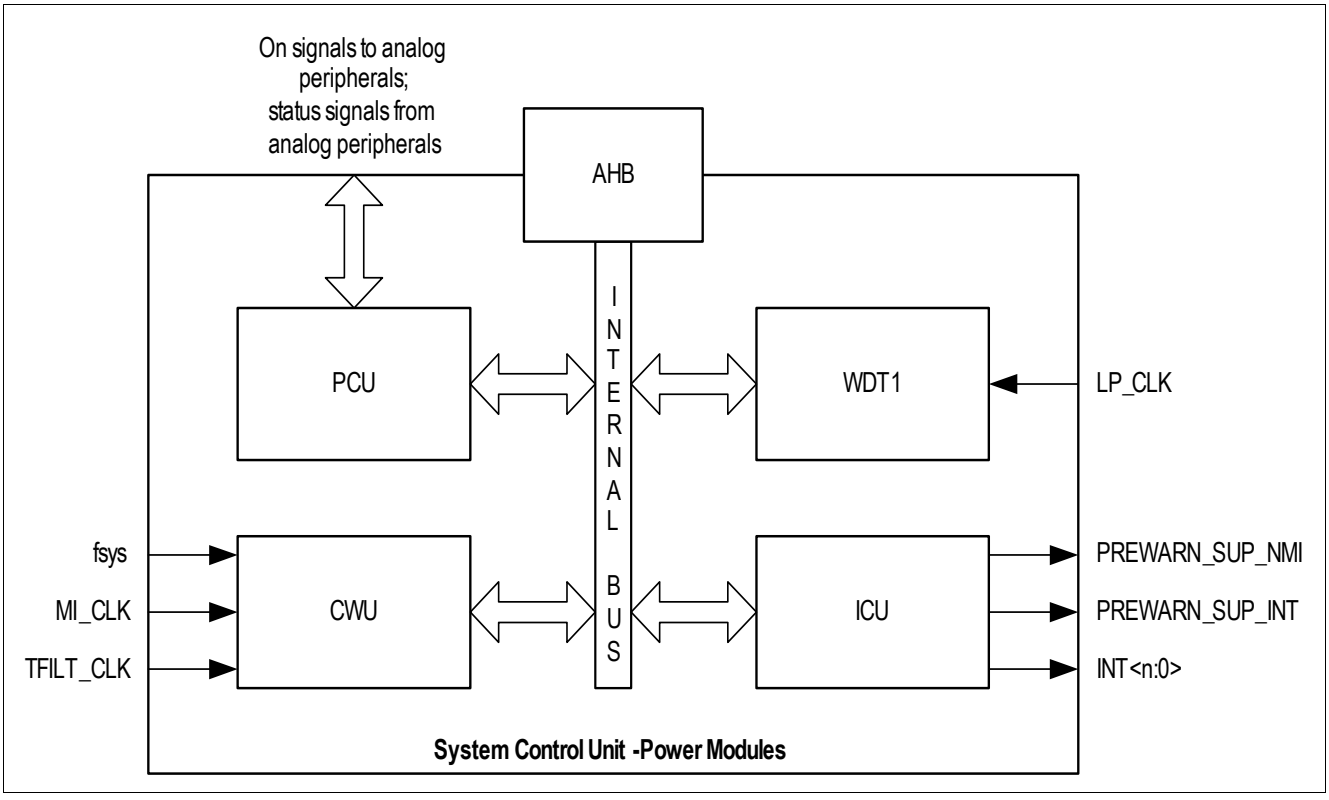

Figure 11 Block diagram of System Control Unit - Power Modules

AHB (Advanced High-Performance Bus)

CWU (Clock Watchdog Unit)

- f_{sys} system frequency: PLL output
- MI_CLK measurement interface clock (analog clock): derived from fsys using division factors 1/2/3/4
- TFILT_CLK clock used for digital filters: derived from fsys using configurable division factors

8.2 Introduction

The ARM Cortex-M3 processor is a leading 32-bit processor and provides a high-performance and cost-optimized platform for a broad range of applications including microcontrollers, automotive body systems and industrial control systems. Like the other Cortex family processors, the Cortex-M3 processor implements the Thumb®-2 instruction set architecture. With the optimized feature set the Cortex-M3 delivers 32-bit performance in an application space that is usually associated with 8- and 16-bit microcontrollers.

8.2.1 Block Diagram

Figure 12 shows the functional blocks of the Cortex-M3.

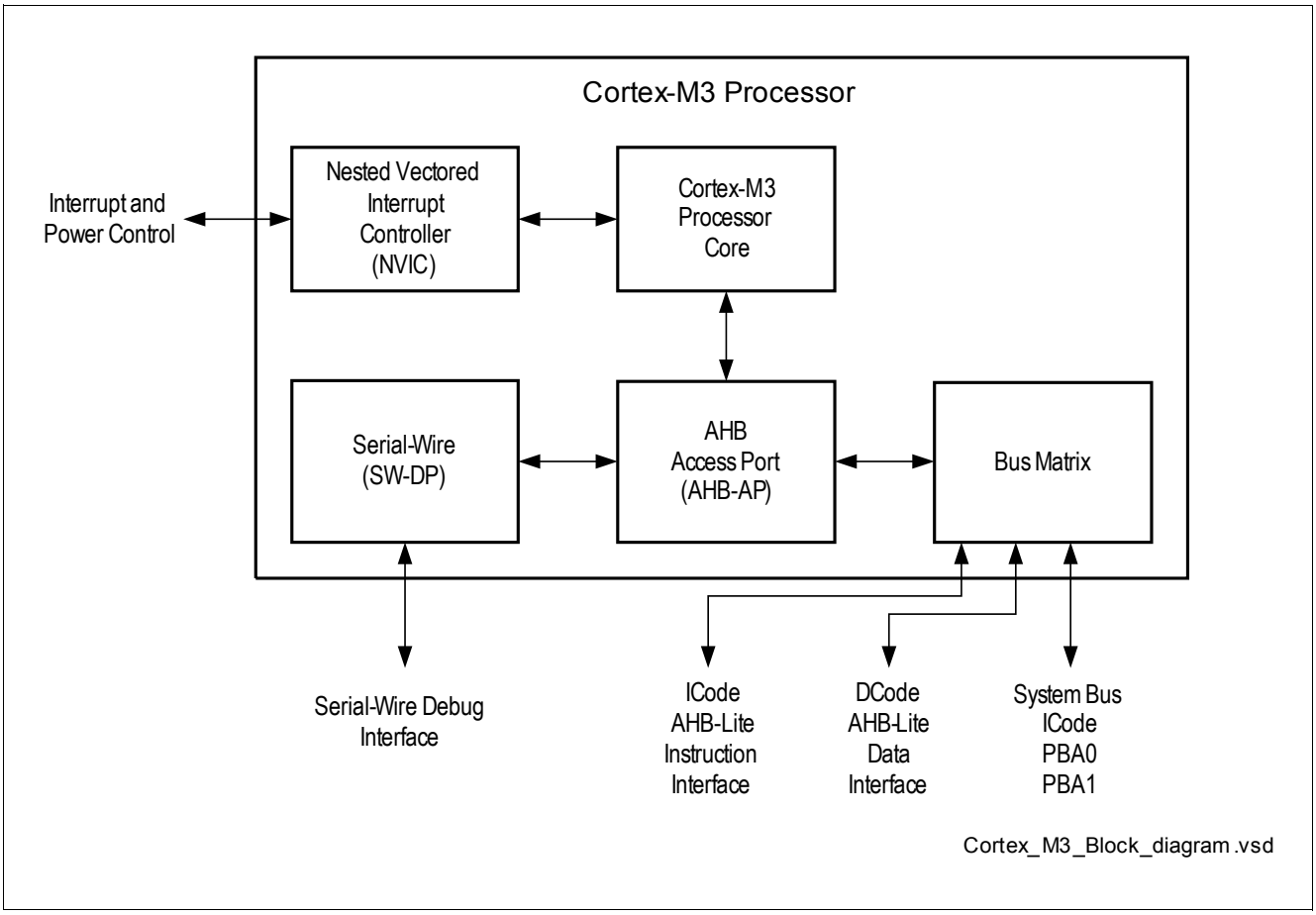

Figure 12 Cortex-M3 Block Diagram

9.3 Functional Description

9.3.1 DMA Mode Overview

The DMA controller implements the following 13 hardware DMA requests:

- ADC1 complete sequence 1 done: DMA transfer is requested on completion of the ADC1 channel conversion sequence.
- ADC1 exceptional sequence 2 (ESM) done: DMA transfer is requested on completion of the ADC1 conversion sequence triggered by an exceptional measurement request.
- SSC1/2 transmit byte: DMA transfer is requested upon the completion of data transmission via SSC1/2
- SSC1/2: receive byte: DMA transfer is requested upon the completion of data reception via SSC1/2.
- ADC1 channel 0 conversion done: DMA transfer is requested on completion of the ADC1 channel 0 conversion.
- ADC1 channel 1 conversion done: DMA transfer is requested on completion of the ADC1 channel 1 conversion.
- ADC1 channel 2 conversion done: DMA transfer is requested on completion of the ADC1 channel 2 conversion.
- ADC1 channel 3 conversion done: DMA transfer is requested on completion of the ADC1 channel 3 conversion.
- ADC1 channel 4 conversion done: DMA transfer is requested on completion of the ADC1 channel 4 conversion.
- ADC1 channel 5 conversion done: DMA transfer is requested on completion of the ADC1 channel 5 conversion.
- ADC1 channel 6 conversion done: DMA transfer is requested on completion of the ADC1 channel 6 conversion.
- ADC1 channel 7 conversion done: DMA transfer is requested on completion of the ADC1 channel 7 conversion.
- Timer3 ccu6_int: DMA transfer is requested following a timer trigger.

12 Interrupt System

12.1 Features

- Up to 16 interrupt nodes for on-chip peripherals
- Up to 8 NMI nodes for critical system events
- Maximum flexibility for all 16 interrupt nodes

12.2 Introduction

Before enabling an interrupt, all corresponding interrupt status flags should be cleared.

12.2.1 Overview

The TLE9879QXA40 supports 16 interrupt vectors with 16 priority levels. Fifteen of these interrupt vectors are assigned to the on-chip peripherals: GPT12, SSC, CCU6, DMA, Bridge Driver and A/D Converter are each assigned to one dedicated interrupt vector; while UART1 and Timer2 or UART2, External Interrupt 2 and Timer21 share interrupt vectors. Two vectors are dedicated for External Interrupt 0 and 1.

Table 6 Interrupt Vector Table

Service Request	Node ID	Description
GPT12	0/1	GPT interrupt (T2-T6, CAPIN)
MU- ADC8/T3	2	Measurement Unit, VBG, Timer3, BEMF
ADC1	3	ADC1 interrupt / VREF5V Overload / VREF5V OV/UV, 10-bit ADC
CCU0	4	CCU6 node 0 interrupt
CCU1	5	CCU6 node 1 interrupt
CCU2	6	CCU6 node 2 interrupt
CCU3	7	CCU6 node 3 interrupt
SSC1	8	SSC1 interrupt (receive, transmit, error)
SSC2	9	SSC2 interrupt (receive, transmit, error)
UART1	10	UART1 (ASC-LIN) interrupt (receive, transmit), Timer2, linsync1, LIN
UART2	11	UART2 interrupt (receive, transmit), Timer21, External interrupt (EINT2)
EXINT0	12	External interrupt (EINT0), MON
EXINT1	13	External interrupt (EINT1)
BDRV/CP	14	Bridge Driver / Charge Pump
DMA	15	DMA Controller

Table 7 NMI Interrupt Table

Service Request	Node	Description
Watchdog Timer NMI	NMI	Watchdog Timer overflow
PLL NMI	NMI	PLL Loss-of-Lock
NVM Operation Complete NMI	NMI	NVM Operation Complete
Overtemperature NMI	NMI	System Overtemperature

14 GPIO Ports and Peripheral I/O

The TLE9879QXA40 has 15 port pins organized into three parallel ports: Port 0 (P0), Port 1 (P1) and Port 2 (P2). Each port pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. P0 and P1 are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected. On Port 2 (P2) analog inputs are shared with general purpose input.

14.1 Features

Bidirectional Port Features (P0, P1)

- Configurable pin direction
- Configurable pull-up/pull-down devices
- Configurable open drain mode
- Configurable drive strength
- Transfer of data through digital inputs and outputs (general purpose I/O)
- Alternate input/output for on-chip peripherals

Analog Port Features (P2)

- Configurable pull-up/pull-down devices
- Transfer of data through digital inputs
- Alternate inputs for on-chip peripherals

14.2 Introduction

14.2.1 Port 0 and Port 1

Figure 17 shows the block diagram of an TLE9879QXA40 bidirectional port pin. Each port pin is equipped with a number of control and data bits, thus enabling very flexible usage of the pin. By defining the contents of the control register, each individual pin can be configured as an input or an output. The user can also configure each pin as an open drain pin with or without internal pull-up/pull-down device.

Each bidirectional port pin can be configured for input or output operation. Switching between input and output mode is accomplished through the register Px_DIR (x = 0 or 1), which enables or disables the output and input drivers. A port pin can only be configured as either input or output mode at any one time.

In input mode (default after reset), the output driver is switched off (high-impedance). The voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt trigger device and can be read via the register Px_DATA.

In output mode, the output driver is activated and drives the value supplied through the multiplexer to the port pin. In the output driver, each port line can be switched to open drain mode or normal mode (push-pull mode) via the register Px_OD.

The output multiplexer in front of the output driver enables the port output function to be used for different purposes. If the pin is used for general purpose output, the multiplexer is switched by software to the data register Px_DATA. Software can set or clear the bit in Px_DATA and therefore directly influence the state of the port pin. If an on-chip peripheral uses the pin for output signals, alternate output lines (AltDataOut) can be switched via the multiplexer to the output driver circuitry. Selection of the alternate output function is defined in registers Px_ALTSEL0 and Px_ALTSEL1. When a port pin is used as an alternate function, its direction must be set accordingly in the register Px_DIR.

15.2.1 Block Diagram GPT1

Block GPT1 contains three timers/counters: The core timer T3 and the two auxiliary timers T2 and T4. The maximum resolution is $f_{GPT}/4$. The auxiliary timers of GPT1 may optionally be configured as reload or capture registers for the core timer.

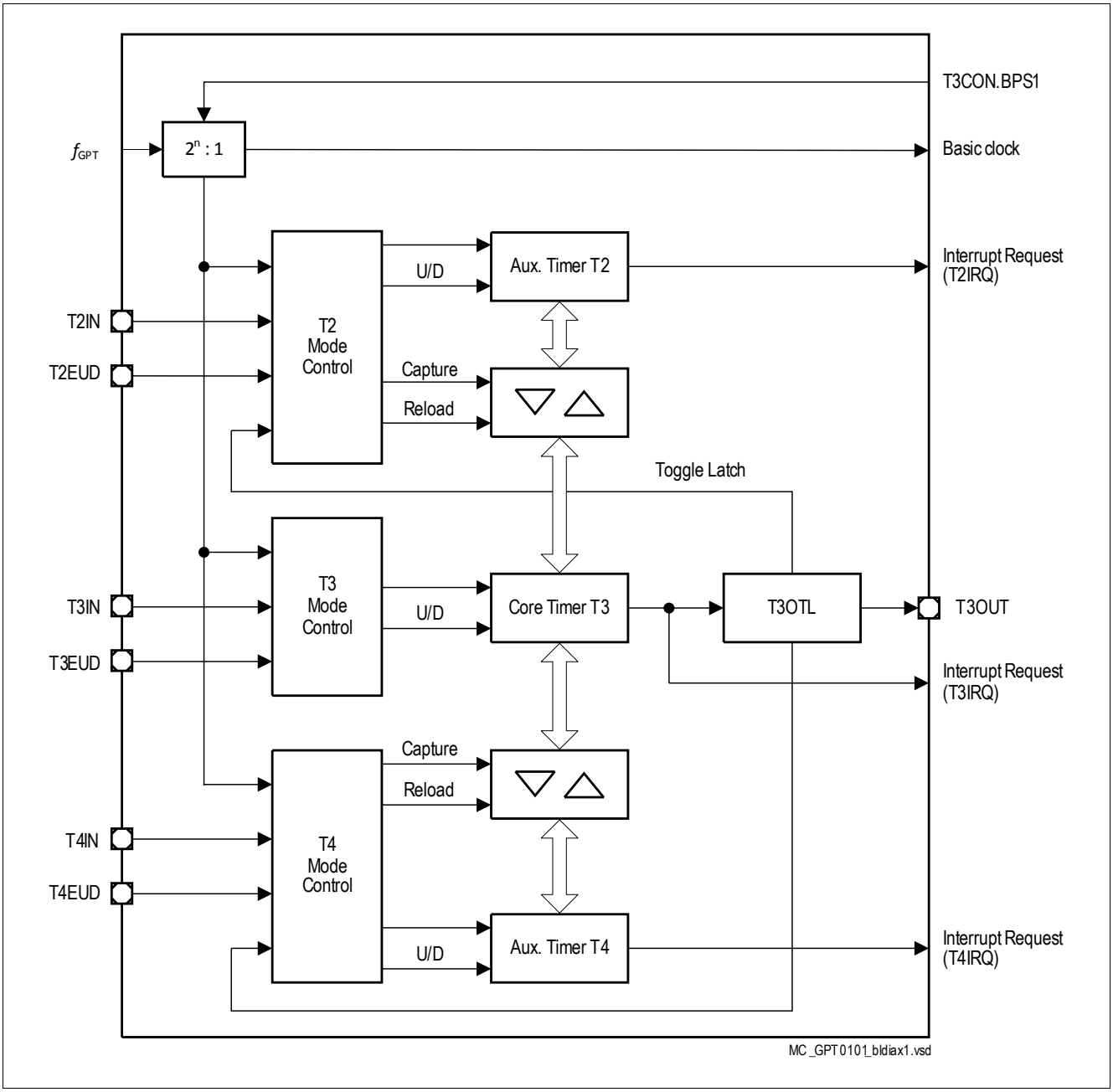

Figure 19 GPT1 Block Diagram (n = 2 … 5)

Note: The capture/compare module itself is referred to as CCU6 (capture/compare unit 6). A capture/compare channel inside this module is referred to as CC6x.

The timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined (e.g. a channel works in compare mode, whereas another channel works in capture mode). The timer T13 can work in compare mode only. The multi-channel control unit generates output patterns which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

18.2.1 Block Diagram

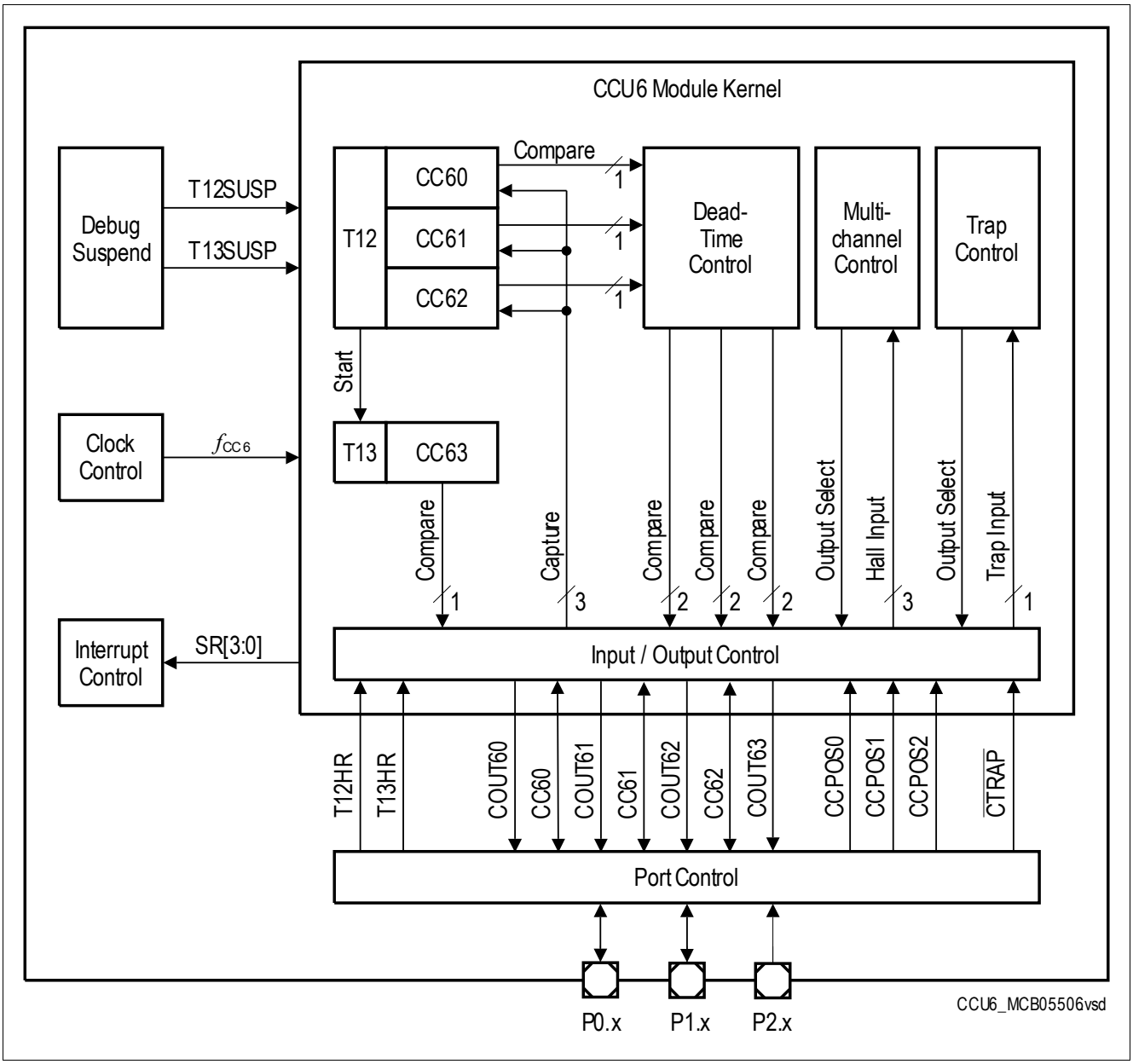

Figure 21 CCU6 Block Diagram

20 LIN Transceiver

20.1 Features

General Functional Features

- Compliant to LIN2.2 standard, backward compatible to LIN1.3, LIN2.0 and LIN 2.1
- Compliant to SAE J2602 (slew rate, receiver hysteresis)

Special Features

- Measurement of LIN master baudrate via Timer 2
- LIN can be used as input/output with SFR bits.
- TxD timeout feature (optional, on by default)

Operation Mode Features

- LIN Sleep Mode (LSLM)
- LIN Receive-Only Mode (LROM)
- LIN Normal Mode (LNM)
- High Voltage Input / Output Mode (LHVIO)

Supported Baud Rates

- Mode for a transmission up to 10.4 kBaud
- Mode for a transmission up to 20 kBaud
- Mode for a transmission up to 40 kBaud
- Mode for a transmission up to 115.2 kBaud

Slope Mode Features

- Normal Slope Mode (20 kbit/s)
- Low Slope Mode (10.4 kbit/s)
- Flash Mode (115.2 kbit/s)

Wake-Up Features

- LIN bus wake-up

22 Measurement Unit

22.1 Features

- 1 x 8-bit ADC with 10 Inputs including attenuator allowing measurement of high voltage input signals
- Supply Voltage Attenuators with attenuation of **VS**, **VDDP** and **VDDC**.
- VBG monitoring of 8-bit ADC to guarantee functional safety requirements.
- Bridge Driver Diagnosis Measurement (VDH, VCP).
- Temperature Sensor for monitoring the chip temperature and PMU Regulator temperature.
- BEMF Comparators for commutation triggering inside BLDC Applications.
- Supplement Block with Reference Voltage Generation, Bias Current Generation, Voltage Buffer for NVM Reference Voltage, Voltage Buffer for Analog Module Reference Voltage and Test Interface.

22.2 Introduction

The measurement unit is a functional unit that comprises the following associated sub-modules:

Table 14 Measurement Functions and Associated Modules

Module Name	Modules	Functions
Central Functions Unit	Bandgap reference circuit	The bandgap-reference sub-module provides two reference voltages 1. a trimmable reference voltage for the 8-bit ADCs. A local dedicated bandgap circuit is implemented to avoid deterioration of the reference voltage arising e.g. from crosstalk or ground voltage shift. 2. the reference voltage for the NVM module
8-bit ADC (ADC2)	8-bit ADC module with 10 multiplexed inputs, including HV input attenuator	5 high voltage full supply range capable inputs (2.5V...30,7V(FS)) 2 medium voltage inputs (0..5V/7V FS). 3 low voltage inputs (0..1.2V/1.6V FS) (allocation see following overview figure)
10-bit ADC (ADC1)	10-bit ADC module with 8 multiplexed inputs	Five (5V) analog inputs from Port 2.x
VDH Input Voltage Attenuator	VDH input voltage attenuator	Scales down V(VDH) to the input voltage range of ADC1.CH6
Temperature Sensor	Temperature sensor with two multiplexed sensing elements: • PMU located sensor • Central chip located sensor	Generates output voltage which is a linear function of the local chip (junction) temperature.

24 10-Bit Analog Digital Converter (ADC1)

24.1 Features

The principal features of the ADC1 are:

- Up to 8 analog input channels (channel 7 reserved for future use)
- Flexible results handling
  - 8-bit and 10-bit resolution
- Flexible source selection due to sequencer
  - insert one exceptional sequence (ESM)
  - insert one interrupt measurement into the current sequence (EIM), single or up to 128 times
  - software mode
- Conversion sample time (separate for each channel) adjustable to adapt to sensors and reference
- Standard external reference (VAREF) to support ratiometric measurements and different signal scales
- DMA support, transfer ADC conversion results via DMA into RAM
- Support of suspend and power saving modes
- Result data protection for slow CPU access (wait-for-read mode)
- Programmable clock divider
- Integrated sample and hold circuitry

24.2 Introduction

The TLE9879QXA40 includes a high-performance 10-bit Analog-to-Digital Converter (ADC1) with eight multiplexed analog input channels. The ADC1 uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC1 are available at AN0, AN2 - AN5.

24.2.1 Block Diagram

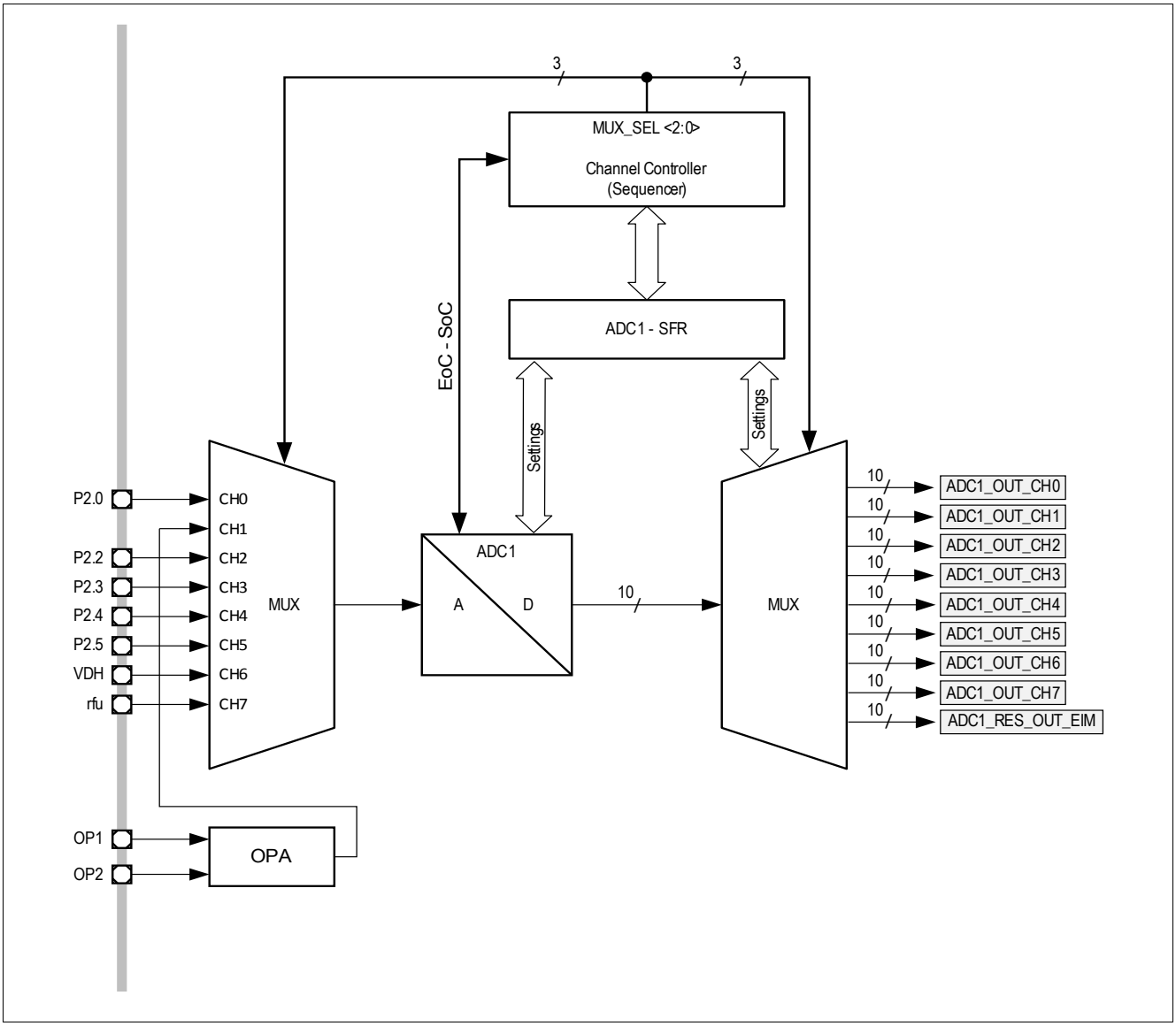

Figure 28 ADC1 Top Level Block Diagram

As shown in the figure above, the ADC1 postprocessing consists of a channel controller (Sequencer) and an 8-channel demultiplexer. The channel control block controls the multiplexer sequencing on the analog side before the ADC1 and on the digital domain after the ADC1. As described in the following section, the channel sequence can be controlled in a flexible way, which allows a certain degree of channel prioritization.

This capability can be used e.g. to give a higher priority to some channels compared to the other channel measurements.

25 High-Voltage Monitor Input

25.1 Features

- High-voltage input with V_S/2 threshold voltage
- Integrated selectable pull-up and pull-down current sources
- Wake capability for power saving modes
- Level change sensitivity configurable for transitions from low to high, high to low or both directions

25.2 Introduction

This module is dedicated to monitor external voltage levels above or below a specified threshold or it can be used to detect a wake-up event at the high-voltage MON pin in low-power mode. The input is sensitive to a input level monitoring, this is available when the module is switched to active mode with the SFR bit EN.

To use the Wake function during low power mode of the IC, the monitoring pin is switched to Sleep Mode via the SFR bit EN.

25.2.1 Block Diagram

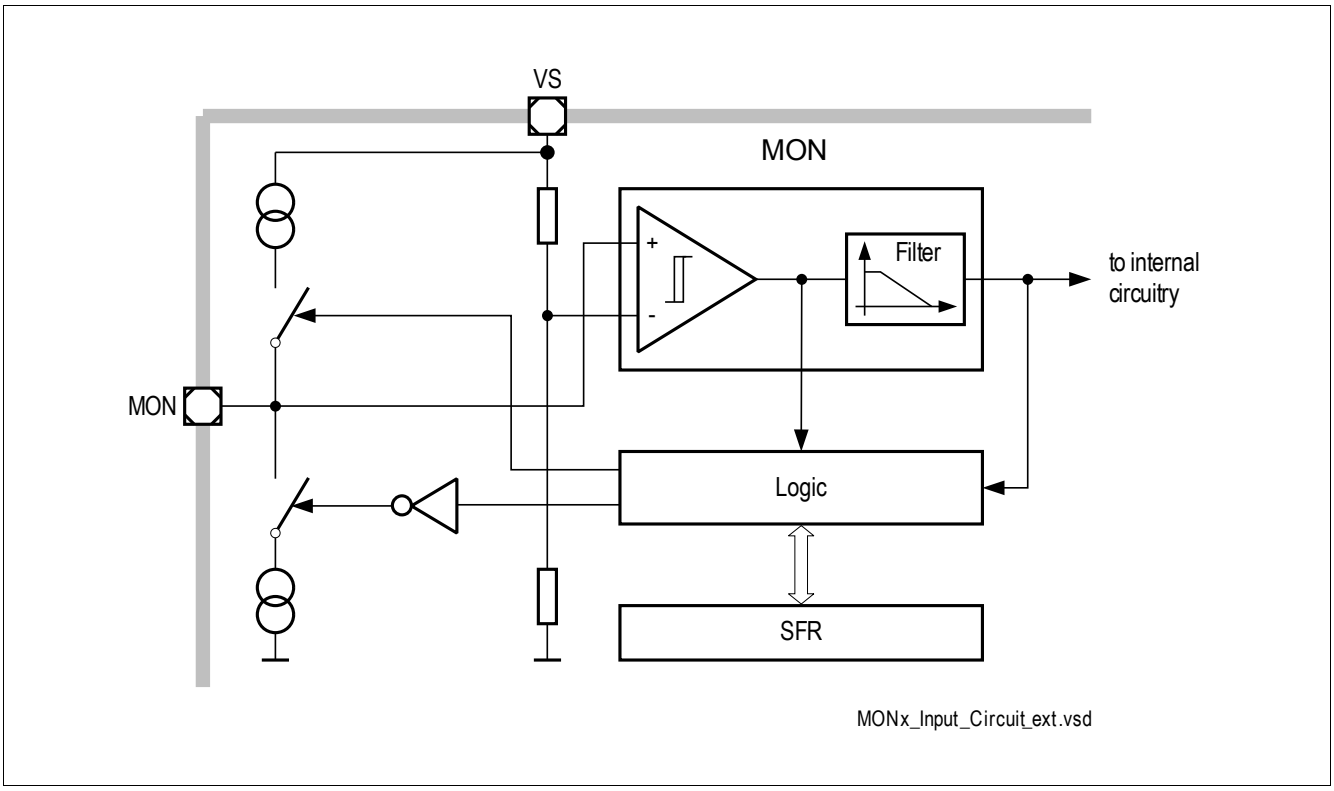

Figure 29 Monitoring Input Block Diagram

1) The typical oscillator frequency is 5 MHz
2) V_{DDC} = 1.5 V, T_j = 25°C
3) Not subject to production test, specified by design.
4) This parameter is valid for PLL operation with an external clock source and thus reflects the real PLL performance.

29.3.2 External Clock Parameters XTAL1, XTAL2

Table 28 Functional Range

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range limits for signal on XTAL1	V_{IX1_SR}	-1.7 + V_{DDC}	–	1.7	V	[2)]	P_3.2.1
Input voltage (amplitude) on XTAL1	V_{AX1_SR}	0.3 x V_{DDC}	–	–	V	[3)] Peak-to-peak voltage	P_3.2.2
XTAL1 input current	I_{IL}	–	–	±20	µA	0 V < V_{IN} < V_{DDI}	P_3.2.3
Oscillator frequency	f_{OSC}	4	–	24	MHz	Clock signal	P_3.2.4
Oscillator frequency	f_{OSC}	4	–	16	MHz	Crystal or Resonator	P_3.2.5
High time	t_1	6	–	–	ns	–	P_3.2.6
Low time	t_2	6	–	–	ns	–	P_3.2.7
Rise time	t_3	–	8	8	ns	–	P_3.2.8
Fall time	t_4	–	8	8	ns	–	P_3.2.9

1) This parameter table is not subject to production test, specified by design.
2) Overload conditions must not occur on pin XTAL1.
3) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF}. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1}.

29.6 LIN Transceiver

29.6.1 Electrical Characteristics

Table 33 Electrical Characteristics LIN Transceiver

V_s = 5.5V to 18V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Bus Receiver Interface							
Receiver threshold voltage, recessive to dominant edge	V_{th_dom}	0.4 × V_S	0.45 × V_S	0.53 x V_S	V	SAE J2602	P_6.1.1
Receiver dominant state	V_{BUSdom}	-27	–	0.4 × V_S	V	LIN Spec 2.2 (Par. 17)	P_6.1.2
Receiver threshold voltage, dominant to recessive edge	V_{th_rec}	0.47 x V_S	0.55 × V_S	0.6 × V_S	V	SAE J2602	P_6.1.3
Receiver recessive state	V_{BUSrec}	0.6 × V_S	–	1.15 × V_S	V	[1] LIN Spec 2.2 (Par. 18)	P_6.1.4
Receiver center voltage	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	[2] LIN Spec 2.2 (Par. 19)	P_6.1.5
Receiver hysteresis	V_{HYS}	0.07 V_S	0.12 × V_S	0.175 × V_S	V	[3] LIN Spec 2.2 (Par. 20)	P_6.1.6
Wake-up threshold voltage	$V_{BUS,wk}$	0.4 × V_S	0.5 × V_S	0.6 × V_S	V	–	P_6.1.7
Dominant time for bus wake-up (internal analog filter delay)	$t_{WK,bus}$	3	–	15	µs	The overall dominant time for bus wake-up is a sum of $t_{WK,bus}$ + adjustable digital filter time. The digital filter time can be adjusted by PMU.CNF_WAKE_FILTER.CNF_LIN_FT;	P_6.1.8
Bus Transmitter Interface							
Bus recessive output voltage	$V_{BUS,ro}$	0.8 × V_S	–	V_S	V	V_{TxD} = high Level	P_6.1.9
Bus dominant output voltage	$V_{BUS,do}$	–	–	0.22 × V_S	V	Driver Dominant Voltage R_L = 500 Ohm	P_6.1.78

Table 35 Supply Voltage Signal Conditioning (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Charge Pump Voltage Measurement V_{CP}							
Input to output voltage attenuation: V_{CP}	ATT_{VCP}	–	0.023	–		–	P_8.1.56
Nominal operating input voltage range V_{CP}	$V_{CP,range}$	2.5	–	52	V	1)	P_8.1.7
Accuracy of V_{CP} sense after calibration	ΔV_{CP}	-747	–	747	mV	V_S = 5.5V to 18V	P_8.1.62
Monitoring Input Voltage Measurement V_{MON}							
Input to output voltage attenuation: V_{MON}	ATT_{VMON}	–	0.039	–		–	P_8.1.49
Nominal operating input voltage range V_{MON}	$V_{MON,range}$	2.5	–	31	V	1)	P_8.1.8
Accuracy of V_{MON} sense after calibration	ΔV_{MON}	-440	–	440	mV	V_S = 5.5V to 18V	P_8.1.68
Pad Supply Voltage Measurement V_{VDDP}							
Input-to-output voltage attenuation: V_{DDP}	ATT_{VDDP}	–	0.164	–		–	P_8.1.33
Nominal operating input voltage range V_{DDP}	$V_{DDP,range}$	0	–	7.50	V	1)	P_8.1.50
Accuracy of V_{DDP} sense after calibration	ΔV_{DDP_SENSE}	-105	–	105	mV	2) V_S = 5.5 to 18V	P_8.1.5
10-Bit ADC Reference Voltage Measurement V_{AREF}							
Input to output voltage attenuation: V_{AREF}	ATT_{VAREF}	–	0.219	–		–	P_8.1.22
Nominal operating input voltage range V_{AREF}	$V_{AREF,range}$	0	–	5.62	V	1)	P_8.1.51
Accuracy of V_{AREF} sense after calibration	ΔV_{AREF}	-79	–	79	mV	V_S = 5.5V to 18V	P_8.1.48
8-Bit ADC Reference Voltage Measurement V_{BG}							
Input-to-output voltage attenuation: V_{BG}	ATT_{VBG}	–	0.75	–		–	P_8.1.57
Nominal operating input voltage range V_{BG}	$V_{BG,range}$	0.8	–	1.64	V	1)	P_8.1.52

Table 35 Supply Voltage Signal Conditioning (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Value of ADC2-V_{BG} measurement after calibration	V_{BG_PMU}	1.01	1.07	1.18	V		P_8.1.73
Core supply Voltage Measurement V_{DDC}							
Input-to-output voltage attenuation: V_{DDC}	ATT_{VDDC}	–	0.75	–		–	P_8.1.34
Nominal operating input voltage range V_{DDC}	$V_{DDC,range}$	0.8	–	1.64	V	1)	P_8.1.53
Accuracy of V_{DDC} sense after calibration	ΔV_{DDC_SENSE}	-22	–	22	mV	V_S = 5.5 to 18V	P_8.1.6
VDH Input Voltage Measurement $V_{VDH10BITADC}$							
VDH Input to output voltage attenuation:	ATT_{VDH_1}	–	0.166	–		SFR setting 1	P_8.1.64
VDH Input to output voltage attenuation:	ATT_{VDH_2}	–	0.224	–		SFR setting 2	P_8.1.65
VDH Input to output voltage attenuation:	ATT_{VDH_3}	-	0.226	-		1)SFR setting 2 Tj = -40..85°C	P_8.1.75
Nominal operating input voltage range V_{VDH}, Range 1	$V_{VDH,range1}$	–	–	30		SFR setting 1	P_8.1.66
Nominal operating input voltage range V_{VDH}, Range 2	$V_{VDH,range2}$	–	–	20		SFR setting 2	P_8.1.67
V_{VDH} 10-bit ADC, Range 1	$\Delta V_{VDHADC10B}$	-300	–	300	mV	V_{DH}= 5.5 to 17.5V, T_j = -40..150°C	P_8.1.39
V_{VDH} 10-bit ADC, Range 3	$\Delta V_{VDHADC10B}$	-200	–	200	mV	1)VDH= 5.5V to 17.5V, Tj = -40..85°C ATT_{VDH_3}	P_8.1.71
V_{VDH} 10-bit ADC, Range 2	$\Delta V_{VDHADC10B\_extend\_T}$	-400	–	400	mV	V_{DH}= 5.5V to 17.5V, T_j = -40..150°C	P_8.1.74
10-Bit ADC measurement input resistance for VDH	$R_{in\_VDH,measure}$	200	390	470	kΩ	PD_N=1 (on-state)	P_8.1.3
Measurement input leakage current for V_{VDH}	$I_{leak\_VDH,\ measure}$	-0.05	–	2.0	µA	PD_N=0 (off-state),	P_8.1.10

1) Not subject to production test, specified by design.

2) Accuracy is valid for a calibrated device.

Table 42 Electrical Characteristics MOSFET Driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
High level output voltage GLx vs. GND	V_{Gxx6}	8	–	–	V	V_{SD} = 6.4 V[1], C_{Load} = 10 nF, I_{CP}=2.5 mA[2]	P_12.1.6
High level output voltage GLx vs. GND	V_{Gxx7}	7	–	–	V	V_{SD} = 5.4 V, C_{Load} = 10 nF, I_{CP}=2.5 mA[2]	P_12.1.7
Rise time	t_{rise3_3nf}	–	200	–	ns	[1]CLoad = 3.3 nF, V_{SD} ≥ 8 V, 25-75% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.8
Fall time	t_{fall3_3nf}	–	200	–	ns	[1]C_{Load} = 3.3 nF, V_{SD} ≥ 8 V, 75-25% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.9
Rise time	$t_{risemax}$	100	250	450	ns	C_{Load} = 10 nF, V_{SD} ≥ 8 V, 25-75% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.57
Fall time	$t_{fallmax}$	100	250	450	ns	C_{Load} = 10 nF, V_{SD} ≥ 8 V, 75-25% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.58
Rise time	$t_{risemin}$	1.25	2.5	5	µs	[1]C_{Load} = 10 nF, V_{SD} ≥ 8 V, 25-75% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 3(min)	P_12.1.14
Fall time	$t_{fallmin}$	1.25	2.5	5	µs	[1]C_{Load} = 10 nF, V_{SD} ≥ 8 V, 75-25% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 3(min)	P_12.1.15
Absolute rise - fall time difference for all LSx	$t_{r\_f(diff)LSx}$	–	–	100	ns	C_{Load} = 10 nF, V_{SD} ≥ 8 V, 25-75% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.35
Absolute rise - fall time difference for all HSx	$t_{r\_f(diff)HSx}$	–	–	100	ns	C_{Load} = 10 nF, V_{SD} ≥ 8 V, 25-75% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.36
Resistor between GHx/GLx and GND	R_{GGND}	30	40	50	kΩ	[1]–	P_12.1.11