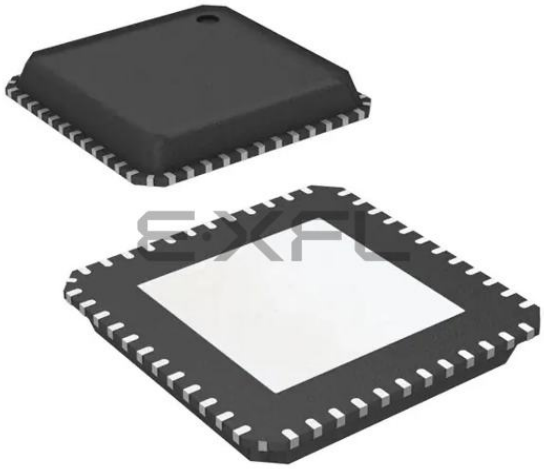

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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive
Core Processor	ARM® Cortex®-M3
Program Memory Type	FLASH (128kB)
Controller Series	-
RAM Size	6K x 8
Interface	LIN, SSI, UART
Number of I/O	10
Voltage - Supply	5.5V ~ 28V
Operating Temperature	-40°C ~ 150°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9879qxa40xuma2

Table of Contents

- Overtemperature protection
- Short circuit protection
- Loss of clock detection with fail safe mode entry for low system power consumption
- Temperature Range T_j = -40 °C to +150 °C
- Package VQFN-48 with LTI feature
- Green package (RoHS compliant)
- AEC qualified

2 Block Diagram

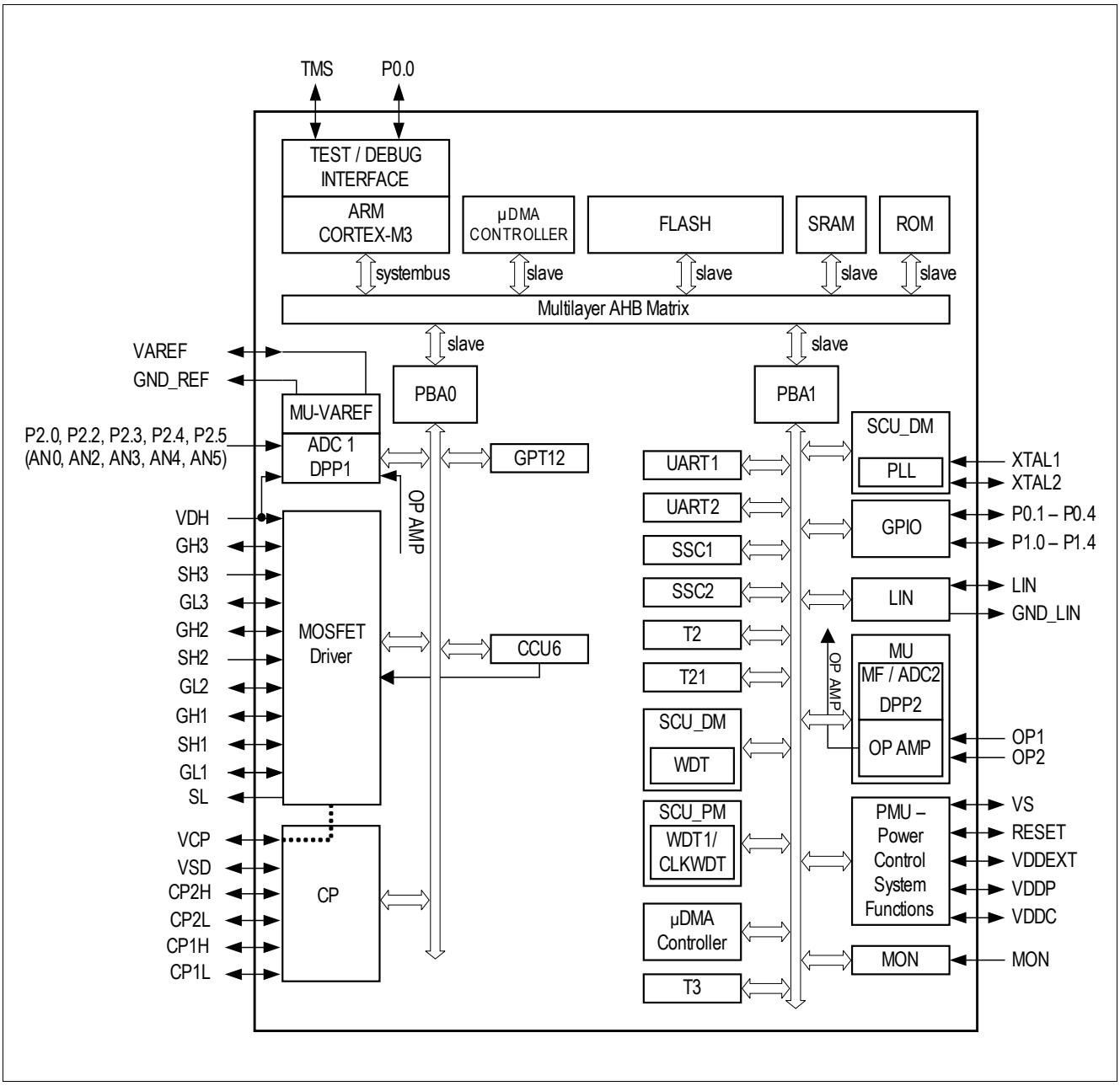

Figure 1 Block Diagram TLE9879QXA40

1) May not be switched off due to safety reasons
2) MC PLL clock disabled, MC supply reduced to 1.1 V

Wake-Up Levels and Transitions

The wake-up can be triggered by rising, falling or both signal edges for the monitor input, by LIN or by cyclic wake-up.

7 System Control Unit - Power Modules (SCU-PM)

7.1 Features

- Clock Watchdog Unit (CWU): supervision of all clocks with NMI signaling relevant to power modules
- Interrupt Control Unit (ICU): all interrupt flags and status flags with system relevance
- Power Control Unit (PCU): takes over control when device enters and exits Sleep and Stop Mode
- External Watchdog (WDT1): independent system watchdog for monitoring system activity

7.2 Introduction

7.2.1 Block Diagram

The System Control Unit of the power modules consists of the sub-modules in the figure shown below:

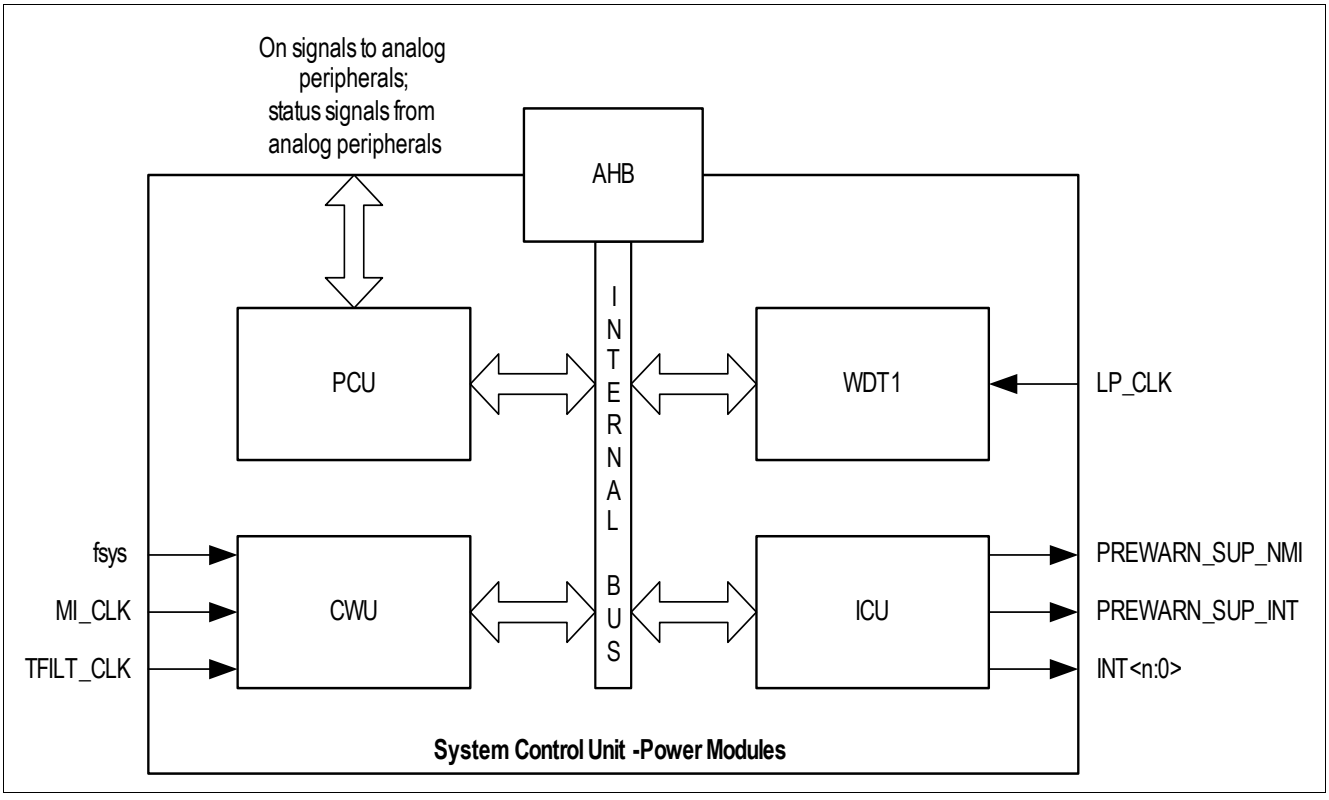

Figure 11 Block diagram of System Control Unit - Power Modules

AHB (Advanced High-Performance Bus)

CWU (Clock Watchdog Unit)

- f_{sys} system frequency: PLL output
- MI_CLK measurement interface clock (analog clock): derived from fsys using division factors 1/2/3/4
- TFILT_CLK clock used for digital filters: derived from fsys using configurable division factors

14.2.2 Port 2

Figure 18 shows the structure of an input-only port pin. Each P2 pin can only function in input mode. Register P2_DIR is provided to enable or disable the input driver. When the input driver is enabled, the actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt trigger device and can be read via register P2_DATA. Each pin can also be programmed to activate an internal weak pull-up or pull-down device. Register P2_PUDSEL selects whether a pull-up or the pull-down device is activated while register P2_PUDEN enables or disables the pull device. The analog input (AnalogIn) bypasses the digital circuitry and Schmitt trigger device for direct feed-through to the ADC input channels.

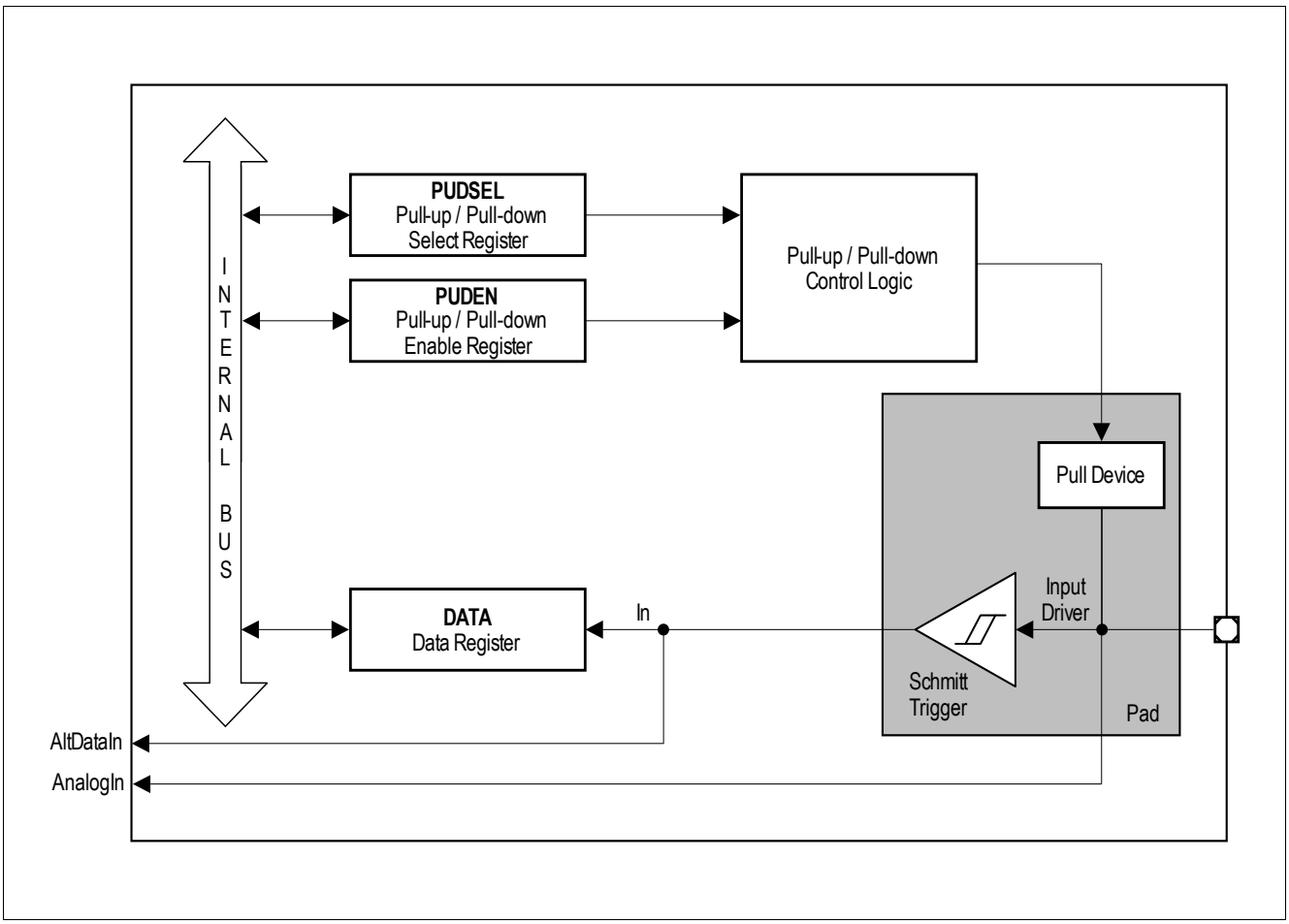

Figure 18 General Structure of Input Port (P2)

Note: The capture/compare module itself is referred to as CCU6 (capture/compare unit 6). A capture/compare channel inside this module is referred to as CC6x.

The timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined (e.g. a channel works in compare mode, whereas another channel works in capture mode). The timer T13 can work in compare mode only. The multi-channel control unit generates output patterns which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

18.2.1 Block Diagram

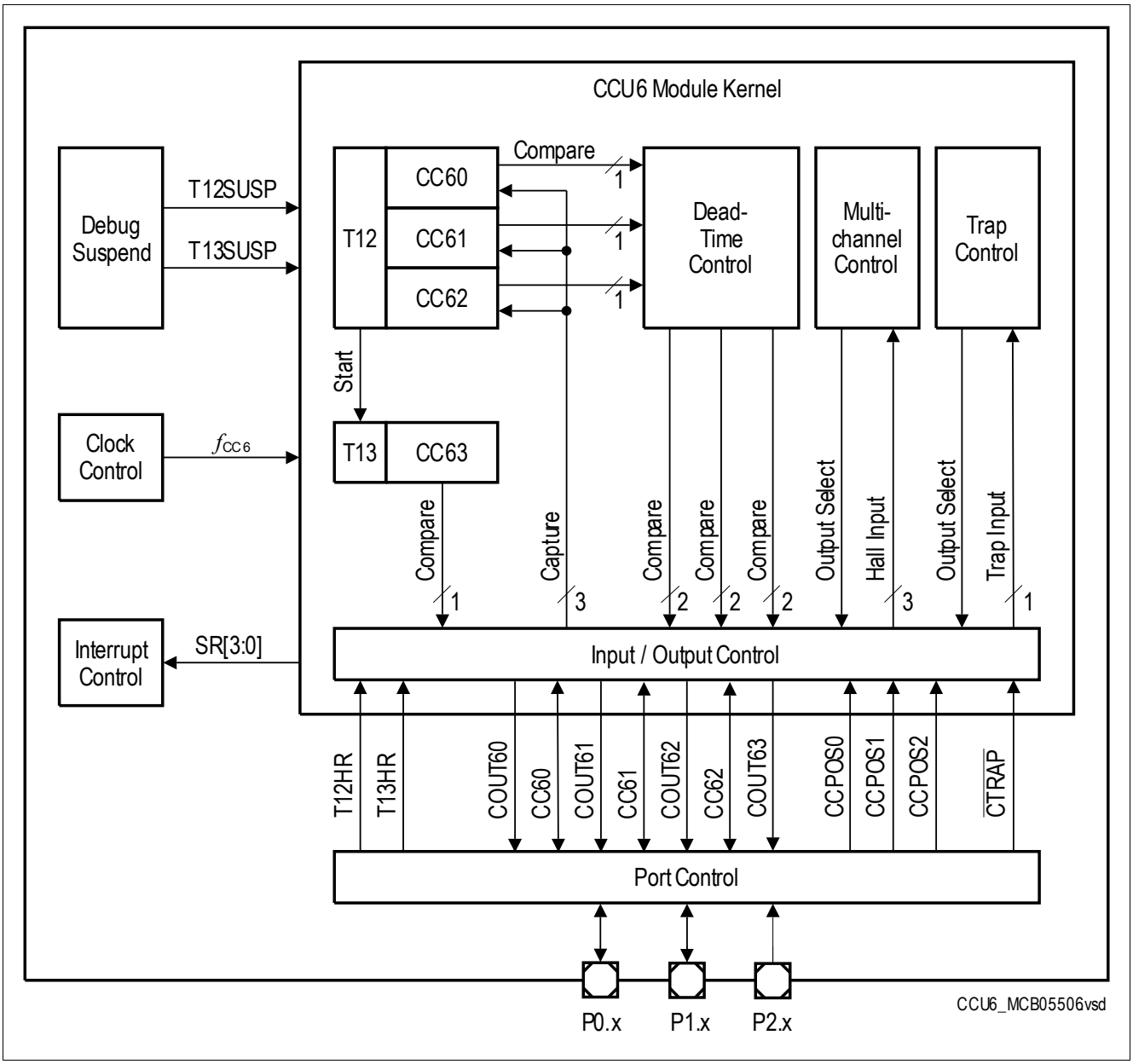

Figure 21 CCU6 Block Diagram

19 UART1/UART2

19.1 Features

- Full-duplex asynchronous modes
  - 8-bit or 9-bit data frames, LSB first
  - fixed or variable baud rate
- Receive buffered
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception
- Baud-rate generator with fractional divider for generating a wide range of baud rates
- Hardware logic for break and synch byte detection

19.2 Introduction

The UART provides a full-duplex asynchronous receiver/transmitter, i.e., it can transmit and receive simultaneously. It is also receive-buffered, i.e., it can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost. The serial port receive and transmit registers are both accessed at Special Function Register (SFR) SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

19.2.1 Block Diagram

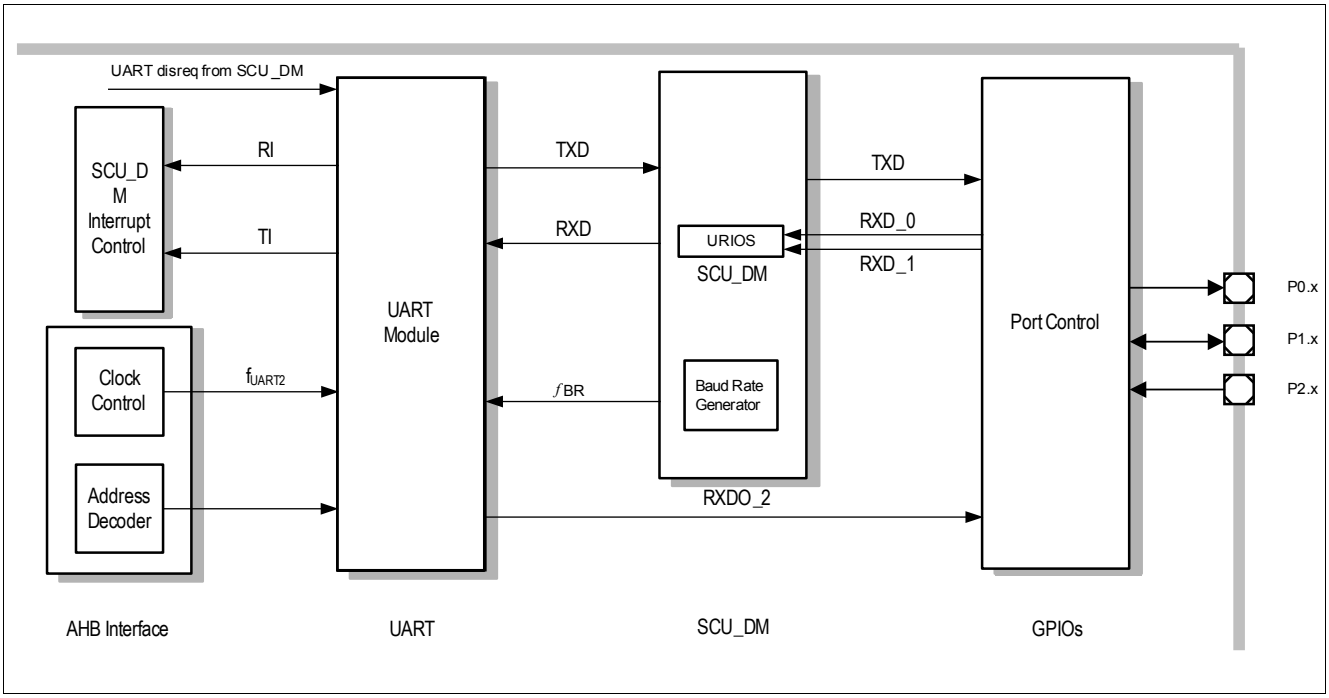

Figure 22 UART Block Diagram

20 LIN Transceiver

20.1 Features

General Functional Features

- Compliant to LIN2.2 standard, backward compatible to LIN1.3, LIN2.0 and LIN 2.1
- Compliant to SAE J2602 (slew rate, receiver hysteresis)

Special Features

- Measurement of LIN master baudrate via Timer 2
- LIN can be used as input/output with SFR bits.
- TxD timeout feature (optional, on by default)

Operation Mode Features

- LIN Sleep Mode (LSLM)
- LIN Receive-Only Mode (LROM)
- LIN Normal Mode (LNM)
- High Voltage Input / Output Mode (LHVIO)

Supported Baud Rates

- Mode for a transmission up to 10.4 kBaud
- Mode for a transmission up to 20 kBaud
- Mode for a transmission up to 40 kBaud
- Mode for a transmission up to 115.2 kBaud

Slope Mode Features

- Normal Slope Mode (20 kbit/s)
- Low Slope Mode (10.4 kbit/s)
- Flash Mode (115.2 kbit/s)

Wake-Up Features

- LIN bus wake-up

24 10-Bit Analog Digital Converter (ADC1)

24.1 Features

The principal features of the ADC1 are:

- Up to 8 analog input channels (channel 7 reserved for future use)
- Flexible results handling
  - 8-bit and 10-bit resolution
- Flexible source selection due to sequencer
  - insert one exceptional sequence (ESM)
  - insert one interrupt measurement into the current sequence (EIM), single or up to 128 times
  - software mode
- Conversion sample time (separate for each channel) adjustable to adapt to sensors and reference
- Standard external reference (VAREF) to support ratiometric measurements and different signal scales
- DMA support, transfer ADC conversion results via DMA into RAM
- Support of suspend and power saving modes
- Result data protection for slow CPU access (wait-for-read mode)
- Programmable clock divider
- Integrated sample and hold circuitry

24.2 Introduction

The TLE9879QXA40 includes a high-performance 10-bit Analog-to-Digital Converter (ADC1) with eight multiplexed analog input channels. The ADC1 uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC1 are available at AN0, AN2 - AN5.

25 High-Voltage Monitor Input

25.1 Features

- High-voltage input with V_S/2 threshold voltage
- Integrated selectable pull-up and pull-down current sources
- Wake capability for power saving modes
- Level change sensitivity configurable for transitions from low to high, high to low or both directions

25.2 Introduction

This module is dedicated to monitor external voltage levels above or below a specified threshold or it can be used to detect a wake-up event at the high-voltage MON pin in low-power mode. The input is sensitive to a input level monitoring, this is available when the module is switched to active mode with the SFR bit EN.

To use the Wake function during low power mode of the IC, the monitoring pin is switched to Sleep Mode via the SFR bit EN.

25.2.1 Block Diagram

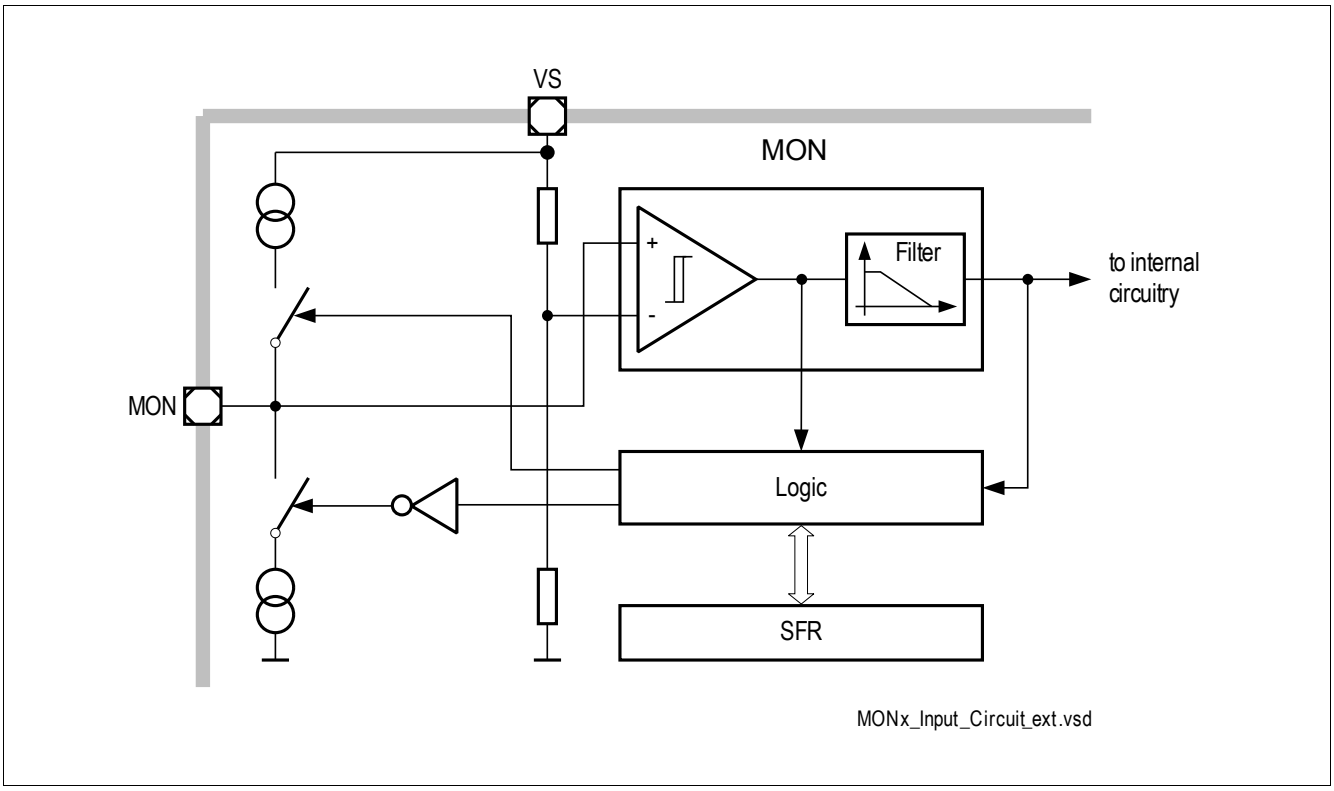

Figure 29 Monitoring Input Block Diagram

28 Application Information

28.1 BLDC Driver

Figure 32 shows the TLE9879QXA40 in an electric drive application setup controlling a BLDC motor.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

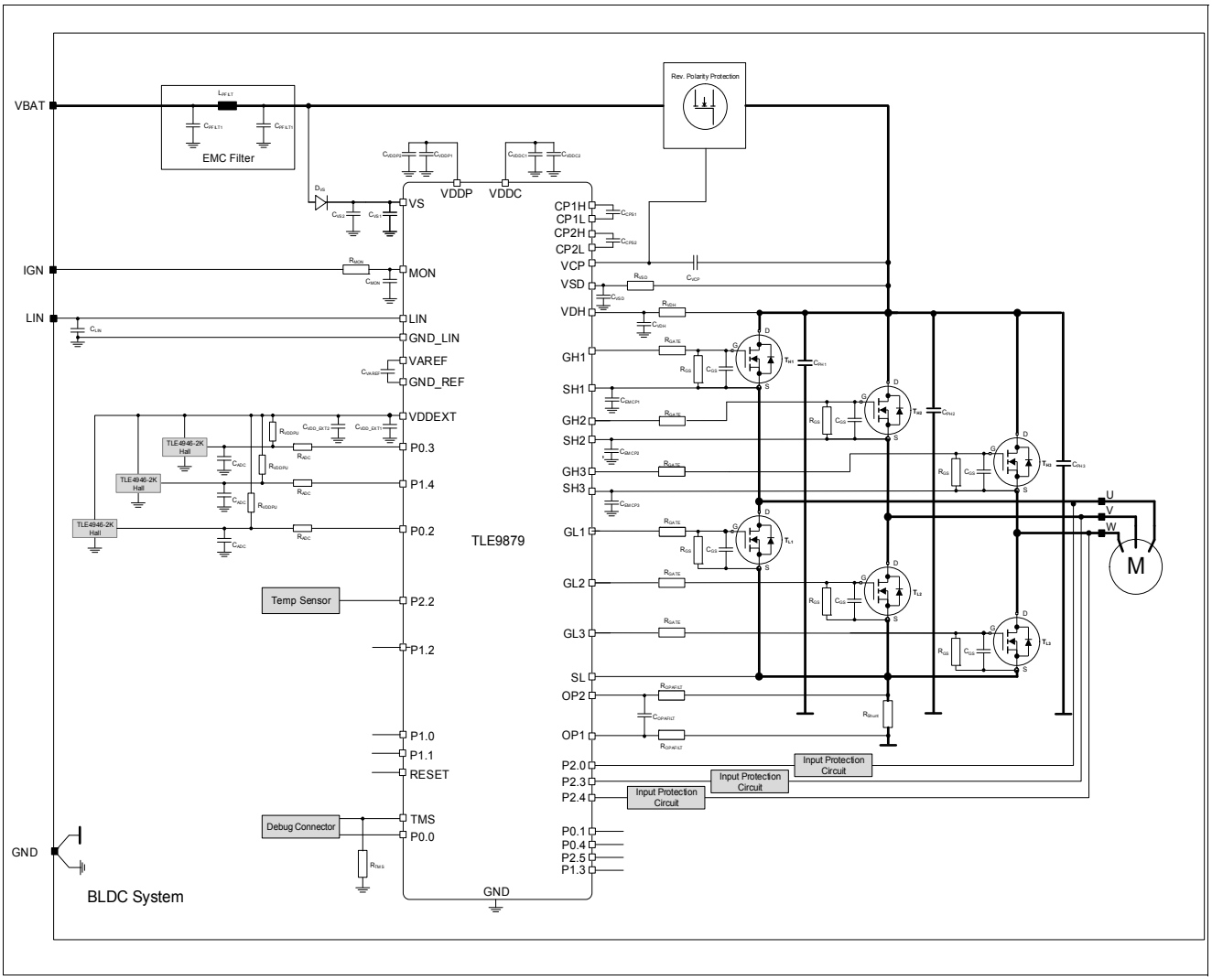

Figure 32 Simplified Application Diagram Example

Note: This is a very simplified example of an application circuit and bill of materials. The function must be verified in the actual application.

28.2 ESD Immunity According to IEC61000-4-2

Note: Tests for ESD immunity according to IEC61000-4-2 “Gun test” (150pF, 330Ω) has been performed. The results and test condition will be available in a test report.

Table 16 ESD “Gun Test”

Performed Test	Result	Unit	Remarks
ESD at pin LIN, versus GND[1)]	> 6	kV	[2)]positive pulse
ESD at pin LIN, versus GND[1)]	< -6	kV	[2)]negative pulse

1) ESD test “ESD GUN” is specified with external components; see application diagram: C_{MON} = 100 nF, R_{MON} = 1 kΩ, C_{LIN} = 220 pF, C_{VS} = >20 µF ELCO + 100 nF ESR < 1 Ω, C_{VSD} = 1 µF, R_{VSD} = 2 Ω.

2) ESD susceptibility “ESD GUN” according to LIN EMC Test Specification, Section 4.3 (IEC 61000-4-2). To be tested by external test house (IBEE Zwickau)

29.1.2 Functional Range

Table 18 Functional Range

T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage in Active Mode	V_{S_AM}	5.5	–	28	V	–	P_1.2.1
Extended supply voltage in Active Mode	$V_{S\_AM\_extend}$	28	–	40	V	1) Functional with parameter deviation	P_1.2.16
Supply voltage in Active Mode for MOSFET Driver Supply	V_{SD_AM}	5.4	–	28	V		P_1.2.18
Extended supply voltage in Active Mode for MOSFET Driver Supply	$V_{SD\_AM\_extend}$	28	–	32	V	1)3)Functional with parameter deviation	P_1.2.17
Specified supply voltage for LIN Transceiver	$V_{S\_AM\_LIN}$	5.5	–	18	V	Parameter Specification	P_1.2.2
Extended supply voltage for LIN Transceiver	$V_{S\_AM\_LIN}$	4.8	–	28	V	Functional with parameter deviation	P_1.2.14
Supply voltage in Active Mode with reduced functionality (Microcontroller / Flash with full operation)	V_{S_AMmin}	3.0	–	5.5	V	2)	P_1.2.3
Supply voltage in Sleep Mode	V_{S_Sleep}	3.0	–	28	V	–	P_1.2.4
Supply voltage transients slew rate	dV_S/dt	-1	–	1	V/µs	3)	P_1.2.5
Output sum current for all GPIO pins	$I_{GPIO,sum}$	-50	–	50	mA	3)	P_1.2.7
Operating frequency	f_{sys}	5	–	40	MHz	4)	P_1.2.15
Junction temperature	T_j	-40	–	150	°C	–	P_1.2.9

1) This operation voltage range is only allowed for a short duration: t_{max} ≤ 400 ms (continuous operation at this voltage is not allowed), f_{sys} = 24 MHz, I_{VDDP} = 10 mA, I_{VDDEXT} = 5 mA. In addition, the power dissipation caused by the Charge Pump + MOSFET driver have to be considered.

2) Reduced functionality (e.g. cranking pulse) - Parameter deviation possible.

3) Not subject to production test, specified by design.

4) Function not specified when limits are exceeded.

Table 19 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current consumption in Sleep Mode with cyclic wake	I_{Cyclic}	–	–	110	µA	T_J = -40°C to 85°C; V_S = 5.5 V to 18V; t_{Cyclic_ON} = 4ms; t_{Cyclic_OFF} = 2048 ms;[2]	P_1.3.4
Current consumption in Stop Mode	I_{Stop}	–	110	160	µA	System in Stop Mode, microcontroller not clocked, Wake capable via LIN and MON; MON connected to VS or GND; GPIOs open (no loads) or connected to GND; T_J = -40°C to 85°C; V_S = 5.5 V to 18V	P_1.3.10
Current consumption in Stop Mode-Extended temperature range 1	I_{Stop_extend}	–	600	1800	µA	System in Stop Mode, microcontroller not clocked, Wake capable via LIN and MON; MON connected to VS or GND; GPIOs open (no loads) or connected to GND; T_J = -40 °C to 150 °C; V_S = 5.5 V to 18 V	P_1.3.20

1) Current on V_S, ADC1/2 active, timer running, LIN active (recessive).

2) Incl. leakage currents form VDH, VSD and MON

Note: Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

Table 31 DC Characteristics Port0, Port1 (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage	V_{IL}	-0.3	–	0.3 x V_{DDP}	V	2)4.5V ≤ V_{DDP} ≤ 5.5V	P_5.1.3
Input low voltage	V_{IL_extend}	-0.3	0.42 x V_{DDP}	–	V	1)2.6V ≤ V_{DDP} ≤ 4.5V	P_5.1.17
Input high voltage	V_{IH}	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	2)4.5V ≤ V_{DDP} ≤ 5.5V	P_5.1.4
Input high voltage	V_{IH_extend}	–	0.52 x V_{DDP}	V_{DDP} + 0.3	V	1)2.6V ≤ V_{DDP} ≤ 4.5V	P_5.1.18
Output low voltage	V_{OL}	–	–	1.0	V	3) 4) $I_{OL} \leq I_{OLmax}$	P_5.1.6
Output low voltage	V_{OL}	–	–	0.4	V	3) 5) $I_{OL} \leq I_{OLnom}$	P_5.1.7
Output high voltage	V_{OH}	V_{DDP} - 1.0	–	–	V	3) 4) $I_{OH} \geq I_{OHmax}$	P_5.1.8
Output high voltage	V_{OH}	V_{DDP} - 0.4	–	–	V	3) 5) $I_{OH} \geq I_{OHnom}$	P_5.1.9
Input leakage current	$I_{OZ\_extend1}$	-500	–	+500	nA	-40°C ≤ T_J ≤ 25°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.20
Input leakage current	I_{OZ1}	-5	–	+5	µA	6) 25°C < T_J ≤ 85°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.10
Input leakage current	$I_{OZ\_extend2}$	-15	–	+15	µA	85°C < T_J ≤ 150°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.11
Pull level keep current	I_{PLK}	-200	–	+200	µA	7) $V_{PIN} \geq V_{IH}$ (up) $V_{PIN} \leq V_{IL}$ (dn)	P_5.1.12
Pull level force current	I_{PLF}	-1.5	–	+1.5	mA	7) $V_{PIN} \leq V_{IL}$ (up) $V_{PIN} \geq V_{IH}$ (dn)	P_5.1.13
Pin capacitance	C_{IO}	–	–	10	pF	1)	P_5.1.14
Reset Pin Timing							
Reset Pin Input Filter Time	t_{filt_RESET}	–	5	–	µs	1)	P_5.1.19

1) Not subject to production test, specified by design.

2) Tested at V_{DDP} = 5V, specified for 4.5V < V_{DDP} < 5.5V.

3) The maximum deliverable output current of a port driver depends on the selected output driver mode. The limit for pin groups must be respected.

4) Tested at 4.9V < V_{DDP} < 5.1V, I_{OL} = 4mA, I_{OH} = -4mA, specified for 4.5V < V_{DDP} < 5.5V.

5) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow GND$, $V_{OH} \rightarrow V_{DDP}$). Tested at 4.9V < V_{DDP} < 5.1V, I_{OL} = 1mA, I_{OH} = -1mA.

Table 32 DC Characteristics Port 2 (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Pull level force current	I_{PLF}	-750	–	+750	µA	3) $V_{PIN} \le V_{IL}$ (up) $V_{PIN} \ge V_{IH}$ (dn)	P_5.2.6
Pin capacitance (digital inputs/outputs)	C_{IO}	–	–	10	pF	2)	P_5.2.7

1) Tested at V_{DDP} = 5V, specified for 4.5V < V_{DDP} < 5.5V.

2) Not subject to production test, specified by design.

3) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \ge V_{IH}$ for a pull-up; $V_{PIN} \le V_{IL}$ for a pull-down.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \le V_{IL}$ for a pull-up; $V_{PIN} \ge V_{IH}$ for a pull-down.

29.6 LIN Transceiver

29.6.1 Electrical Characteristics

Table 33 Electrical Characteristics LIN Transceiver

V_s = 5.5V to 18V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Bus Receiver Interface							
Receiver threshold voltage, recessive to dominant edge	V_{th_dom}	0.4 × V_S	0.45 × V_S	0.53 x V_S	V	SAE J2602	P_6.1.1
Receiver dominant state	V_{BUSdom}	-27	–	0.4 × V_S	V	LIN Spec 2.2 (Par. 17)	P_6.1.2
Receiver threshold voltage, dominant to recessive edge	V_{th_rec}	0.47 x V_S	0.55 × V_S	0.6 × V_S	V	SAE J2602	P_6.1.3
Receiver recessive state	V_{BUSrec}	0.6 × V_S	–	1.15 × V_S	V	[1] LIN Spec 2.2 (Par. 18)	P_6.1.4
Receiver center voltage	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	[2] LIN Spec 2.2 (Par. 19)	P_6.1.5
Receiver hysteresis	V_{HYS}	0.07 V_S	0.12 × V_S	0.175 × V_S	V	[3] LIN Spec 2.2 (Par. 20)	P_6.1.6
Wake-up threshold voltage	$V_{BUS,wk}$	0.4 × V_S	0.5 × V_S	0.6 × V_S	V	–	P_6.1.7
Dominant time for bus wake-up (internal analog filter delay)	$t_{WK,bus}$	3	–	15	µs	The overall dominant time for bus wake-up is a sum of $t_{WK,bus}$ + adjustable digital filter time. The digital filter time can be adjusted by PMU.CNF_WAKE_FILTER.CNF_LIN_FT;	P_6.1.8
Bus Transmitter Interface							
Bus recessive output voltage	$V_{BUS,ro}$	0.8 × V_S	–	V_S	V	V_{TxD} = high Level	P_6.1.9
Bus dominant output voltage	$V_{BUS,do}$	–	–	0.22 × V_S	V	Driver Dominant Voltage R_L = 500 Ohm	P_6.1.78

29.8.2 Central Temperature Sensor Parameters

Table 36 Electrical Characteristics Temperature Sensor Module

V_S = 3.0 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output voltage V_{TEMP} at T_0=273 K (0°C)	a	–	0.666	–	V	1) T_0=273 K (0°C)	P_8.2.2
Temperature sensitivity b	b	–	2.31	–	mV/K	1)	P_8.2.4
Accuracy_1	Acc_1	-10	–	10	°C	2)1) -40°C < Tj < 85°C	P_8.2.5
Accuracy_2	Acc_2	-10	–	10	°C	2)1) 125°C < Tj < 150°C	P_8.2.6
Accuracy_3	Acc_3	-5	–	5	°C	2)1) 85°C < Tj < 125°C	P_8.2.7

1) Not subject to production test, specified by design

2) Accuracy with reference to on-chip temperature calibration measurement, valid for Mode1

Table 42 Electrical Characteristics MOSFET Driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
High level output voltage GLx vs. GND	V_{Gxx6}	8	–	–	V	V_{SD} = 6.4 V[1], C_{Load} = 10 nF, I_{CP}=2.5 mA[2]	P_12.1.6
High level output voltage GLx vs. GND	V_{Gxx7}	7	–	–	V	V_{SD} = 5.4 V, C_{Load} = 10 nF, I_{CP}=2.5 mA[2]	P_12.1.7
Rise time	t_{rise3_3nf}	–	200	–	ns	[1]CLoad = 3.3 nF, V_{SD} ≥ 8 V, 25-75% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.8
Fall time	t_{fall3_3nf}	–	200	–	ns	[1]C_{Load} = 3.3 nF, V_{SD} ≥ 8 V, 75-25% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.9
Rise time	$t_{risemax}$	100	250	450	ns	C_{Load} = 10 nF, V_{SD} ≥ 8 V, 25-75% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.57
Fall time	$t_{fallmax}$	100	250	450	ns	C_{Load} = 10 nF, V_{SD} ≥ 8 V, 75-25% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.58
Rise time	$t_{risemin}$	1.25	2.5	5	µs	[1]C_{Load} = 10 nF, V_{SD} ≥ 8 V, 25-75% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 3(min)	P_12.1.14
Fall time	$t_{fallmin}$	1.25	2.5	5	µs	[1]C_{Load} = 10 nF, V_{SD} ≥ 8 V, 75-25% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 3(min)	P_12.1.15
Absolute rise - fall time difference for all LSx	$t_{r\_f(diff)LSx}$	–	–	100	ns	C_{Load} = 10 nF, V_{SD} ≥ 8 V, 25-75% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.35
Absolute rise - fall time difference for all HSx	$t_{r\_f(diff)HSx}$	–	–	100	ns	C_{Load} = 10 nF, V_{SD} ≥ 8 V, 25-75% of V_{Gxx1}, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.36
Resistor between GHx/GLx and GND	R_{GGND}	30	40	50	kΩ	[1]–	P_12.1.11