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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 11x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl17z128vfm4r

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.4 Voltage and current operating ratings

Table 4. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V _{DD}	Digital supply voltage	-0.3	3.8	V
I _{DD}	Digital supply current	—	120	mA
V _{IO}	IO pin input voltage	-0.3	V _{DD} + 0.3	V
۱ _D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V _{DDA}	Analog supply voltage	V _{DD} – 0.3	V _{DD} + 0.3	V

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is V_{IL} + (V_{IH} - V_{IL}) / 2

Figure 1. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- $C_L=30 \text{ pF loads}$
- Slew rate disabled
- Normal drive strength

2.2 Nonswitching electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
	 VLPS → RUN 					
		_	7.5	8	μs	
	• STOP \rightarrow RUN					
		—	7.5	8	μs	

 Table 8. Power mode transition operating behaviors (continued)

1. Normal boot (FTFA_FOPT[LPBOOT]=11)

2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

NOTE

The while (1) test is executed with flash cache enabled.

NOTE

The data at 105 °C are for QFN, LQFP and MAPBGA packages only.

 Table 9. Power consumption operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—		See note	mA	1
I _{DD_RUNCO}	Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V					2
	• at 25 °C	—	5.76	6.40	mA	
	• at 105 °C	—	6.04	6.68		
I _{DD_RUNCO}	Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V _{DD} = 3.0 V					
	• at 25 °C	—	3.21	3.85	mA	
	• at 105 °C	_	3.49	4.13		
I _{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, $V_{DD} = 3.0 V$					2
	• at 25 °C	—	6.45	7.09	mA	
	• at 105 °C	—	6.75	7.39		
I _{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, $V_{DD} = 3.0 V$					2

Table continues on the next page...

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Table 9.	Power consumption operating behaviors ((continued)
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Symbol	Description	Min.	Тур.	Max.	Unit	Notes
	disable, 125 kHz core / 31.25 kHz flash, V _{DD} =		50	131	μA	
	• at 25 °C					
I _{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 2 MHz core / 0.5 MHz flash, $V_{DD} = 3.0 \text{ V}$ • at 25 °C		208	289	цА	
	Wait mode current—core disabled, 48 MHz		200	200	P/ 1	
DD_WAI	system/24 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, V _{DD} = 3.0 V	_	1.81	1.89	mA	
I _{DD_WAIT}	Wait mode current—core disabled, 24 MHz system/12 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, V _{DD} = 3.0 V		1.22	1.39	mA	
I _{DD_VLPW}	Very-low-power wait mode current, core disabled, 4 MHz system/ 1 MHz bus and flash, all peripheral clocks disabled, $V_{DD} = 3.0$ V	_	172	182	μA	
I _{DD_VLPW}	Very-low-power wait mode current, core disabled, 2 MHz system/ 0.5 MHz bus and flash, all peripheral clocks disabled, $V_{DD} = 3.0 V$	_	69	76	μΑ	
I _{DD_VLPW}	Very-low-power wait mode current, core disabled, 125 kHz system/ 31.25 kHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V	—	36	40	μΑ	
I _{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, 12 MHz bus and flash, V_{DD} = 3.0 V					
			1.81	2.06	mA	
I _{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, flash doze enabled, 12 MHz bus, $V_{DD} = 3.0 V$					
		_	1.00	1.25	mA	
I _{DD_STOP}	Stop mode current at 3.0 V • at 25 °C and below	_	161.93	171.82		
	• at 85 °C	_	181.45	191.96		
	• at 105 °C	—	236.29	271.17	μA	
			390.33	465.58		
IDD_VLPS	 at 25 °C and below 	_	3 31	5 1/1		
	• at 50 °C	_	10.43	17.68		
	• at 85 °C	_	34.14	61.06	μΑ	
	• at 105 °C	_	104.38	164.44		
I _{DD_VLPS}	Very-low-power stop mode current at 1.8 V • at 25 °C and below	_	3.21	5.22		

Table continues on the next page...

General



1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times chip$ power dissipation.

Table 16. Thermal operating requirements for other packages

Symbol	Description	Min.	Max.	Unit	Notes
TJ	Die junction temperature	-40	125	°C	
T _A	Ambient temperature	-40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.

2.4.2 Thermal attributes

Table 17. Thermal attributes

Board type	Symbo I	Description	48 QFN	32 QFN	64 LQFP	64 MAPB GA	36 WLCS P	Unit	Notes
Single-layer (1S)	R _{θJA}	Thermal resistance, junction to ambient (natural convection)	86	101	70	50.3	77.6	°C/W	1
Four-layer (2s2p)	R _{θJA}	Thermal resistance, junction to ambient (natural convection)	29	33	51	42.9	38.9	°C/W	
Single-layer (1S)	R _{θJMA}	Thermal resistance, junction to ambient (200 ft./min. air speed)	71	84	58	41.4	69.6	°C/W	
Four-layer (2s2p)	R _{θJMA}	Thermal resistance, junction to ambient (200 ft./min. air speed)	24	28	45	38.0	35.6	°C/W	
_	R _{θJB}	Thermal resistance, junction to board	12	13	33	39.6	34.8	°C/W	2
_	R _{θJC}	Thermal resistance, junction to case	1.7	1.7	20	27.3	0.37	°C/W	3
_	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	3	4	0.4	0.2	°C/W	4
_	Ψ_{JB}	Thermal characterization parameter, junction to package bottom (natural convection)	-	-	-	12.6	-	°C/W	5

1. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air), or EIA/JEDEC Standard JESD51-6, Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air).

2. Determined according to JEDEC Standard JESD51-8, Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board.

Peripheral operating requirements and behaviors

- 3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
- 4. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air).
- 5. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation			
	Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width			
	Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10		ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0		ns
J11	SWD_CLK high to SWD_DIO data valid	_	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

Table 18. SWD full voltage range electricals



Figure 4. Serial wire clock input timing



Figure 5. Serial wire data timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG-Lite specifications

Table 19.	IRC48M	specification
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Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DD}	Supply current	—	400	500	μA	—
f _{IRC}	Output frequency		48	—	MHz	
Δf _{irc48m_ol_lv}	Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over temperature		± 0.5	± 1.5	%f _{irc48m}	1
$\Delta f_{irc48m_ol_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over temperature	_	± 0.5	± 1.0	%f _{irc48m}	1

Table continues on the next page...

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
	• 24 MHz	—	1.5	—	mA	
	• 32 MHz					
IDDOSC	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	_	25	_	μA	
	• 4 MHz	_	400	_	μA	
	• 8 MHz (RANGE=01)	_	500	_	μA	
	• 16 MHz	_	2.5	_	mA	
	• 24 MHz	_	3	_	mA	
	• 32 MHz	_	4	_	mA	
C _x	EXTAL load capacitance	_	_	_		2, 3
Cy	XTAL load capacitance	_	—	—		2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	_	MΩ	
	Feedback resistor — high-frequency, low- power mode (HGO=0)	_			MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	_	1		MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)				kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	_	200		kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	_			kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
		_	0	_	kΩ	
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	_	0.6	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	_	V _{DD}	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	_	0.6	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	_	V _{DD}	_	V	

Table 21. Oscillator DC electrical specifications (continued)

V_{DD}=3.3 V, Temperature =25 °C
 See crystal or resonator manufacturer's recommendation

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Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
		 <12-bit modes 	—	±0.5	–0.7 to +0.5		
E _{FS}	Full-scale error	12-bit modes	—	-4	-5.4	LSB ⁴	$V_{ADIN} = V_{DDA}^5$
		 <12-bit modes 	_	-1.4	-1.8		
EQ	Quantization error	16-bit modes	—	-1 to 0	—	LSB ⁴	
		• ≤13-bit modes	_	_	±0.5		
ENOB	Effective number of	16-bit differential mode					6
	bits	• Avg = 32	12.8	14.5		bits	
		• Avg = 4	11.9	13.8	_	bits	
		16-bit single-ended mode					
		• Avg = 32	12.2	13.9		hite	
		• Avg = 4	11.4	13.1		DIIS	
					_	bits	
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode				dB	7
		• Avg = 32	_	-94			
						dB	
		16-bit single-ended mode	_	-85	_		
		• Avg = 32					
SFDR	Spurious free	16-bit differential mode				dB	7
	dynamic range	• Avg = 32	82	95			
						dB	
		16-bit single-ended mode	78	90			
		• Avg = 32					
E _{IL}	Input leakage error		I _{In} × R _{AS}			mV	I _{In} = leakage current
							(refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V _{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$ 2. Typical values assume $V_{DDA} = 3.0 \text{ V}$, Temp = 25 °C, $f_{ADCK} = 2.0 \text{ MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.

- The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 4. 1 LSB = $(V_{REFH} V_{REFL})/2^{N}$
- 5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- 6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- 7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
- 8. ADC conversion clock < 3 MHz







Figure 9. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode



Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)



Figure 12. Typical INL error vs. digital code



Figure 13. Offset at half scale vs. temperature

3.7 Timers

See General switching specifications.

3.8 Communication interfaces

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f _{op}	Frequency of operation	0	f _{periph} /4	Hz	1
2	t _{SPSCK}	SPSCK period	4 x t _{periph}	—	ns	2
3	t _{Lead}	Enable lead time	1	—	t _{periph}	—
4	t _{Lag}	Enable lag time	1	—	t _{periph}	_
5	t _{WSPSCK}	Clock (SPSCK) high or low time	t _{periph} - 30	—	ns	—
6	t _{SU}	Data setup time (inputs)	2	—	ns	—
7	t _{HI}	Data hold time (inputs)	7	—	ns	_
8	t _a	Slave access time	_	t _{periph}	ns	3
9	t _{dis}	Slave MISO disable time	_	t _{periph}	ns	4
10	t _v	Data valid (after SPSCK edge)	_	122	ns	_
11	t _{HO}	Data hold time (outputs)	0	—	ns	—
12	t _{RI}	Rise time input	_	t _{periph} - 25	ns	—
	t _{FI}	Fall time input				
13	t _{RO}	Rise time output	_	36	ns	_
	t _{FO}	Fall time output				

Table 39. SPI slave mode timing on slew rate enabled pads

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).

2.

- $t_{periph} = 1/f_{periph}$ Time to data active from high-impedance state З.
- 4. Hold time to high-impedance state





Peripheral operating requirements and behaviors

- 1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can be achieved only when using the high drive pins across the full voltage range and when using the normal drive pins and VDD ≥ 2.7 V.
- The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves
 acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL
 lines.
- 3. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
- 4. Input signal Slew = 10 ns and Output Load = 50 pF
- 5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
- 6. A Fast mode I²C bus device can be used in a Standard mode I2C bus system, but the requirement t_{SU; DAT} ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax} + t_{SU; DAT} = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.
- 7. C_b = total capacitance of the one bus line in pF.

Characteristic	Symbol	Minimum	Maximum	Unit
SCL Clock Frequency	f _{SCL}	0	1 ¹	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t _{HD} ; STA	0.26	—	μs
LOW period of the SCL clock	t _{LOW}	0.5		μs
HIGH period of the SCL clock	t _{HIGH}	0.26	_	μs
Set-up time for a repeated START condition	t _{SU} ; STA	0.26		μs
Data hold time for I ₂ C bus devices	t _{HD} ; DAT	0		μs
Data set-up time	t _{SU} ; DAT	50		ns
Rise time of SDA and SCL signals	t _r	20 +0.1C _b	120	ns
Fall time of SDA and SCL signals	t _f	20 +0.1C _b ²	120	ns
Set-up time for STOP condition	t _{SU} ; STO	0.26	_	μs
Bus free time between STOP and START condition	t _{BUF}	0.5	—	μs
Pulse width of spikes that must be suppressed by the input filter	t _{SP}	0	50	ns

Table 41. I²C 1Mbit/s timing

- 1. The maximum SCL clock frequency of 1 Mbit/s can support maximum bus loading when using the high drive pins across the full voltage range.
- 2. C_b = total capacitance of the one bus line in pF.



Figure 18. Timing definition for devices on the I²C bus



Figure 20. I2S/SAI timing — slave modes

3.8.4.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

 Table 44.
 I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	-	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	_	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	_	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK		_	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	_	ns



Figure 25. 48 QFN Pinout diagram

Figure below shows the 64 MAPBGA pinouts:



Pinouts and Packaging

Figure 27. 64 LQFP Pinout diagram

5.3 Recommended connection for unused analog and digital pins

Table 46 shows the recommended connections for analog interface pins if those analog interfaces are not used in the customer's application

Pin Type	KL17	Short recommendation	Detailed recommendation	
GPIO/Analog	PTA18/EXTAL0	Float	Analog input - Float	
GPIO/Analog	PTA19/XTAL0	Float	Analog output - Float	
GPIO/Analog	PTx/DAC0_OUT	Float	Float (default is analog input)	
GPIO/Analog	PTx/ADCx	Float	Float (default is analog input)	
GPIO/Analog	PTx/CMPx	Float	Float (default is analog input)	
GPIO/Digital	PTA0/SWD_CLK	Float	Float (default is SWD with pulldown)	
GPIO/Digital	PTA3/SWD_DIO	Float	Float (default is SWD with pullup)	
GPIO/Digital	PTA4/NMI_b	10 k Ω pullup or disabled and float	Pull high or disable in PCR & FOPT and float	
GPIO/Digital	PTx	Float	Float (default is disabled)	
VDDA	VDDA	Always connect to VDD potential	Always connect to VDD potential	
VREFH	VREFH	Always connect to VDD potential	Always connect to VDD potential	
VREFL	VREFL	Always connect to VSS potential	Always connect to VSS potential	
VSSA	VSSA	Always connect to VSS potential	Always connect to VSS potential	
Reserved	Reserved	Tie to ground through 10 k Ω	Tie to ground through 10 k Ω	

Table 46. Recommended connection for unused analog interfaces

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the Web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers:

7 Part identification

8 Terminology and guidelines

8.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:
	 Operating ratings apply during operation of the chip. Handling ratings apply when the chip is not powered.
	NOTE: The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that:
	 Lies within the range of values specified by the operating behavior Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions
	NOTE: Typical values are provided as design guidelines and are neither tested nor guaranteed.