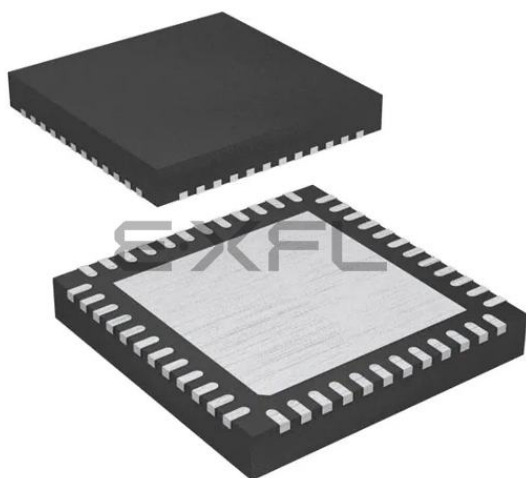




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 18x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl17z128vft4

2.2.1 Voltage and current operating requirements

Table 5. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD} -to- V_{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS} -to- V_{SSA} differential voltage	-0.1	0.1	V	
V_{IH}	Input high voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	$0.7 \times V_{DD}$	—	V	
		$0.75 \times V_{DD}$	—	V	
V_{IL}	Input low voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	—	$0.35 \times V_{DD}$	V	
		—	$0.3 \times V_{DD}$	V	
V_{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I_{ICIO}	IO pin negative DC injection current — single pin $V_{IN} < V_{SS}-0.3\text{V}$	-3	—	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins Negative current injection	-25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

1. All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} greater than V_{IO_MIN} ($= V_{SS}-0.3\text{ V}$) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|$.
2. Open drain outputs must be pulled to V_{DD} .

2.2.2 LVD and POR operating requirements

Table 6. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	—
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	—
	Low-voltage warning thresholds — high range					1

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	- at 25 °C - at 105 °C					
I _{DD_VLPRCO}	Very Low Power Run Core Mark in Flash in Compute Operation mode: Core@4MHz, Flash @1MHz, V _{DD} = 3.0 V at 25 °C	—	826	907	μA	
I _{DD_VLPRCO}	Very-low-power-run While(1) loop in SRAM in compute operation mode— 8 MHz LIRC mode, 4 MHz core / 1 MHz flash, V _{DD} = 3.0 V at 25 °C	—	405	486	μA	
I _{DD_VLPRCO}	Very-low-power run While(1) loop in SRAM in compute operation mode:—2 MHz LIRC mode, 2 MHz core / 0.5 MHz flash, V _{DD} = 3.0 V at 25 °C	—	154	235	μA	
I _{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V _{DD} = 3.0 V at 25 °C	—	108	189	μA	
I _{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V _{DD} = 3.0 V at 25 °C	—	39	120	μA	
I _{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 4 MHz core / 1 MHz flash, V _{DD} = 3.0 V at 25 °C	—	249	330	μA	
I _{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock enable, 4 MHz core / 1 MHz flash, V _{DD} = 3.0 V at 25 °C	—	337	418	μA	
I _{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 4 MHz core / 1 MHz flash, V _{DD} = 3.0 V at 25 °C	—	416	497	μA	
I _{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 4 MHz core / 1 MHz flash, V _{DD} = 3.0 V at 25 °C	—	494	575	μA	
I _{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V _{DD} = 3.0 V at 25 °C	—	166	247	μA	
I _{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock					

Table continues on the next page...

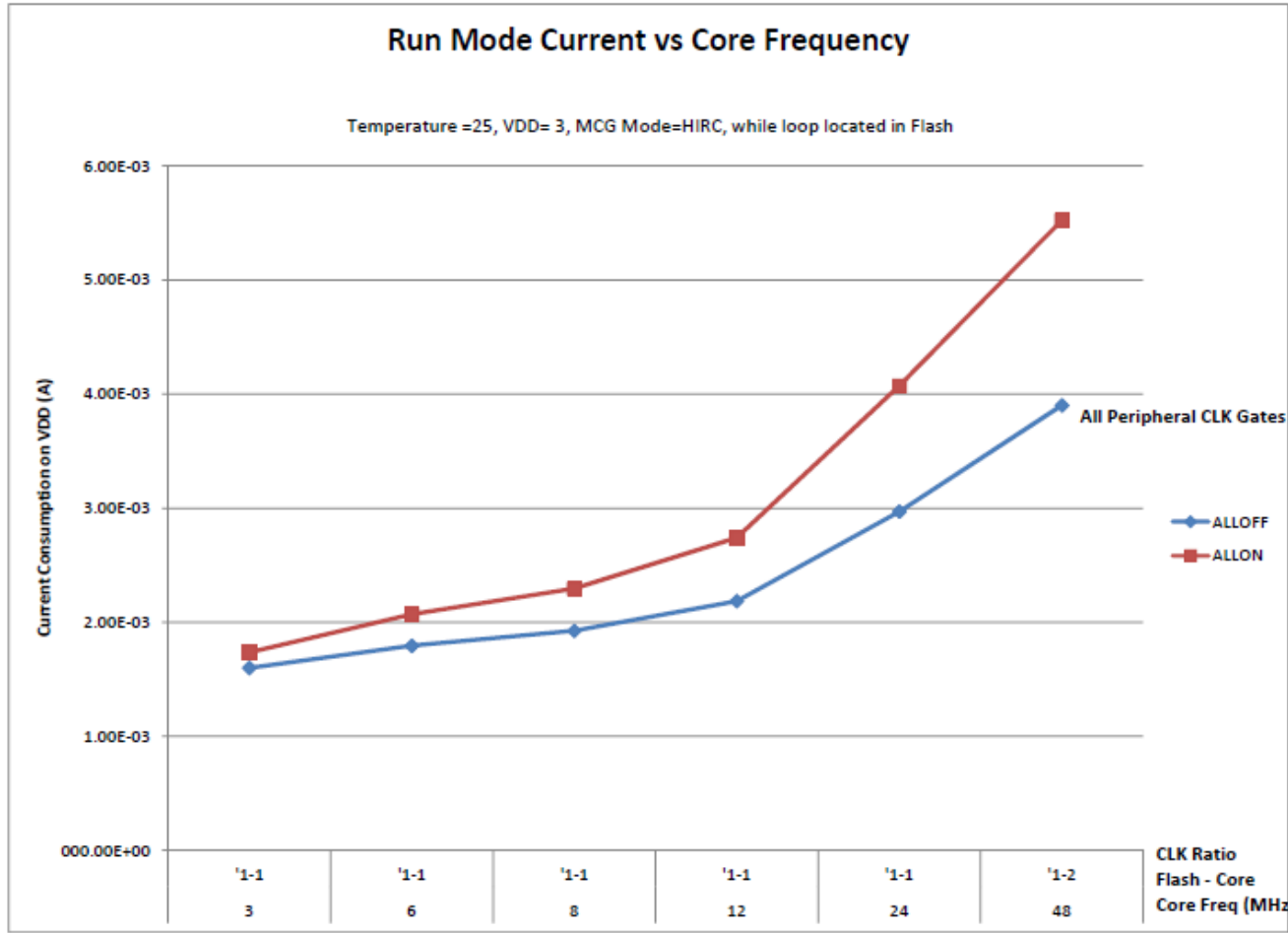
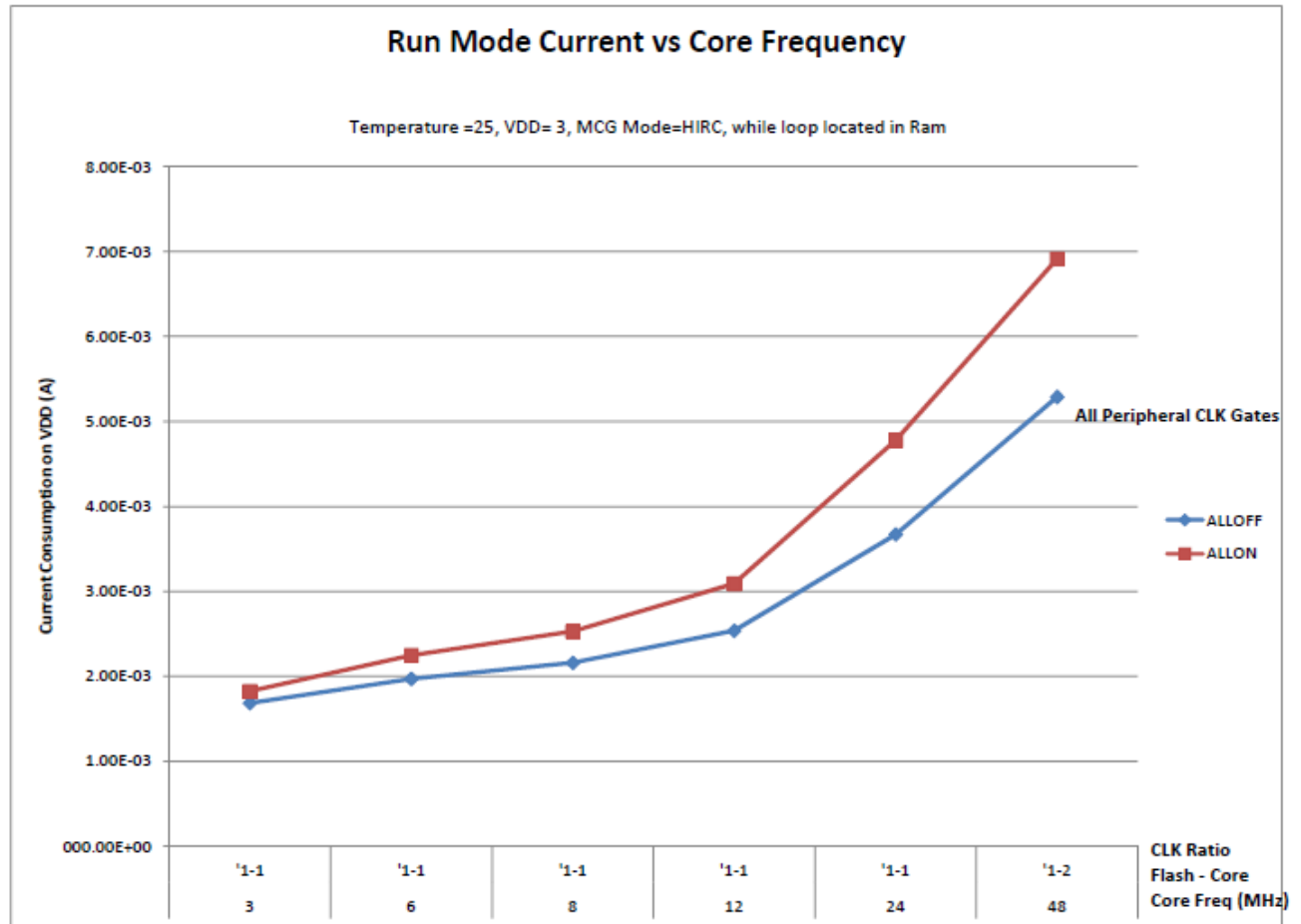


Figure 2. Run mode supply current vs. core frequency



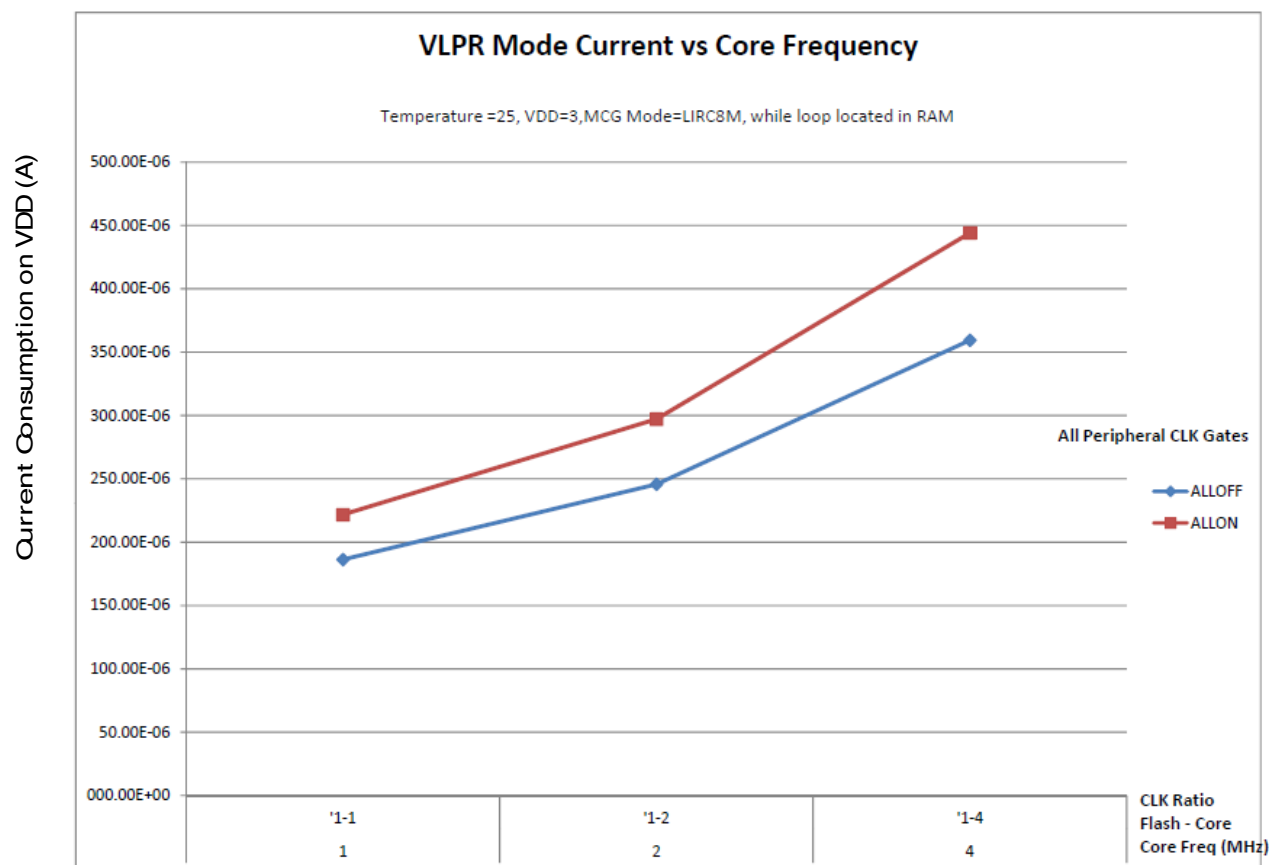


Figure 3. VLPR mode current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 11. EMC radiated emissions operating behaviors for 64-pin LQFP package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	11	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	12	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	10	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	6	dBμV	
V _{RE_IEC}	IEC level	0.15–1000	N	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement*

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$.

Table 16. Thermal operating requirements for other packages

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	−40	125	°C	
T_A	Ambient temperature	−40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$.

2.4.2 Thermal attributes

Table 17. Thermal attributes

Board type	Symbol	Description	48 QFN	32 QFN	64 LQFP	64 MAPB GA	36 WLCS P	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	86	101	70	50.3	77.6	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	29	33	51	42.9	38.9	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	71	84	58	41.4	69.6	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	24	28	45	38.0	35.6	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	12	13	33	39.6	34.8	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	1.7	1.7	20	27.3	0.37	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	3	4	0.4	0.2	°C/W	4
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom (natural convection)	-	-	-	12.6	-	°C/W	5

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.

Table 21. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	24 MHz 32 MHz	—	1.5	—	mA	
I _{DDOSC}	Supply current — high gain mode (HGO=1) 32 kHz 4 MHz 8 MHz (RANGE=01) 16 MHz 24 MHz 32 MHz	—	25 400 500 2.5 3 4	—	μA μA μA mA mA mA	1
C _x	EXTAL load capacitance	—	—	—		2, 3
C _y	XTAL load capacitance	—	—	—		2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C

2. See crystal or resonator manufacturer's recommendation

3.4.1.3 Flash high voltage current behaviors

Table 25. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I _{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I _{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.4.1.4 Reliability specifications

Table 26. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Program Flash						
t _{nvmretp10k}	Data retention after up to 10 K cycles	5	50	—	years	—
t _{nvmretp1k}	Data retention after up to 1 K cycles	20	100	—	years	—
n _{nvmcycp}	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40\text{ °C} \leq T_j \leq 125\text{ °C}$.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

Using differential inputs can achieve better system accuracy than using single-end inputs.

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
		<12-bit modes	—	±0.5	−0.7 to +0.5		
E_{FS}	Full-scale error	12-bit modes <12-bit modes	—	−4	−5.4	LSB ⁴	$V_{ADIN} = V_{DDA}$ ⁵
E_Q	Quantization error	16-bit modes ≤13-bit modes	—	−1 to 0	—	LSB ⁴	
ENOB	Effective number of bits	16-bit differential mode - Avg = 32 - Avg = 4 16-bit single-ended mode - Avg = 32 - Avg = 4	12.8 11.9	14.5 13.8	— —	bits bits	6
						bits	
						bits	
						bits	
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	
THD	Total harmonic distortion	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	—	−94	—	dB dB	7
			—	−85	—		
SFDR	Spurious free dynamic range	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	82	95	— —	dB dB	7
			78	90			
E_{IL}	Input leakage error		$I_{in} \times R_{AS}$			mV	I_{in} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$

2. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3.6.4.2 12-bit DAC operating behaviors

Table 35. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	250	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	900	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	$V_{DACR} - 100$	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	± 8	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2 V$	—	—	± 1	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF_OUT}$	—	—	± 1	LSB	4
V_{OFFSET}	Offset error	—	± 0.4	± 0.8	%FSR	5
E_G	Gain error	—	± 0.1	± 0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4 V$	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	$\mu V/C$	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
R_{op}	Output resistance (load = 3 k Ω)	—	—	250	Ω	
SR	Slew rate -80h → F7Fh → 80h - High power (SP_{HP}) - Low power (SP_{LP})	1.2 0.05	1.7 0.12	— —	V/ μs	
BW	3dB bandwidth - High power (SP_{HP}) - Low power (SP_{LP})	550 40	— —	— —	kHz	

- Settling within ± 1 LSB
- The INL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
- The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
- The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV with $V_{DDA} > 2.4 V$
- Calculated by a best fit curve from $V_{SS} + 100$ mV to $V_{DACR} - 100$ mV
- $V_{DDA} = 3.0 V$, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

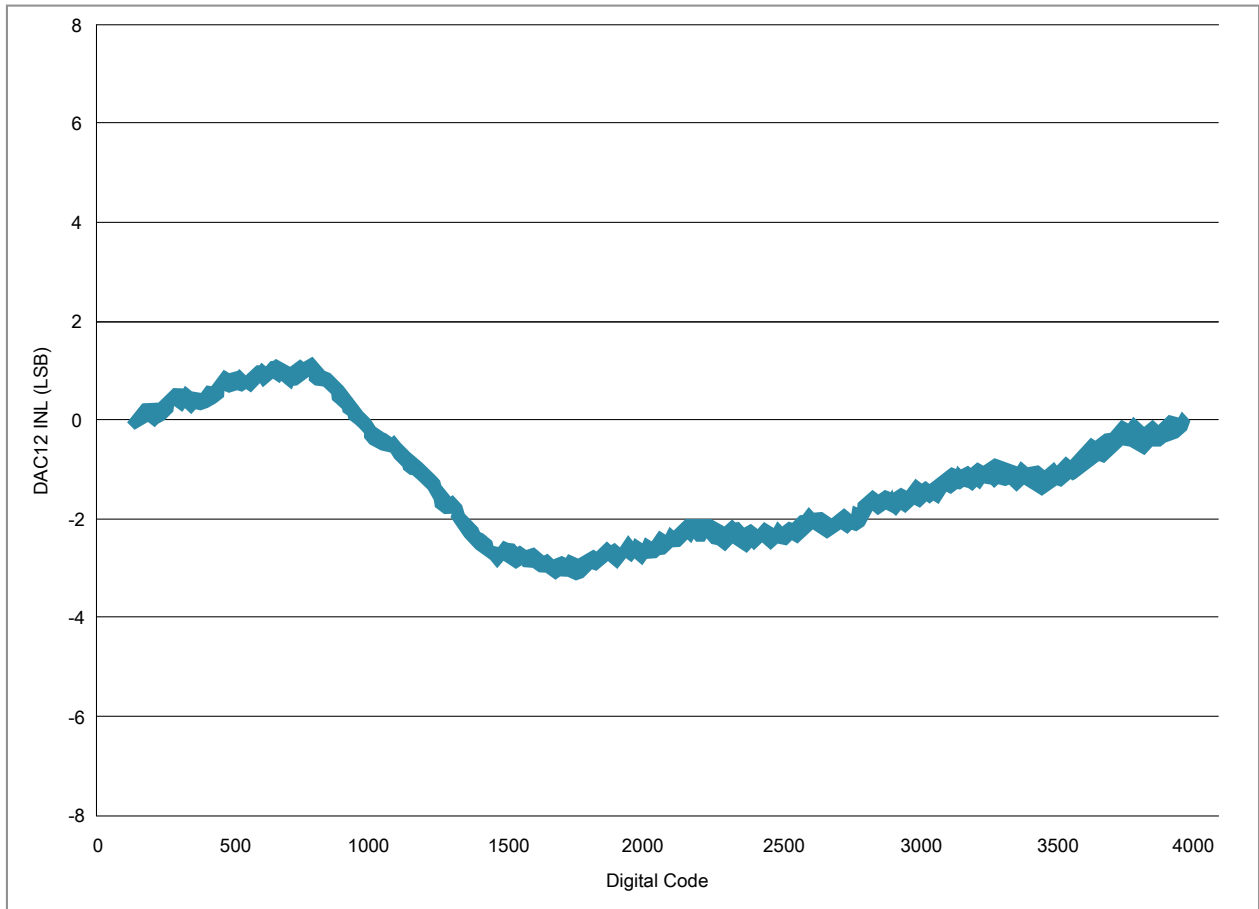


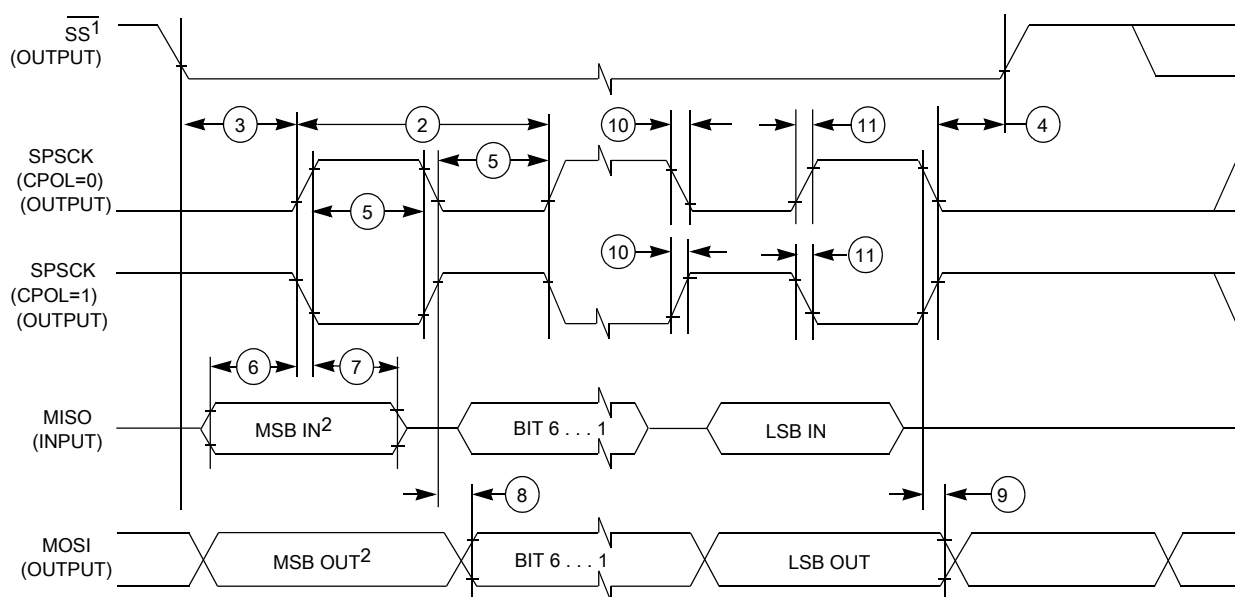
Figure 12. Typical INL error vs. digital code

Table 37. SPI master mode timing on slew rate enabled pads (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
8	t_v	Data valid (after SPSCCK edge)	—	52	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	$t_{\text{periph}} - 25$	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).

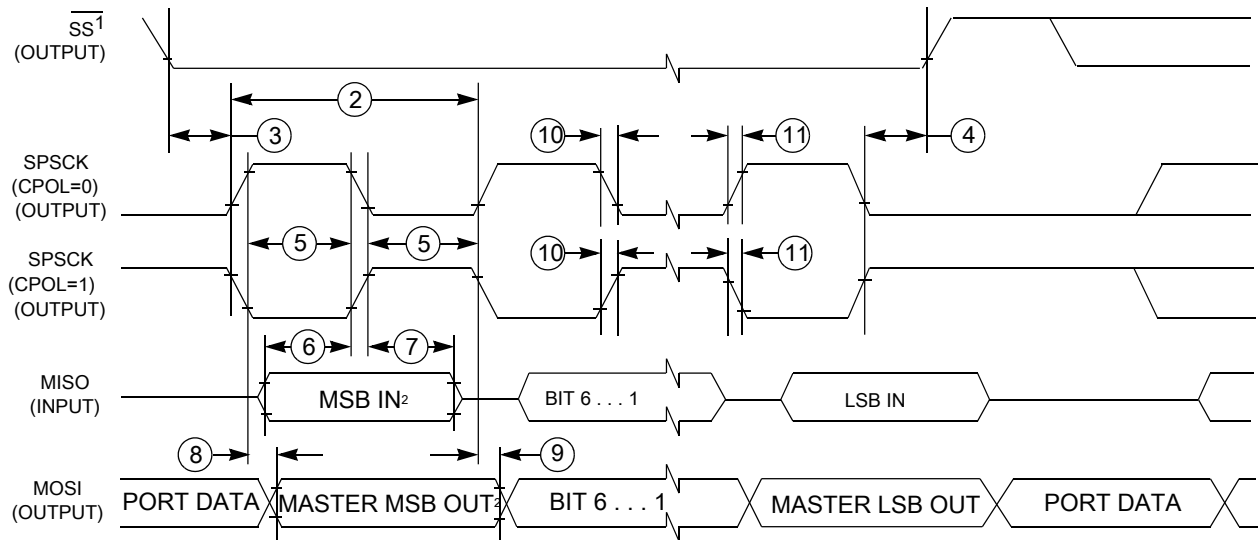
2. $t_{\text{periph}} = 1/f_{\text{periph}}$



1. If configured as an output.

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 14. SPI master mode timing (CPHA = 0)



1. If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI master mode timing (CPHA = 1)

Table 38. SPI slave mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCCK}	SPSCCK period	$4 \times t_{periph}$	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	$t_{WSPSCCK}$	Clock (SPSCCK) high or low time	$t_{periph} - 30$	—	ns	—
6	t_{SU}	Data setup time (inputs)	2.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.5	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCCK edge)	—	31	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	$t_{periph} - 25$	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).

2. $t_{periph} = 1/f_{periph}$

3. Time to data active from high-impedance state

4. Hold time to high-impedance state

Peripheral operating requirements and behaviors

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can be achieved only when using the high drive pins across the full voltage range and when using the normal drive pins and $V_{DD} \geq 2.7$ V.
2. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum t_{HD}; DAT must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement t_{SU}; DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax} + t_{SU}; DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.
7. C_b = total capacitance of the one bus line in pF.

Table 41. I²C 1Mbit/s timing

Characteristic	Symbol	Minimum	Maximum	Unit
SCL Clock Frequency	f _{SCL}	0	1 ¹	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t _{HD} ; STA	0.26	—	μs
LOW period of the SCL clock	t _{LOW}	0.5	—	μs
HIGH period of the SCL clock	t _{HIGH}	0.26	—	μs
Set-up time for a repeated START condition	t _{SU} ; STA	0.26	—	μs
Data hold time for I ² C bus devices	t _{HD} ; DAT	0	—	μs
Data set-up time	t _{SU} ; DAT	50	—	ns
Rise time of SDA and SCL signals	t _r	20 + 0.1C _b	120	ns
Fall time of SDA and SCL signals	t _f	20 + 0.1C _b ²	120	ns
Set-up time for STOP condition	t _{SU} ; STO	0.26	—	μs
Bus free time between STOP and START condition	t _{BUF}	0.5	—	μs
Pulse width of spikes that must be suppressed by the input filter	t _{SP}	0	50	ns

1. The maximum SCL clock frequency of 1 Mbit/s can support maximum bus loading when using the high drive pins across the full voltage range.
2. C_b = total capacitance of the one bus line in pF.

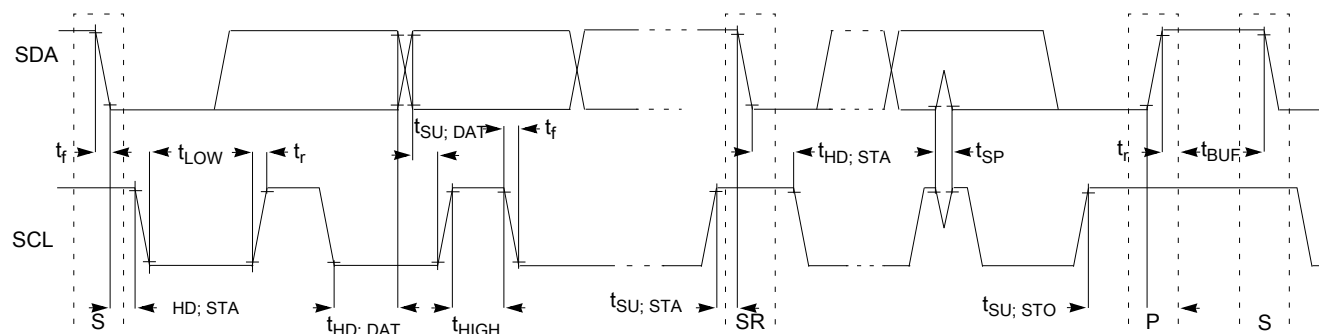


Figure 18. Timing definition for devices on the I²C bus

Pinouts and Packaging

64 MAP BGA	64 LQFP	48 QFN	36 WLC SP	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
E8	38	30	—	—	PTB3	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	TPM2_CH1				
E6	39	31	—	—	PTB16	DISABLED		PTB16	SPI1_MOSI	LPUART0_RX	TPM_CLKIN0	SPI1_MISO		
D7	40	32	—	—	PTB17	DISABLED		PTB17	SPI1_MISO	LPUART0_TX	TPM_CLKIN1	SPI1_MOSI		
D6	41	—	—	—	PTB18	DISABLED		PTB18		TPM2_CH0	I2S0_TX_BCLK			
C7	42	—	—	—	PTB19	DISABLED		PTB19		TPM2_CH1	I2S0_TX_FS			
D8	43	33	—	—	PTC0	ADC0_SE14	ADC0_SE14	PTC0		EXTRG_IN	audioUSB_SOF_OUT	CMP0_OUT	I2S0_TXD0	
C6	44	34	B1	22	PTC1/ LLWU_P6/ RTC_CLKIN	ADC0_SE15	ADC0_SE15	PTC1/ LLWU_P6/ RTC_CLKIN	I2C1_SCL		TPM0_CH0		I2S0_TXD0	
B7	45	35	B2	23	PTC2	ADC0_SE11	ADC0_SE11	PTC2	I2C1_SDA		TPM0_CH1		I2S0_TX_FS	
C8	46	36	A1	24	PTC3/ LLWU_P7	DISABLED		PTC3/ LLWU_P7	SPI1_SCK	LPUART1_RX	TPM0_CH2	CLKOUT	I2S0_TX_BCLK	
E3	47	—	C4	—	VSS	VSS	VSS							
E4	48	—	B3	—	VDD	VDD	VDD							
B8	49	37	A2	25	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	LPUART1_TX	TPM0_CH3	I2S0_MCLK		
A8	50	38	A3	26	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0		CMP0_OUT	
A7	51	39	B4	27	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_MOSI	EXTRG_IN	I2S0_RX_BCLK	SPI0_MISO	I2S0_MCLK	
B6	52	40	A4	28	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_MISO	audioUSB_SOF_OUT	I2S0_RX_FS	SPI0_MOSI		
A6	53	—	—	—	PTC8	CMP0_IN2	CMP0_IN2	PTC8	I2C0_SCL	TPM0_CH4	I2S0_MCLK			
B5	54	—	—	—	PTC9	CMP0_IN3	CMP0_IN3	PTC9	I2C0_SDA	TPM0_CH5	I2S0_RX_BCLK			
B4	55	—	—	—	PTC10	DISABLED		PTC10	I2C1_SCL		I2S0_RX_FS			
A5	56	—	—	—	PTC11	DISABLED		PTC11	I2C1_SDA		I2S0_RXD0			
C3	57	41	—	—	PTD0	DISABLED		PTD0	SPI0_PCS0		TPM0_CH0		FXIO0_D0	
A4	58	42	—	—	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1		FXIO0_D1	
C2	59	43	—	—	PTD2	DISABLED		PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO	FXIO0_D2	
B3	60	44	—	—	PTD3	DISABLED		PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI	FXIO0_D3	
A3	61	45	A5	29	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI1_PCS0	UART2_RX	TPM0_CH4		FXIO0_D4	
C1	62	46	B5	30	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5		FXIO0_D5	
B2	63	47	A6	31	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI1_MOSI	LPUART0_RX		SPI1_MISO	FXIO0_D6	

Pinouts and Packaging

	1	2	3	4	5	6	7	8	
A	PTE0	PTD7	PTD4/ LLWU_P14	PTD1	PTC11	PTC8	PTC6/ LLWU_P10	PTC5/ LLWU_P9	A
B	PTE1	PTD6/ LLWU_P15	PTD3	PTC10	PTC9	PTC7	PTC2	PTC4/ LLWU_P8	B
C	PTD5	PTD2	PTD0	VSS	NC	PTC1/ LLWU_P6/ RTC_CLKIN	PTB19	PTC3/ LLWU_P7	C
D	PTE17	PTE19	PTA0	PTA1	PTA3	PTB18	PTB17	PTC0	D
E	PTE16	PTE18	VSS	VDD	PTA2	PTB16	PTB2	PTB3	E
F	PTE21	PTE23	VSSA	VDDA	PTA5	PTB1	PTB0/ LLWU_P5	PTA20	F
G	PTE20	PTE22	VREFL	VREFH	PTA4	PTA13	VDD	PTA19	G
H	PTE29	PTE30	PTE31	PTE24	PTE25	PTA12	VSS	PTA18	H
	1	2	3	4	5	6	7	8	

Figure 26. 64 MAPBGA Pinout diagram:

Figure below shows the 64 LQFP pinouts:

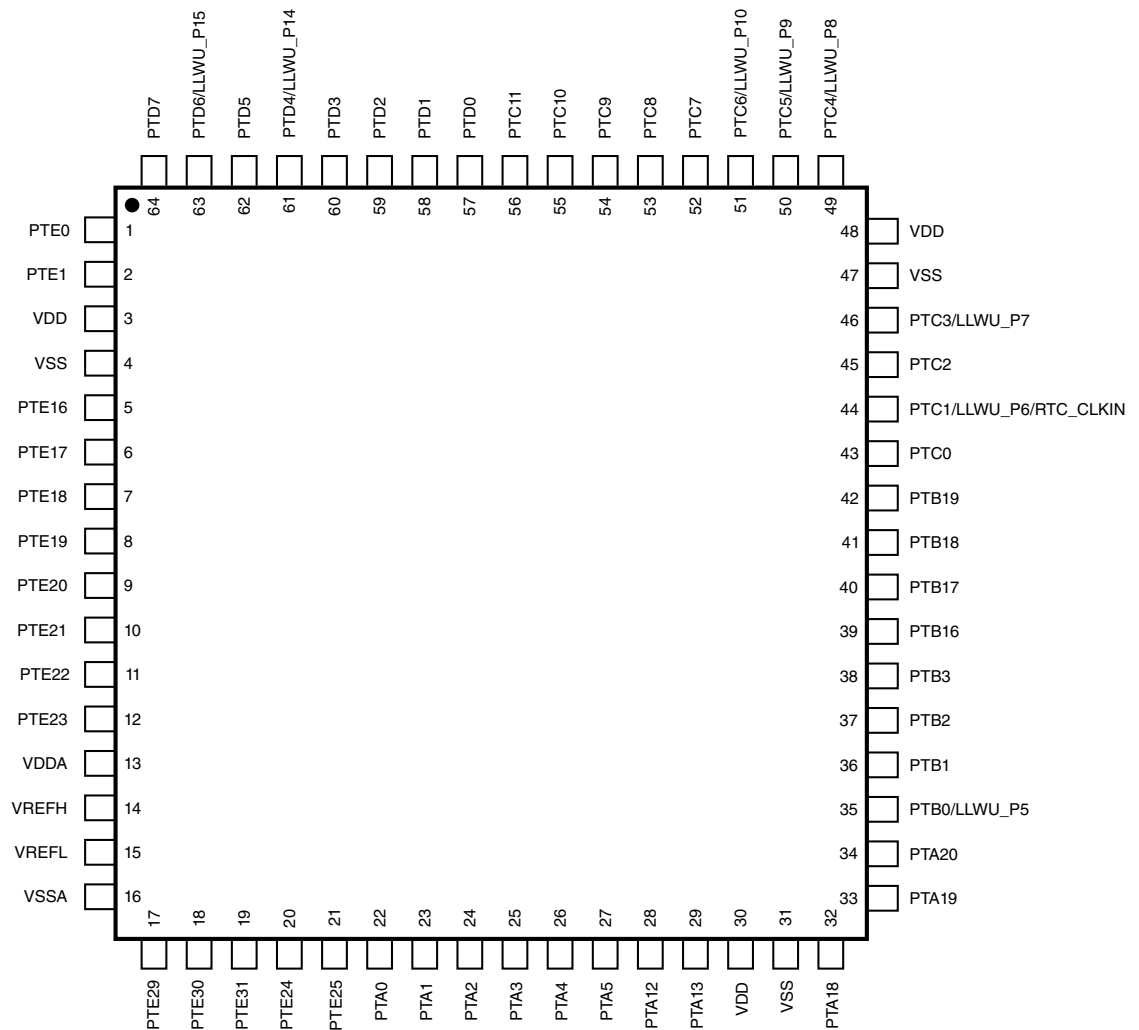


Figure 27. 64 LQFP Pinout diagram

5.3 Recommended connection for unused analog and digital pins

Table 46 shows the recommended connections for analog interface pins if those analog interfaces are not used in the customer's application

Table 46. Recommended connection for unused analog interfaces

Pin Type	KL17	Short recommendation	Detailed recommendation
GPIO/Analog	PTA18/EXTAL0	Float	Analog input - Float
GPIO/Analog	PTA19/XTAL0	Float	Analog output - Float
GPIO/Analog	PTx/DAC0_OUT	Float	Float (default is analog input)
GPIO/Analog	PTx/ADCx	Float	Float (default is analog input)
GPIO/Analog	PTx/CMPx	Float	Float (default is analog input)
GPIO/Digital	PTA0/SWD_CLK	Float	Float (default is SWD with pulldown)
GPIO/Digital	PTA3/SWD_DIO	Float	Float (default is SWD with pullup)
GPIO/Digital	PTA4/NMI_b	10 k Ω pullup or disabled and float	Pull high or disable in PCR & FOPT and float
GPIO/Digital	PTx	Float	Float (default is disabled)
VDDA	VDDA	Always connect to VDD potential	Always connect to VDD potential
VREFH	VREFH	Always connect to VDD potential	Always connect to VDD potential
VREFL	VREFL	Always connect to VSS potential	Always connect to VSS potential
VSSA	VSSA	Always connect to VSS potential	Always connect to VSS potential
Reserved	Reserved	Tie to ground through 10 k Ω	Tie to ground through 10 k Ω

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the Web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers:

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 47. Part number fields descriptions

Field	Description	Values
Q	Qualification status	- M = Fully qualified, general market flow - P = Prequalification
KL##	Kinetis family	KL17
A	Key attribute	Z = Cortex-M0+
FFF	Program flash memory size	128 = 128 KB 256 = 256 KB
R	Silicon revision	(Blank) = Main - A = Revision after main
T	Temperature range (°C)	- V = -40 to 105 - C = -40 to 85
PP	Package identifier	- FM = 32 QFN (5 mm x 5 mm) - AL = 36 WLCSP (2.8 mm x 2.7 mm) - FT = 48 QFN (7 mm x 7 mm) - LH = 64 LQFP (10 mm x 10 mm) - MP = 64 MAPBGA (5 mm x 5 mm)
CC	Maximum CPU frequency (MHz)	4 = 48 MHz
N	Packaging type	R = Tape and reel

7.4 Example

This is an example part number:

Table 48. Revision History (continued)

Rev. No.	Date	Substantial Changes
		- Updated Related Resources table to include Chip Errata resource name and Package Drawing part numbers in the respective rows. Also updated Product Brief resource references. - Updated Table 7. Voltage and current operating behaviors. - Specified correct max. value for I_{IN}. - Updated Table - 9 Power consumption operating behaviors. - Rows added for IDD for reset pin hold low ($I_{DD_RESET_LOW}$) at 1.7V and 3V. - Measurement unit updated for I_{DD_VLLS1} from nA to μA. - Footnote 1 was moved in the beginning of the table as text. - Added Table - 11 EMC radiated emissions operating behaviors for 64-pin LQFP package under section 2.2.6. - Updated Table - 18 (IRC48M specification) and Table - 19 (IRC8M/2M specification) under section 3.3.1 - 'MCG-Lite specifications'. - Removed supply voltage (V_{DD}), temperature range (T), untrimmed (f_{IRC_UT}), trim function (Δf_{IRC_C}, Δf_{IRC_F}) data from Table - 18 (IRC48M specification). - Removed supply voltage (V_{DD}), temperature range (T) data from Table - 19 (IRC8M/2M specification). - Added Figure 6. IRC8M Frequency Drift vs Temperature curve after Table - 19 (IRC8M/2M specification). - Updated Table 29. VREF full-range operating behaviors. - Removed A_c(Aging coefficient) row. - Added $T_{chop_osc_stup}$ parameter. - Added tables: "I2C timing" and "I2C 1Mbit/s timing" under section - I²C. - Added VREF specifications (V_{REFH} and V_{REFL}) to Table 26. 16-bit ADC operating conditions. - Removed note: "This device does not have the USB_CLKIN signal available."
5	12 August 2015	- In Table 9. Power consumption operating behaviors: - Updated Max. values of I_{DD_WAIT}, I_{DD_VLPW}, I_{DD_STOP}, I_{DD_VLPS}, I_{DD_LLS}, I_{DD_VLLS3}, I_{DD_VLLS1}, I_{DD_VLLS0}. - Modified unit of I_{DD_VLLS0} from nA to μA. - Removed $I_{DD_RESET_LOW}$ information. - In Table 13. Device clock specifications, added a footnote for normal run mode. - In Table 15. Thermal operating requirements, modified the footnote for Ambient temperature. - In Table 18. IRC48M specification, removed f_{IRC_T} data and added $\Delta f_{irc48m_of_lv}$ and $\Delta f_{irc48m_of_hv}$ specifications. - In Table 26. 16-bit ADC operating conditions, updated Max. value of f_{ADCK} and C_{rate}.
5.1	16 Nov 2015	Added 36-pin WLCSP package information.
6	25 Jan 2016	Completed all the TBDs of the 36-pin WLCSP package.