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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 18x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl17z256vft4r

Related Resources (continued)

Type	Description	Resource
Package drawing	Package dimensions are provided in package drawings.	64-LQFP: 98ASS23234W ¹ 64-MAPBGA: 98ASA00420D ¹ 32-QFN: 98ASA00615D ¹ 48-QFN: 98ASA00616D ¹ 36-WLCSP: 98ASA00949D ¹

1. To find the associated resource, go to <http://www.nxp.com> and perform a search using this term.

1 Ratings

1.1 Thermal handling ratings

Table 1. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	–55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Table 2. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Table 3. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105 °C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

Table 7. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	<ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 18\text{ mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 6\text{ mA}$ 	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	μA	2
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	μA	2
I_{IN}	Input leakage current (total all pins) for full temperature range	—	64	μA	2
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
R_{PU}	Internal pullup resistors	20	50	k Ω	3

1. PTB0, PTB1, PTC3, PTC4, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at $V_{DD} = 3.6\text{ V}$
3. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{SS}$

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and $VLLSx \rightarrow \text{RUN}$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- HIRC clock mode

Table 8. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	μs	1
	• $VLLS0 \rightarrow \text{RUN}$	—	152	166	μs	
	• $VLLS1 \rightarrow \text{RUN}$	—	152	166	μs	
	• $VLLS3 \rightarrow \text{RUN}$	—	93	104	μs	
	• $LLS \rightarrow \text{RUN}$	—	7.5	8	μs	

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> at 25 °C at 105 °C 	—	3.95	4.59	mA	
		—	4.23	4.87		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, $V_{DD} = 3.0\text{ V}$ <ul style="list-style-type: none"> at 25 °C at 105 °C 	—	2.68	3.32	mA	2
		—	2.96	3.60		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, $V_{DD} = 3.0\text{ V}$ <ul style="list-style-type: none"> at 25 °C at 105 °C 	—	8.08	8.72	mA	2
		—	8.39	9.03		
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, $V_{DD} = 3.0\text{ V}$ <ul style="list-style-type: none"> at 25 °C at 105 °C 	—	3.90	4.54	mA	
		—	4.21	4.85		
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, $V_{DD} = 3.0\text{ V}$ <ul style="list-style-type: none"> at 25 °C at 105 °C 	—	2.66	3.30	mA	
		—	2.94	3.58		
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, $V_{DD} = 3.0\text{ V}$ <ul style="list-style-type: none"> at 25 °C at 105 °C 	—	2.03	2.67	mA	
		—	2.31	2.95		
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, $V_{DD} = 3.0\text{ V}$ <ul style="list-style-type: none"> at 25 °C at 105 °C 	—	5.52	6.16	mA	
		—	5.83	6.47		
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock disable, 48 MHz core/24 MHz flash, $V_{DD} = 3.0\text{ V}$ <ul style="list-style-type: none"> at 25 °C at 105 °C 	—	5.29	5.93	mA	
		—	5.56	6.20		
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock enable, 48 MHz core/24 MHz flash, $V_{DD} = 3.0\text{ V}$	—	6.91	7.55	mA	
		—	7.19	7.91		

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> at 25 °C at 105 °C 					
I_{DD_VLPRCO}	Very Low Power Run Core Mark in Flash in Compute Operation mode: Core@4MHz, Flash @1MHz, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C 	—	826	907	μA	
I_{DD_VLPRCO}	Very-low-power-run While(1) loop in SRAM in compute operation mode— 8 MHz LIRC mode, 4 MHz core / 1 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C 	—	405	486	μA	
I_{DD_VLPRCO}	Very-low-power run While(1) loop in SRAM in compute operation mode:—2 MHz LIRC mode, 2 MHz core / 0.5 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C 	—	154	235	μA	
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 2 MHz core / 0.5 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C 	—	108	189	μA	
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 125 kHz core / 31.25 kHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C 	—	39	120	μA	
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 4 MHz core / 1 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C 	—	249	330	μA	
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock enable, 4 MHz core / 1 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C 	—	337	418	μA	
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 4 MHz core / 1 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C 	—	416	497	μA	
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 4 MHz core / 1 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C 	—	494	575	μA	
I_{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 2 MHz core / 0.5 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C 	—	166	247	μA	
I_{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock					

Table continues on the next page...

Table 9. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> at 25 °C and below at 50 °C at 70 °C at 85 °C at 105 °C 	—	0.18	0.28	μA	
		—	1.09	1.31		
		—	2.25	2.94		
		—	4.25	5.10		
		—	15.95	19.10		

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG_Lite configured for HIRC mode. CoreMark benchmark compiled using IAR 7.10 with optimization level high, optimized for balanced.
3. RTC uses external 32 kHz crystal as clock source, and the current includes ERCLK32K power consumption.

Table 10. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I _{IRC8MHz}	8 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 8 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	93	93	93	93	93	93	μA
I _{IRC2MHz}	2 MHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 2 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	29	29	29	29	29	29	μA
I _{EREFSTEN4MHz}	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	224	230	238	245	253	μA
I _{EREFSTEN32KHz}	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled. <ul style="list-style-type: none"> VLLS1 VLLS3 LLS VLPS STOP 							nA
		440	490	540	560	570	580	
		440	490	540	560	570	580	
		490	490	540	560	570	680	
		510	560	560	560	610	680	
		510	560	560	560	610	680	
I _{LPTMR}	LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO.	30	30	30	85	100	200	

Table continues on the next page...

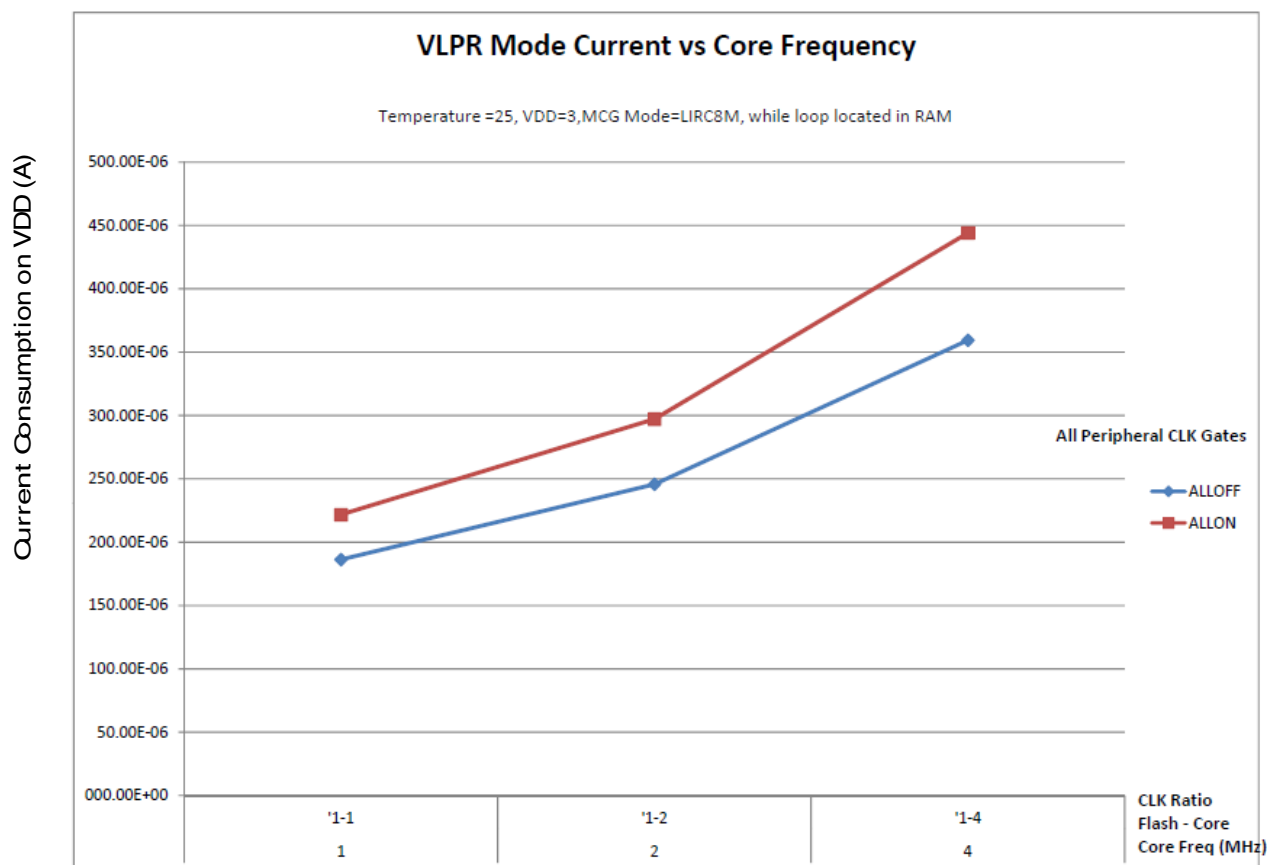


Figure 3. VLPR mode current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 11. EMC radiated emissions operating behaviors for 64-pin LQFP package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	11	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	12	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	10	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	6	dBμV	
V _{RE_IEC}	IEC level	0.15–1000	N	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement*

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$.

Table 16. Thermal operating requirements for other packages

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	−40	125	°C	
T_A	Ambient temperature	−40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$.

2.4.2 Thermal attributes

Table 17. Thermal attributes

Board type	Symbol	Description	48 QFN	32 QFN	64 LQFP	64 MAPB GA	36 WLCS P	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	86	101	70	50.3	77.6	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	29	33	51	42.9	38.9	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	71	84	58	41.4	69.6	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	24	28	45	38.0	35.6	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	12	13	33	39.6	34.8	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	1.7	1.7	20	27.3	0.37	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	3	4	0.4	0.2	°C/W	4
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom (natural convection)	-	-	-	12.6	-	°C/W	5

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.

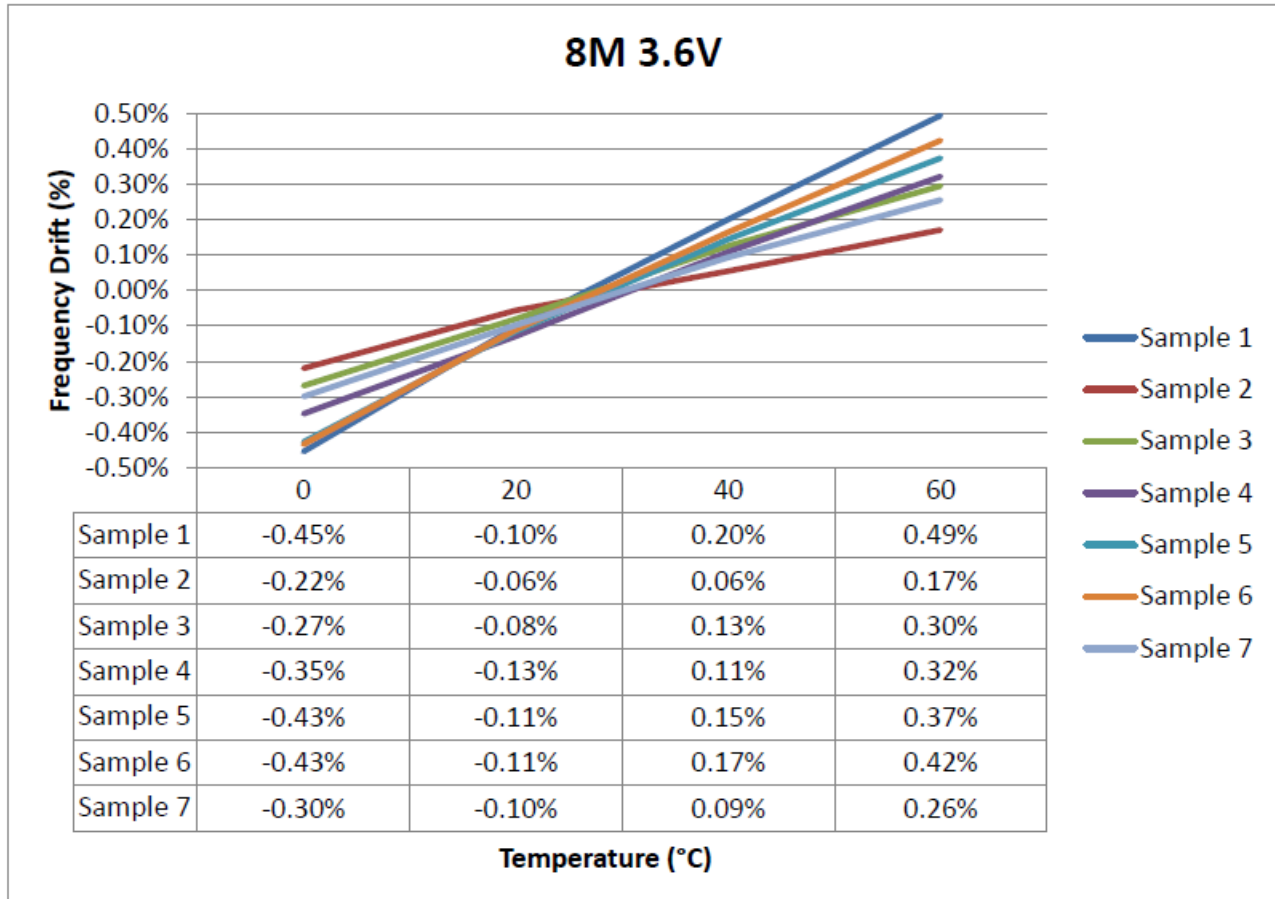


Figure 6. IRC8M Frequency Drift vs Temperature curve

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 21. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	—	3.6	V	
I _{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	μA	
	• 8 MHz (RANGE=01)	—	300	—	μA	
	• 16 MHz	—	950	—	μA	
		—	1.2	—	mA	

Table continues on the next page...

3. C_x, C_y can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 22. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc_hi_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc_hi_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.6.2 Voltage reference electrical specifications

Table 29. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V _{DDA}	Supply voltage		3.6	V	
T _A	Temperature	Operating temperature range of the device		°C	
C _L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 30 is tested under the condition of setting VREF_TRM[CHOPEN], VREF_SC[REGEN] and VREF_SC[ICOMPEN] bits to 1.

Table 30. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{out}	Voltage reference output with factory trim at nominal V _{DDA} and temperature=25°C	1.1915	1.195	1.1977	V	1
V _{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	1
V _{out}	Voltage reference output — user trim	1.193	—	1.197	V	1
V _{step}	Voltage reference trim step	—	0.5	—	mV	1
V _{tdrift}	Temperature drift (V _{max} -V _{min} across the full temperature range: 0 to 70°C)	—	—	50	mV	1
I _{bg}	Bandgap only current	—	—	80	μA	1
I _{lp}	Low-power buffer current	—	—	360	μA	1
I _{hp}	High-power buffer current	—	—	1	mA	1
ΔV _{LOAD}	Load regulation • current = ± 1.0 mA	—	200	—	μV	1, 2
T _{stup}	Buffer startup time	—	—	100	μs	
T _{chop_osc_st up}	Internal bandgap start-up delay with chop oscillator enabled	—	—	35	ms	—
V _{vdift}	Voltage drift (V _{max} -V _{min} across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

3.6.4.2 12-bit DAC operating behaviors

Table 35. 12-bit DAC operating behaviors

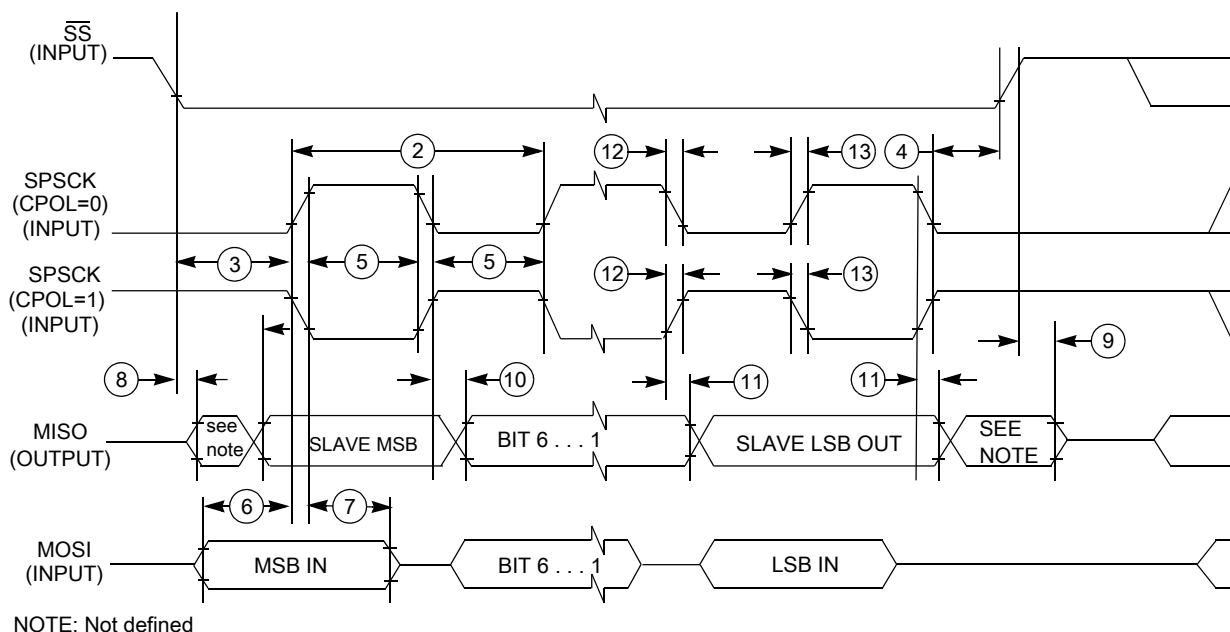
Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	250	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	900	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	$V_{DACR} - 100$	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	± 8	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2 V$	—	—	± 1	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF_OUT}$	—	—	± 1	LSB	4
V_{OFFSET}	Offset error	—	± 0.4	± 0.8	%FSR	5
E_G	Gain error	—	± 0.1	± 0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4 V$	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	$\mu V/C$	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
R_{op}	Output resistance (load = 3 k Ω)	—	—	250	Ω	
SR	Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> High power (SP_{HP}) Low power (SP_{LP}) 	1.2 0.05	1.7 0.12	— —	V/ μs	
BW	3dB bandwidth <ul style="list-style-type: none"> High power (SP_{HP}) Low power (SP_{LP}) 	550 40	— —	— —	kHz	

- Settling within ± 1 LSB
- The INL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
- The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
- The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV with $V_{DDA} > 2.4 V$
- Calculated by a best fit curve from $V_{SS} + 100$ mV to $V_{DACR} - 100$ mV
- $V_{DDA} = 3.0 V$, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

Table 39. SPI slave mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	$4 \times t_{periph}$	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{periph} - 30$	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	122	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	$t_{periph} - 25$	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

**Figure 16. SPI slave mode timing (CPHA = 0)**

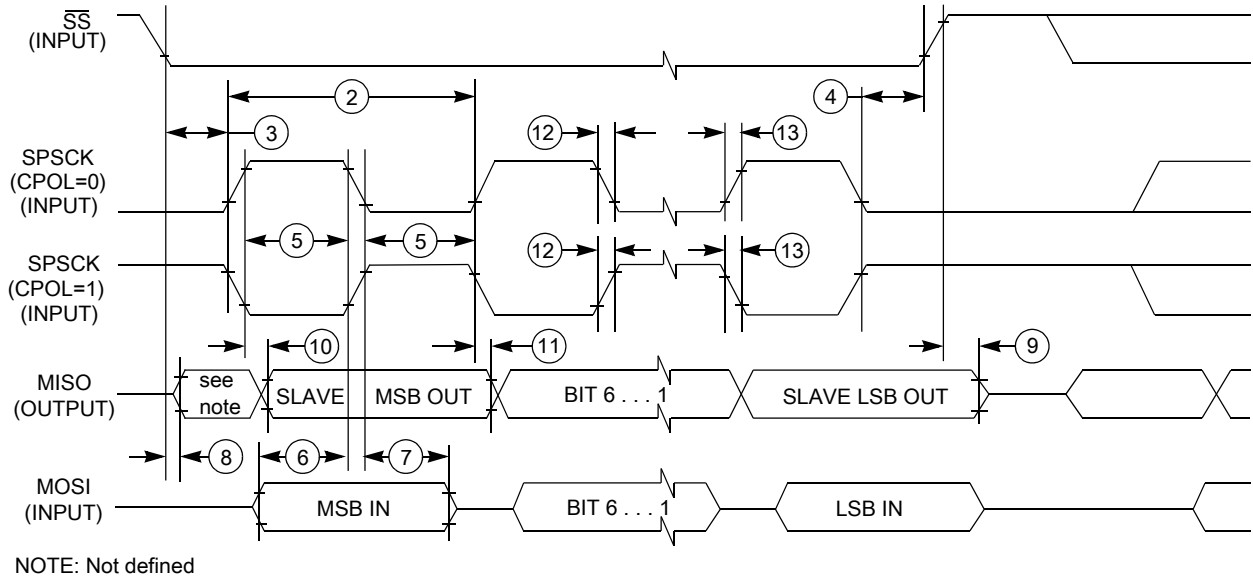


Figure 17. SPI slave mode timing (CPHA = 1)

3.8.2 I²C

3.8.2.1 Inter-Integrated Circuit Interface (I²C) timing

Table 40. I²C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f _{SCL}	0	100	0	400 ¹	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t _{HD} ; STA	4	—	0.6	—	μs
LOW period of the SCL clock	t _{LOW}	4.7	—	1.25	—	μs
HIGH period of the SCL clock	t _{HIGH}	4	—	0.6	—	μs
Set-up time for a repeated START condition	t _{SU} ; STA	4.7	—	0.6	—	μs
Data hold time for I ² C bus devices	t _{HD} ; DAT	0 ²	3.45 ³	0 ⁴	0.9 ²	μs
Data set-up time	t _{SU} ; DAT	250 ⁵	—	100 ^{3, 6}	—	ns
Rise time of SDA and SCL signals	t _r	—	1000	20 + 0.1C _b ⁷	300	ns
Fall time of SDA and SCL signals	t _f	—	300	20 + 0.1C _b ⁶	300	ns
Set-up time for STOP condition	t _{SU} ; STO	4	—	0.6	—	μs
Bus free time between STOP and START condition	t _{BUF}	4.7	—	1.3	—	μs
Pulse width of spikes that must be suppressed by the input filter	t _{SP}	N/A	N/A	0	50	ns

Peripheral operating requirements and behaviors

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can be achieved only when using the high drive pins across the full voltage range and when using the normal drive pins and $V_{DD} \geq 2.7$ V.
2. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum t_{HD}; DAT must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement t_{SU}; DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax} + t_{SU}; DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.
7. C_b = total capacitance of the one bus line in pF.

Table 41. I²C 1Mbit/s timing

Characteristic	Symbol	Minimum	Maximum	Unit
SCL Clock Frequency	f _{SCL}	0	1 ¹	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t _{HD} ; STA	0.26	—	μs
LOW period of the SCL clock	t _{LOW}	0.5	—	μs
HIGH period of the SCL clock	t _{HIGH}	0.26	—	μs
Set-up time for a repeated START condition	t _{SU} ; STA	0.26	—	μs
Data hold time for I ² C bus devices	t _{HD} ; DAT	0	—	μs
Data set-up time	t _{SU} ; DAT	50	—	ns
Rise time of SDA and SCL signals	t _r	20 + 0.1C _b	120	ns
Fall time of SDA and SCL signals	t _f	20 + 0.1C _b ²	120	ns
Set-up time for STOP condition	t _{SU} ; STO	0.26	—	μs
Bus free time between STOP and START condition	t _{BUF}	0.5	—	μs
Pulse width of spikes that must be suppressed by the input filter	t _{SP}	0	50	ns

1. The maximum SCL clock frequency of 1 Mbit/s can support maximum bus loading when using the high drive pins across the full voltage range.
2. C_b = total capacitance of the one bus line in pF.

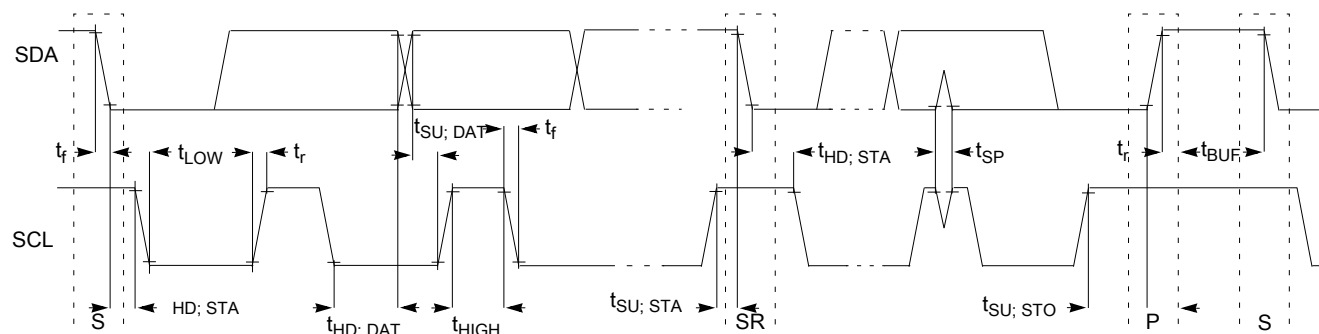


Figure 18. Timing definition for devices on the I²C bus

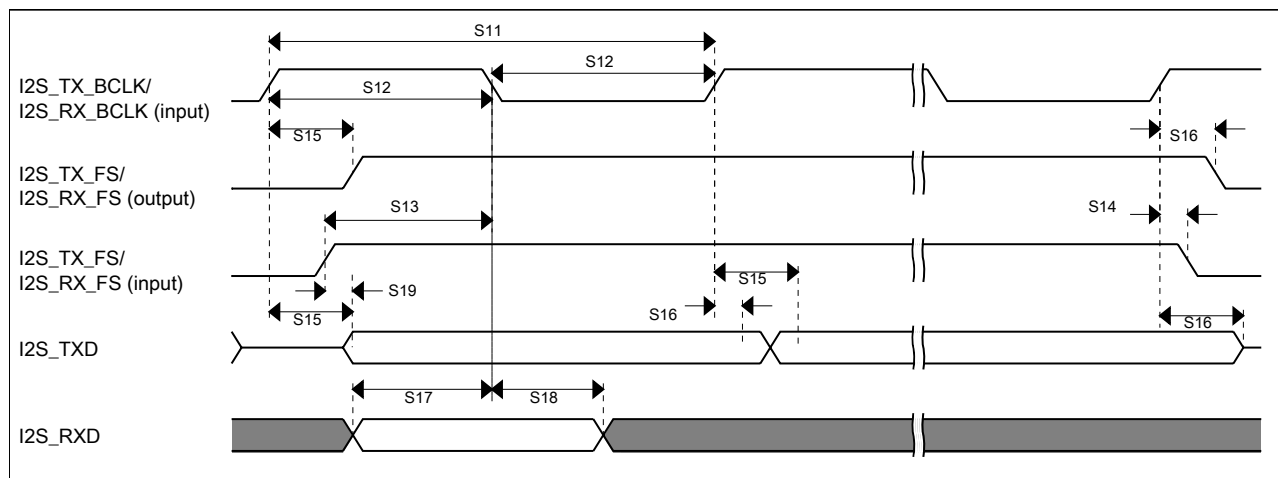


Figure 22. I2S/SAI timing — slave modes

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin QFN	98ASA00615D
36-pin WLCSP	98ASA00949D
48-pin QFN	98ASA00616D
64-pin LQFP	98ASS23234W
64-pin MAPBGA	98ASA00420D

5 Pinouts and Packaging

5.1 KL17 signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

VREFH can act as VREF_OUT when VREFV1 module is enabled.

NOTE

It is prohibited to set VREFEN in 32 QFN and 36 WLCSP pin packages because 1.2 V on-chip voltage is not available in these packages.

64 MAP BGA	64 LQFP	48 QFN	36 WLC SP	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
A1	1	—	—	1	PTE0	DISABLED		PTE0/ CLKOUT32 K	SPI1_MISO	LPUART1_ TX	RTC_ CLKOUT	CMP0_OUT	I2C1_SDA	
B1	2	—	—	2	PTE1	DISABLED		PTE1	SPI1_MOSI	LPUART1_ RX		SPI1_MISO	I2C1_SCL	
—	3	1	—	—	VDD	VDD	VDD							
C4	4	2	—	—	VSS	VSS	VSS							
E1	5	3	—	3	PTE16	ADC0_DP1/ ADC0_SE1	ADC0_DP1/ ADC0_SE1	PTE16	SPI0_PCS0	UART2_TX	TPM_ CLKIN0		FXIO0_D0	
D1	6	4	—	4	PTE17	ADC0_DM1/ ADC0_SE5a	ADC0_DM1/ ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	TPM_ CLKIN1	LPTMR0_ ALT3	FXIO0_D1	
E2	7	5	—	5	PTE18	ADC0_DP2/ ADC0_SE2	ADC0_DP2/ ADC0_SE2	PTE18	SPI0_MOSI		I2C0_SDA	SPI0_MISO	FXIO0_D2	
D2	8	6	—	6	PTE19	ADC0_DM2/ ADC0_SE6a	ADC0_DM2/ ADC0_SE6a	PTE19	SPI0_MISO		I2C0_SCL	SPI0_MOSI	FXIO0_D3	
G1	9	7	—	—	PTE20	ADC0_DP0/ ADC0_SE0	ADC0_DP0/ ADC0_SE0	PTE20		TPM1_CH0	LPUART0_ TX		FXIO0_D4	
F1	10	8	—	—	PTE21	ADC0_DM0/ ADC0_SE4a	ADC0_DM0/ ADC0_SE4a	PTE21		TPM1_CH1	LPUART0_ RX		FXIO0_D5	
G2	11	—	—	—	PTE22	ADC0_DP3/ ADC0_SE3	ADC0_DP3/ ADC0_SE3	PTE22		TPM2_CH0	UART2_TX		FXIO0_D6	
F2	12	—	—	—	PTE23	ADC0_DM3/ ADC0_SE7a	ADC0_DM3/ ADC0_SE7a	PTE23		TPM2_CH1	UART2_RX		FXIO0_D7	

Pinouts and Packaging

64 MAP BGA	64 LQFP	48 QFN	36 WLC SP	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
E8	38	30	—	—	PTB3	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	TPM2_CH1				
E6	39	31	—	—	PTB16	DISABLED		PTB16	SPI1_MOSI	LPUART0_RX	TPM_CLKIN0	SPI1_MISO		
D7	40	32	—	—	PTB17	DISABLED		PTB17	SPI1_MISO	LPUART0_TX	TPM_CLKIN1	SPI1_MOSI		
D6	41	—	—	—	PTB18	DISABLED		PTB18		TPM2_CH0	I2S0_TX_BCLK			
C7	42	—	—	—	PTB19	DISABLED		PTB19		TPM2_CH1	I2S0_TX_FS			
D8	43	33	—	—	PTC0	ADC0_SE14	ADC0_SE14	PTC0		EXTRG_IN	audioUSB_SOF_OUT	CMP0_OUT	I2S0_TXD0	
C6	44	34	B1	22	PTC1/ LLWU_P6/ RTC_CLKIN	ADC0_SE15	ADC0_SE15	PTC1/ LLWU_P6/ RTC_CLKIN	I2C1_SCL		TPM0_CH0		I2S0_TXD0	
B7	45	35	B2	23	PTC2	ADC0_SE11	ADC0_SE11	PTC2	I2C1_SDA		TPM0_CH1		I2S0_TX_FS	
C8	46	36	A1	24	PTC3/ LLWU_P7	DISABLED		PTC3/ LLWU_P7	SPI1_SCK	LPUART1_RX	TPM0_CH2	CLKOUT	I2S0_TX_BCLK	
E3	47	—	C4	—	VSS	VSS	VSS							
E4	48	—	B3	—	VDD	VDD	VDD							
B8	49	37	A2	25	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	LPUART1_TX	TPM0_CH3	I2S0_MCLK		
A8	50	38	A3	26	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0		CMP0_OUT	
A7	51	39	B4	27	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_MOSI	EXTRG_IN	I2S0_RX_BCLK	SPI0_MISO	I2S0_MCLK	
B6	52	40	A4	28	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_MISO	audioUSB_SOF_OUT	I2S0_RX_FS	SPI0_MOSI		
A6	53	—	—	—	PTC8	CMP0_IN2	CMP0_IN2	PTC8	I2C0_SCL	TPM0_CH4	I2S0_MCLK			
B5	54	—	—	—	PTC9	CMP0_IN3	CMP0_IN3	PTC9	I2C0_SDA	TPM0_CH5	I2S0_RX_BCLK			
B4	55	—	—	—	PTC10	DISABLED		PTC10	I2C1_SCL		I2S0_RX_FS			
A5	56	—	—	—	PTC11	DISABLED		PTC11	I2C1_SDA		I2S0_RXD0			
C3	57	41	—	—	PTD0	DISABLED		PTD0	SPI0_PCS0		TPM0_CH0		FXIO0_D0	
A4	58	42	—	—	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1		FXIO0_D1	
C2	59	43	—	—	PTD2	DISABLED		PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO	FXIO0_D2	
B3	60	44	—	—	PTD3	DISABLED		PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI	FXIO0_D3	
A3	61	45	A5	29	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI1_PCS0	UART2_RX	TPM0_CH4		FXIO0_D4	
C1	62	46	B5	30	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5		FXIO0_D5	
B2	63	47	A6	31	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI1_MOSI	LPUART0_RX		SPI1_MISO	FXIO0_D6	

Pinouts and Packaging

	1	2	3	4	5	6	
A	PTC3	PTC4	PTC5	PTC7	PTD4	PTD6	A
B	PTC1	PTC2	VDD	PTC6	PTD5	PTD7	B
C	PTB1	PTB0	PTA16	VSS	Reserved	Reserved	C
D	PTA20	PTA17	PTA15	PTA2	Reserved	Reserved	D
E	PTA19	VDD	PTA14	PTA1	PTE30	VDDA/ VREFH	E
F	PTA18	VSS	PTA4	PTA3	PTA0	VSSA/ VREFL	F
	1	2	3	4	5	6	

Figure 24. 36 WLCSP Pinout diagram

Figure below shows the 48 QFN pinouts:

MKL17Z256VMP4

8 Terminology and guidelines

8.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	<p>A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:</p> <ul style="list-style-type: none">• <i>Operating ratings</i> apply during operation of the chip.• <i>Handling ratings</i> apply when the chip is not powered. <p>NOTE: The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.</p>
Operating requirement	<p>A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip</p>
Operating behavior	<p>A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions</p>
Typical value	<p>A specified value for a technical characteristic that:</p> <ul style="list-style-type: none">• Lies within the range of values specified by the operating behavior• Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions <p>NOTE: Typical values are provided as design guidelines and are neither tested nor guaranteed.</p>