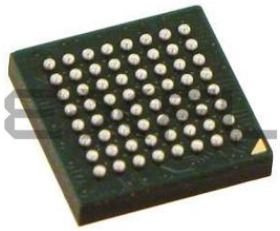

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 20x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA
Supplier Device Package	64-MAPBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl17z256vmp4r

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range: –40 to 85 °C for WLCSP package and –40 to 105 °C for other packages

Packages

- 64 LQFP 10mm x 10mm, 0.5mm pitch, 1.6mm thickness
- 64 MAPBGA 5mm x 5mm, 0.5mm pitch, 1.23mm thickness
- 48 QFN 7mm x 7mm, 0.5mm pitch, 0.65mm thickness
- 32 QFN 5mm x 5mm, 0.5mm pitch, 0.65mm thickness
- 36 WLCSP 2.8mm x 2.7mm, 0.4mm pitch, 0.6mm thickness

Security and Integrity

- 80-bit unique identification number per chip
- Advanced flash security

I/O

- Up to 54 general-purpose input/output pins (GPIO) and 6 high-drive pad

Low Power

- Down to 54uA/MHz in very low power run mode
- Down to 1.96uA in VLLS3 mode (RAM + RTC retained)
- Six flexible static modes

Ordering Information

Product		Memory		Package		IO and ADC channel		
Part number	Marking (Line1/ Line2)	Flash (KB)	SRAM (KB)	Pin count	Package	GPIOs	GPIOs (INT/HD)[1]	ADC channels (SE/DP)
MKL17Z128VFM4	M17P7V	128	32	32	QFN	28	19/6	11/2
MKL17Z256VFM4	M17P8V	256	32	32	QFN	28	19/6	11/2
MKL17Z128VFT4	M17P7V	128	32	48	QFN	40	24/6	18/3
MKL17Z256VFT4	M17P8V	256	32	48	QFN	40	24/6	18/3
MKL17Z128VLH4	MKL17Z128V//LH4	128	32	64	LQFP	54	31/6	20/4
MKL17Z256VLH4	MKL17Z256V//LH4	256	32	64	LQFP	54	31/6	20/4
MKL17Z128VMP4	M17P7V	128	32	64	MAPBGA	54	31/6	20/4
MKL17Z256VMP4	M17P8V	256	32	64	MAPBGA	54	31/6	20/4
MKL17Z256CAL4R	MKL17Z256CAL4	256	32	36	WLCSP	26	23/6	7/0

1. INT: interrupt pin numbers; HD: high drive pin numbers

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KL1XPB[1]
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL17P64M48SF6RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_L_1N71K[1]

Table continues on the next page...

Table of Contents

1.4 Voltage and current operating ratings

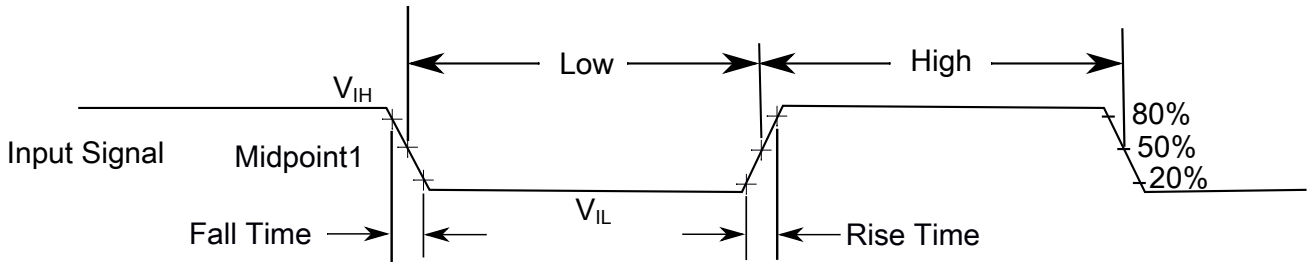
Table 4. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is V_{IL} + (V_{IH} - V_{IL}) / 2

Figure 1. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L=30 pF loads
- Slew rate disabled
- Normal drive strength

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 5. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICIO}	IO pin negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-3	—	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins • Negative current injection	 -25	 —	 mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

1. All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than V_{IO_MIN} (= V_{SS}-0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|.
2. Open drain outputs must be pulled to V_{DD}.

2.2.2 LVD and POR operating requirements

Table 6. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	—
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	—
	Low-voltage warning thresholds — high range					1

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 50 °C	—	10.26	17.62		
	• at 85 °C	—	33.49	60.19	µA	
	• at 105 °C	—	102.92	162.20		
I_{DD_LLS}	Low-leakage stop mode current, all peripheral disable, at 3.0 V				µA	
	• at 25 °C and below	—	2.06	3.33		
	• at 50 °C	—	4.72	6.85		
	• at 70 °C	—	8.13	13.30		
	• at 85 °C	—	13.34	24.70		
	• at 105 °C	—	41.08	52.43		
I_{DD_LLS}	Low-leakage stop mode current with RTC current, at 3.0 V				µA	
	• at 25 °C and below	—	2.46	3.73		
	• at 50 °C	—	5.12	7.25		
	• at 70 °C	—	8.53	11.78		
	• at 85 °C	—	13.74	18.91		
	• at 105 °C	—	41.48	52.83		
I_{DD_LLS}	Low-leakage stop mode current with RTC current, at 1.8 V				µA	3
	• at 25 °C and below	—	2.35	2.70		
	• at 50 °C	—	4.91	6.75		
	• at 70 °C	—	8.32	11.78		
	• at 85 °C	—	13.44	18.21		
	• at 105 °C	—	40.47	51.85		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V				µA	
	• at 25 °C and below	—	1.45	1.85		
	• at 50 °C	—	3.37	4.39		
	• at 70 °C	—	5.76	8.48		
	• at 85 °C	—	9.72	14.30		
	• at 105 °C	—	30.41	37.50		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V				µA	3
	• at 25 °C and below	—	2.05	2.45		
	• at 50 °C	—	3.97	4.99		
	• at 70 °C	—	6.36	9.08		
	• at 85 °C	—	10.32	14.73		
	• at 105 °C	—	31.01	38.10		

Table continues on the next page...

of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = IRC48M, f_{SYS} = 48 MHz, f_{BUS} = 24 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

2.2.8 Capacitance attributes

Table 12. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN}	Input capacitance	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 13. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
f_{SYS}	System and core clock[1]	—	48	MHz
f_{BUS}	Bus clock[1]	—	24	MHz
f_{FLASH}	Flash clock[1]	—	24	MHz
f_{LPTMR}	LPTMR clock	—	24	MHz
VLPR and VLPS modes[2]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	1	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{LPTMR}	LPTMR clock[3]	—	24	MHz

Table continues on the next page...

3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.
5. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

Table 18. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

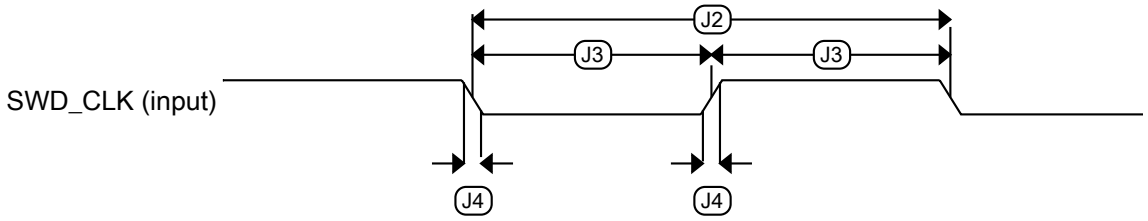


Figure 4. Serial wire clock input timing

3.6.2 Voltage reference electrical specifications

Table 29. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage		3.6	V	
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 30 is tested under the condition of setting VREF_TRM[CHOPEN], VREF_SC[REGEN] and VREF_SC[ICOMPEN] bits to 1.

Table 30. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	1
V_{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	1
V_{out}	Voltage reference output — user trim	1.193	—	1.197	V	1
V_{step}	Voltage reference trim step	—	0.5	—	mV	1
V_{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range: 0 to 70°C)	—	—	50	mV	1
I_{bg}	Bandgap only current	—	—	80	µA	1
I_{lp}	Low-power buffer current	—	—	360	uA	1
I_{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	— —	 200	 —	µV	1, 2
T_{stup}	Buffer startup time	—	—	100	µs	
$T_{chop\_osc\_stup}$	Internal bandgap start-up delay with chop oscillator enabled	—	—	35	ms	—
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 31. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	°C	

Table 32. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	

3.6.3 CMP and 6-bit DAC electrical specifications

Table 33. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

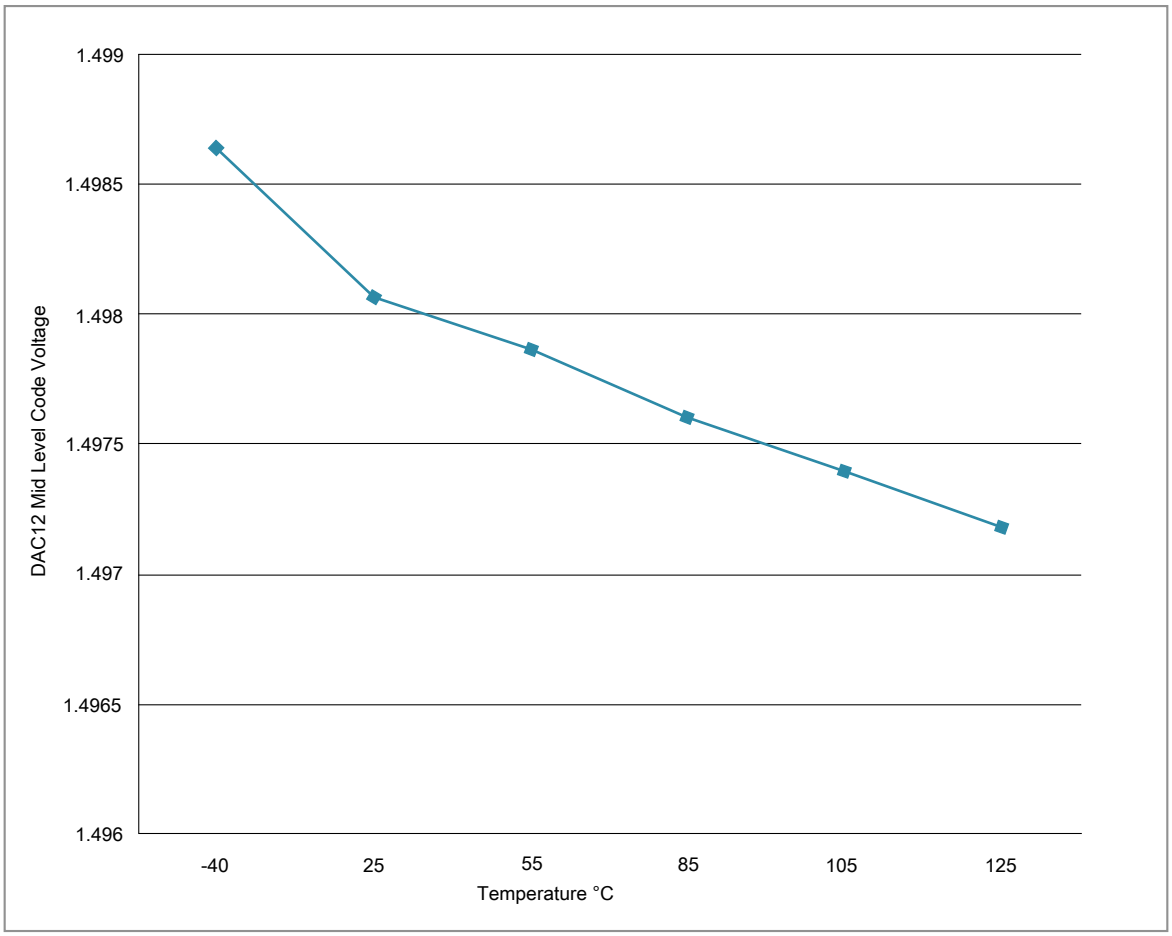


Figure 13. Offset at half scale vs. temperature

3.7 Timers

See General switching specifications.

3.8 Communication interfaces

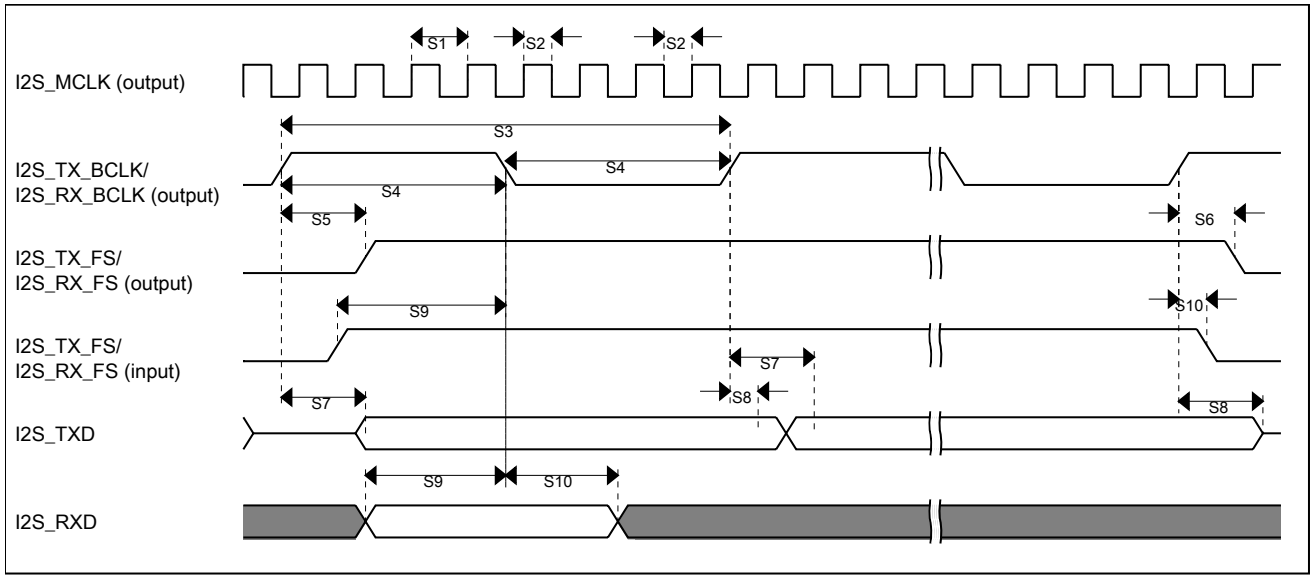


Figure 19. I2S/SAI timing — master modes

Table 43. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	33	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	28	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

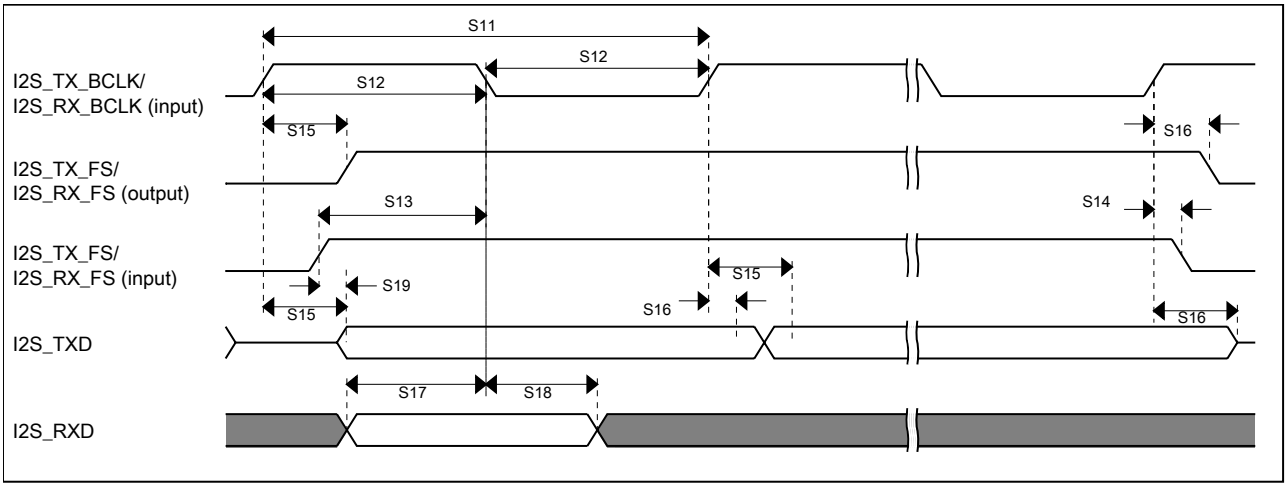


Figure 20. I2S/SAI timing — slave modes

3.8.4.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 44. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK		—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

64 MAP BGA	64 LQFP	48 QFN	36 WLCSP	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
A2	64	48	B6	32	PTD7	DISABLED		PTD7	SPI1_MISO	LPUART0_TX		SPI1_MOSI	FXIO0_D7	
C5	—	—	C5	—	Reserved	Reserved	Reserved							
—	—	—	C6	—	Reserved	Reserved	Reserved							
—	—	—	D5	—	Reserved	Reserved	Reserved							
—	—	—	D6	—	Reserved	Reserved	Reserved							

5.2 KL17 Family Pinouts

Figure below shows the 32 QFN pinouts:

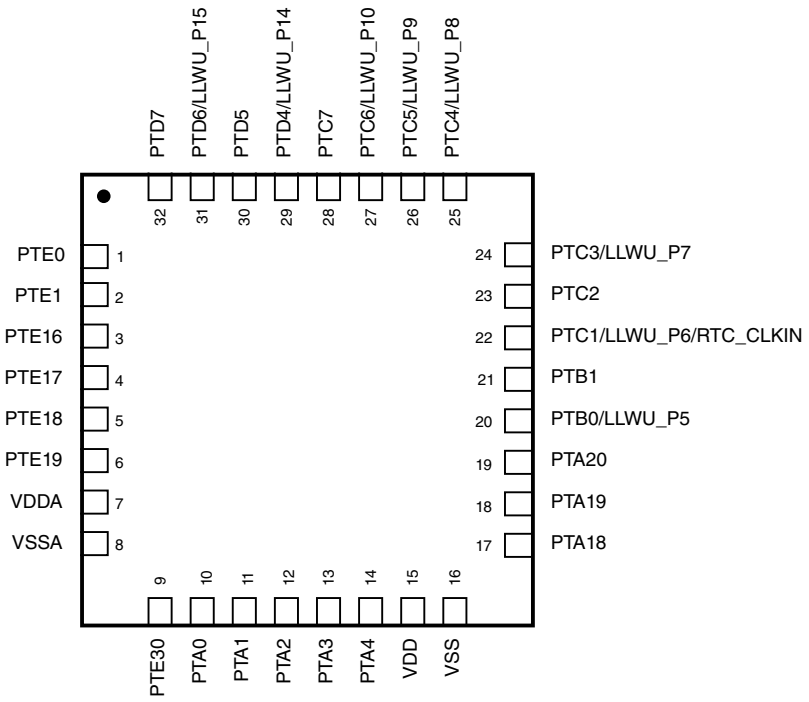
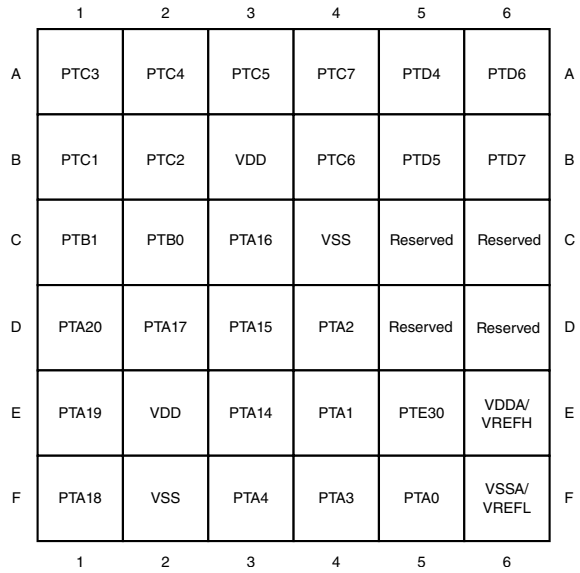


Figure 23. 32 QFN Pinout diagram

Figure below shows the 36 WLCSP pinouts:



	1	2	3	4	5	6	
A	PTC3	PTC4	PTC5	PTC7	PTD4	PTD6	A
B	PTC1	PTC2	VDD	PTC6	PTD5	PTD7	B
C	PTB1	PTB0	PTA16	VSS	Reserved	Reserved	C
D	PTA20	PTA17	PTA15	PTA2	Reserved	Reserved	D
E	PTA19	VDD	PTA14	PTA1	PTE30	VDDA/ VREFH	E
F	PTA18	VSS	PTA4	PTA3	PTA0	VSSA/ VREFL	F
	1	2	3	4	5	6	

Figure 24. 36 WLCSP Pinout diagram

Figure below shows the 48 QFN pinouts:

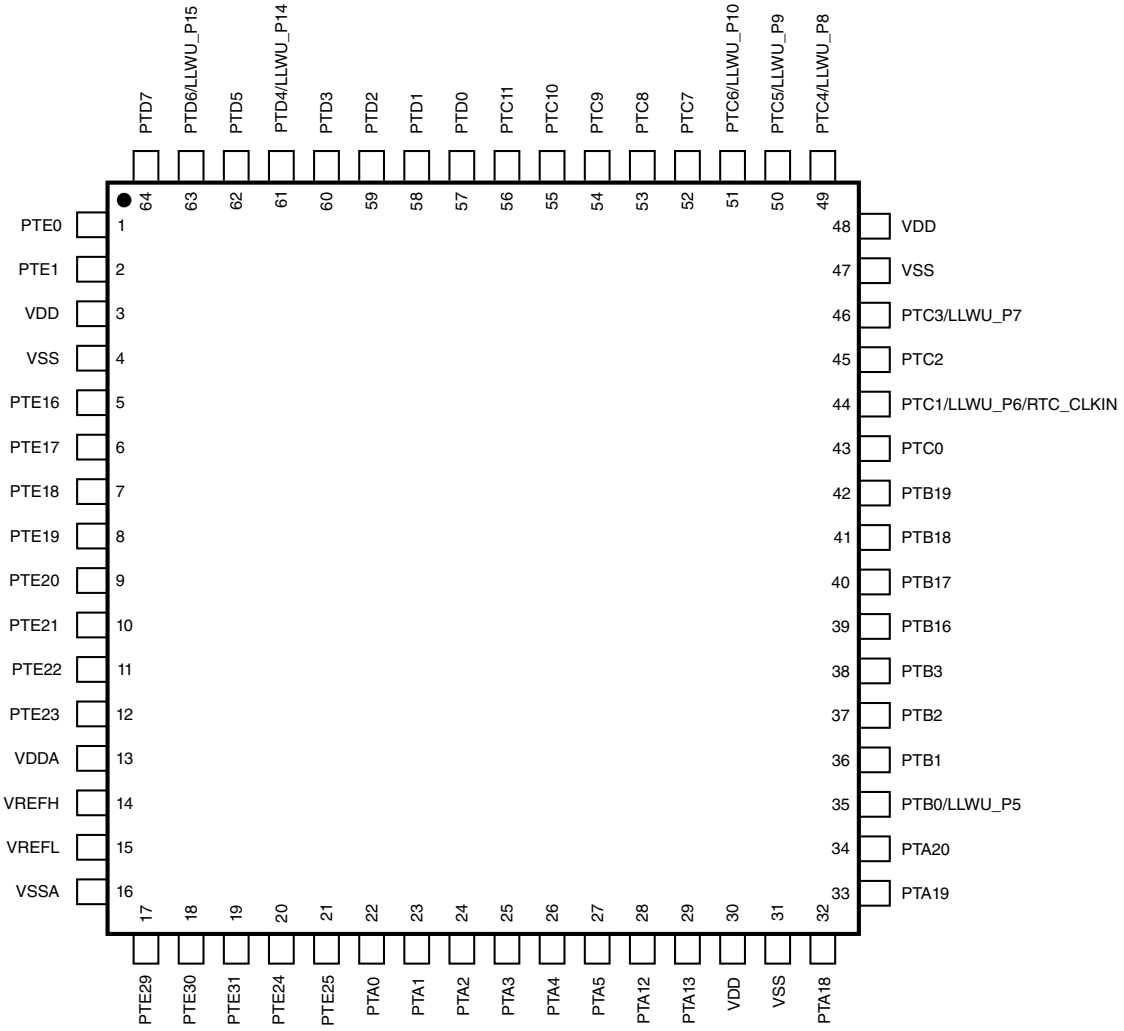


Figure 27. 64 LQFP Pinout diagram

5.3 Recommended connection for unused analog and digital pins

Table 46 shows the recommended connections for analog interface pins if those analog interfaces are not used in the customer's application

Table 46. Recommended connection for unused analog interfaces

Pin Type	KL17	Short recommendation	Detailed recommendation
GPIO/Analog	PTA18/EXTAL0	Float	Analog input - Float
GPIO/Analog	PTA19/XTAL0	Float	Analog output - Float
GPIO/Analog	PTx/DAC0_OUT	Float	Float (default is analog input)
GPIO/Analog	PTx/ADCx	Float	Float (default is analog input)
GPIO/Analog	PTx/CMPx	Float	Float (default is analog input)
GPIO/Digital	PTA0/SWD_CLK	Float	Float (default is SWD with pulldown)
GPIO/Digital	PTA3/SWD_DIO	Float	Float (default is SWD with pullup)
GPIO/Digital	PTA4/NMI_b	10 kΩ pullup or disabled and float	Pull high or disable in PCR & FOPT and float
GPIO/Digital	PTx	Float	Float (default is disabled)
VDDA	VDDA	Always connect to VDD potential	Always connect to VDD potential
VREFH	VREFH	Always connect to VDD potential	Always connect to VDD potential
VREFL	VREFL	Always connect to VSS potential	Always connect to VSS potential
VSSA	VSSA	Always connect to VSS potential	Always connect to VSS potential
Reserved	Reserved	Tie to ground through 10 kΩ	Tie to ground through 10 kΩ

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the Web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers:

7 Part identification

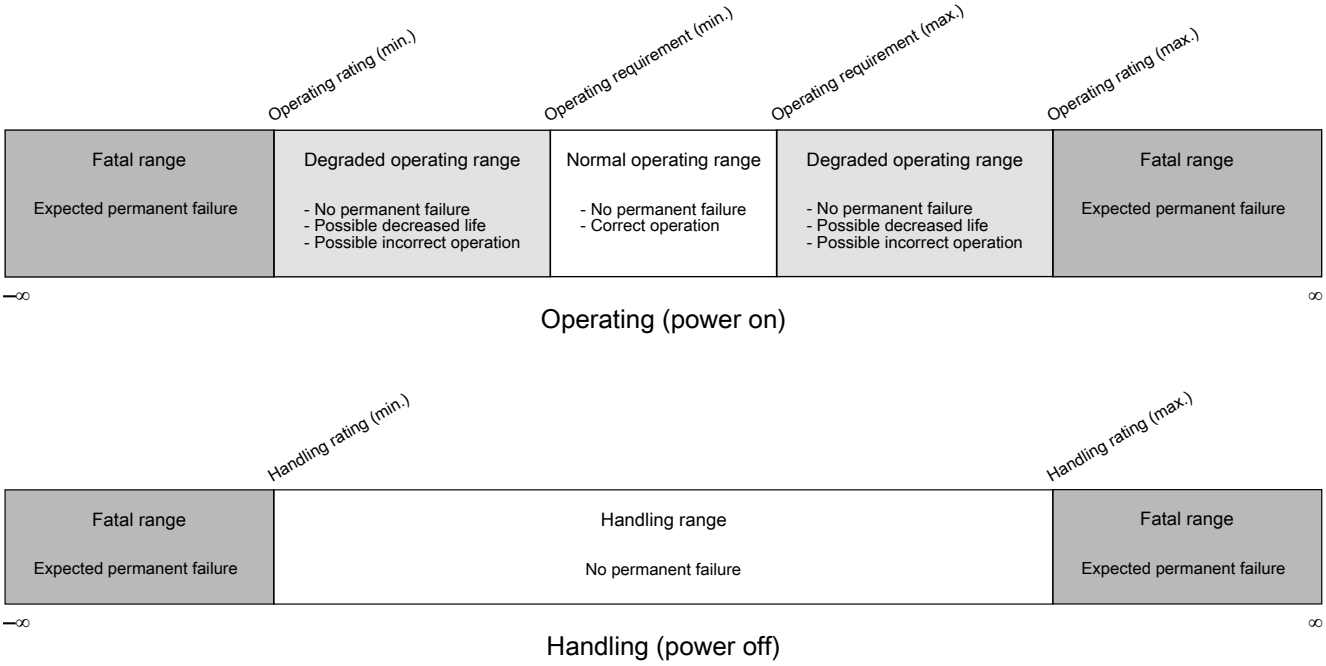
8 Terminology and guidelines

8.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. **NOTE:** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions **NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed.

8.4 Relationship between ratings and operating requirements



8.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

9 Revision History

The following table provides a revision history for this document.

Table 48. Revision History

Rev. No.	Date	Substantial Changes
3	09 August 2014	Initial Public release • Updated Table 9 - Power consumption operating behaviors. • Added a note related to 32 QFN pin package in Pinouts topic.
4	03 March 2015	• Updated the features and completed the ordering information. • Removed thickness dimension from package diagrams.

Table continues on the next page...

Table 48. Revision History (continued)

Rev. No.	Date	Substantial Changes

		• Updated Related Resources table to include Chip Errata resource name and Package Drawing part numbers in the respective rows. Also updated Product Brief resource references.
		• Updated Table 7. Voltage and current operating behaviors.
		  • Specified correct max. value for I_{IN}.
		• Updated Table - 9 Power consumption operating behaviors.
		  • Rows added for IDD for reset pin hold low ($I_{DD\_RESET\_LOW}$) at 1.7V and 3V.
		  • Measurement unit updated for I_{DD_VLLS1} from nA to µA.
		  • Footnote 1 was moved in the beginning of the table as text.
		• Added Table - 11 EMC radiated emissions operating behaviors for 64-pin LQFP package under section 2.2.6.
		• Updated Table - 18 (IRC48M specification) and Table - 19 (IRC8M/2M specification) under section 3.3.1 - 'MCG-Lite specifications'.
		  • Removed supply voltage (V_{DD}), temperature range (T), untrimmed (f_{IRC_UT}), trim function (Δf_{IRC_C}, Δf_{IRC_F}) data from Table - 18 (IRC48M specification).
		  • Removed supply voltage (V_{DD}), temperature range (T) data from Table - 19 (IRC8M/2M specification).
		• Added Figure 6. IRC8M Frequency Drift vs Temperature curve after Table - 19 (IRC8M/2M specification).
		• Updated Table 29. VREF full-range operating behaviors.
		  • Removed A_c(Aging coefficient) row.
		  • Added $T_{chop\_osc\_stup}$ parameter.
		• Added tables: "I2C timing" and "I2C 1Mbit/s timing" under section - I^2C.
		• Added VREF specifications (V_{REFH} and V_{REFL}) to Table 26. 16-bit ADC operating conditions.
		• Removed note: “This device does not have the USB_CLKIN signal available.”

5	12 August 2015	• In Table 9. Power consumption operating behaviors:
		  • Updated Max. values of I_{DD_WAIT}, I_{DD_VLPW}, I_{DD_STOP}, I_{DD_VLPS}, I_{DD_LLS}, I_{DD_VLLS3}, I_{DD_VLLS1}, I_{DD_VLLS0}.
		  • Modified unit of I_{DD_VLLS0} from nA to µA.
		  • Removed $I_{DD\_RESET\_LOW}$ information.
		• In Table 13. Device clock specifications, added a footnote for normal run mode.
		• In Table 15. Thermal operating requirements, modified the footnote for Ambient temperature.
		• In Table 18. IRC48M specification, removed f_{IRC_T} data and added $\Delta f_{irc48m\_of\_lv}$ and $\Delta f_{irc48m\_of\_hv}$ specifications.
		• In Table 26. 16-bit ADC operating conditions, updated Max. value of f_{ADCK} and C_{rate}.

5.1	16 Nov 2015	• Added 36-pin WLCSP package information.
6	25 Jan 2016	• Completed all the TBDs of the 36-pin WLCSP package.

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