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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	196
Number of Logic Elements/Cells	466
Total RAM Bits	6272
Number of I/O	61
Number of Gates	5000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc4005l-5pc84c

Table 1: XC4000-Series Field Programmable Gate Arrays

Device	Max Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total Logic Blocks	Number of Flip-Flops	Max. Decode Inputs per side	Max. User I/O
XC4003E	3,000	3,200	2,000 - 5,000	10 x 10	100	360	30	80
XC4005E/L	5,000	6,272	3,000 - 9,000	14 x 14	196	616	42	112
XC4006E	6,000	8,192	4,000 - 12,000	16 x 16	256	768	48	128
XC4008E	8,000	10,368	6,000 - 15,000	18 x 18	324	936	54	144
XC4010E/L	10,000	12,800	7,000 - 20,000	20 x 20	400	1,120	60	160
XC4013E/L	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	72	192
XC4020E	20,000	25,088	13,000 - 40,000	28 x 28	784	2,016	84	224
XC4025E	25,000	32,768	15,000 - 45,000	32 x 32	1,024	2,560	96	256
XC4028EX/XL	28,000	32,768	18,000 - 50,000	32 x 32	1,024	2,560	96	256
XC4036EX/XL	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	108	288
XC4044EX/XL	44,000	51,200	27,000 - 80,000	40 x 40	1,600	3,840	120	320
XC4052XL	52,000	61,952	33,000 - 100,000	44 x 44	1,936	4,576	132	352
XC4062XL	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	144	384
	Larger Devices Available in the First Half of 1997							

* Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

Note: *Throughout the functional descriptions in this document, references to the XC4000E device family include the XC4000L, and references to the XC4000EX device family include the XC4000XL, unless explicitly stated otherwise. References to the XC4000 Series include the XC4000E, XC4000EX, XC4000L, and XC4000XL families. All functionality in low-voltage families is the same as in the corresponding 5-Volt family, except where numerical references are made to timing, power, or current-sinking capability.*

Description

XC4000-Series devices are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs). They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal memory cells. The FPGA can either actively read its configuration data from an external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA from an external device (slave, peripheral and Express modes).

XC4000-Series FPGAs are supported by powerful and sophisticated software, covering every aspect of design from schematic or behavioral entry, floorplanning, simulation, automatic block placement and routing of interconnects, to the creation, downloading, and readback of the configuration bit stream.

Because Xilinx FPGAs can be reprogrammed an unlimited number of times, they can be used in innovative designs where hardware is changed dynamically, or where hardware must be adapted to different user applications. FPGAs are ideal for shortening design and development cycles, and also offer a cost-effective solution for production rates well beyond 5,000 systems per month. For lowest high-volume unit cost, a design can first be implemented in the XC4000E or XC4000EX, then migrated to one of Xilinx' compatible HardWire mask-programmed devices.

Table 2 shows density and performance for a few common circuit functions that can be implemented in XC4000-Series devices.

Table 3: CLB Count of Selected XC4000-Series Soft Macros

7400 Equivalents	CLBs
‘138	5
‘139	2
‘147	5
‘148	6
‘150	5
‘151	3
‘152	3
‘153	2
‘154	16
‘157	2
‘158	2
‘160	5
‘161	6
‘162	8
‘163	8
‘164	4
‘165s	9
‘166	5
‘168	7
‘174	3
‘194	5
‘195	3
‘280	3
‘283	8
‘298	2
‘352	2
‘390	3
‘518	3
‘521	3
Explanation of RAM nomenclature	
s = single-port edge-triggered	
d = dual-port edge-triggered	
no extension = level-sensitive	

Barrel Shifters	CLBs
brlshft4	4
brlshft8	13
4-Bit Counters	
cd4cd	3
cd4cle	5
cd4rle	6
cb4ce	3
cb4cle	6
cb4re	5
8- and 16-Bit Counters	
cb8ce	6
cb8re	10
cc16ce	9
cc16cle	9
cc16cled	21
Identity Comparators	
comp4	1
comp8	2
comp16	5
Magnitude Comparators	
compm4	4
compm8	9
compm16	20
RAMs	
ram16x4	2
ram16x4s	2
ram16x4d	4

Multiplexers	CLBs
m2-1e	1
m4-1e	1
m8-1e	3
m16-1e	5
Registers	
rd4r	2
rd8r	4
rd16r	8
Shift Registers	
sr8ce	4
sr16re	8
Decoders	
d2-4e	2
d3-8e	4
d4-16e	16

Explanation of counter nomenclature
- cb = binary counter
- cd = BCD counter
- cc = cascadable binary counter
- d = bidirectional
- l = loadable
- e = clock enable
- r = synchronous reset
- c = asynchronous clear

Clock Enable

The clock enable signal (EC) is active High. The EC pin is shared by both storage elements. If left unconnected for either, the clock enable for that storage element defaults to the active state. EC is not invertible within the CLB.

Set/Reset

An asynchronous storage element input (SR) can be configured as either set or reset. This configuration option determines the state in which each flip-flop becomes operational after configuration. It also determines the effect of a Global Set/Reset pulse during normal operation, and the effect of a pulse on the SR pin of the CLB. All three set/reset functions for any single flip-flop are controlled by the same configuration data bit.

The set/reset state can be independently specified for each flip-flop. This input can also be independently disabled for either flip-flop.

The set/reset state is specified by using the INIT attribute, or by placing the appropriate set or reset flip-flop library symbol.

SR is active High. It is not invertible within the CLB.

Global Set/Reset

A separate Global Set/Reset line (not shown in Figure 1) sets or clears each storage element during power-up, reconfiguration, or when a dedicated Reset net is driven active. This global net (GSR) does not compete with other routing resources; it uses a dedicated distribution network.

Each flip-flop is configured as either globally set or reset in the same way that the local set/reset (SR) is specified. Therefore, if a flip-flop is set by SR, it is also set by GSR. Similarly, a reset flip-flop is reset by both SR and GSR.

GSR can be driven from any user-programmable pin as a global reset input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GSR pin of the STARTUP symbol. (See Figure 2.) A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global Set/Reset signal.

Alternatively, GSR can be driven from any internal node.

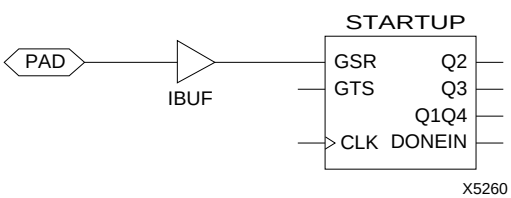


Figure 2: Schematic Symbols for Global Set/Reset

Data Inputs and Outputs

The source of a storage element data input is programmable. It is driven by any of the functions F', G', and H', or by the Direct In (DIN) block input. The flip-flops or latches drive the XQ and YQ CLB outputs.

Two fast feed-through paths are available, as shown in Figure 1. A two-to-one multiplexer on each of the XQ and YQ outputs selects between a storage element output and any of the control inputs. This bypass is sometimes used by the automated router to repower internal signals.

Control Signals

Multiplexers in the CLB map the four control inputs (C1 - C4 in Figure 1) into the four internal control signals (H1, DIN/H2, SR/H0, and EC). Any of these inputs can drive any of the four internal control signals.

When the logic function is enabled, the four inputs are:

- EC — Enable Clock
- SR/H0 — Asynchronous Set/Reset or H function generator Input 0
- DIN/H2 — Direct In or H function generator Input 2
- H1 — H function generator Input 1.

When the memory function is enabled, the four inputs are:

- EC — Enable Clock
- WE — Write Enable
- D0 — Data Input to F and/or G function generator
- D1 — Data input to G function generator (16x1 and 16x2 modes) or 5th Address bit (32x1 mode).

Using FPGA Flip-Flops and Latches

The abundance of flip-flops in the XC4000 Series invites pipelined designs. This is a powerful way of increasing performance by breaking the function into smaller subfunctions and executing them in parallel, passing on the results through pipeline flip-flops. This method should be seriously considered wherever throughput is more important than latency.

To include a CLB flip-flop, place the appropriate library symbol. For example, FDCE is a D-type flip-flop with clock enable and asynchronous clear. The corresponding latch symbol (for the XC4000EX only) is called LDCE.

In XC4000-Series devices, the flip flops can be used as registers or shift registers without blocking the function generators from performing a different, perhaps unrelated task. This ability increases the functional capacity of the devices.

The CLB setup time is specified between the function generator inputs and the clock input K. Therefore, the specified CLB flip-flop setup time includes the delay through the function generator.

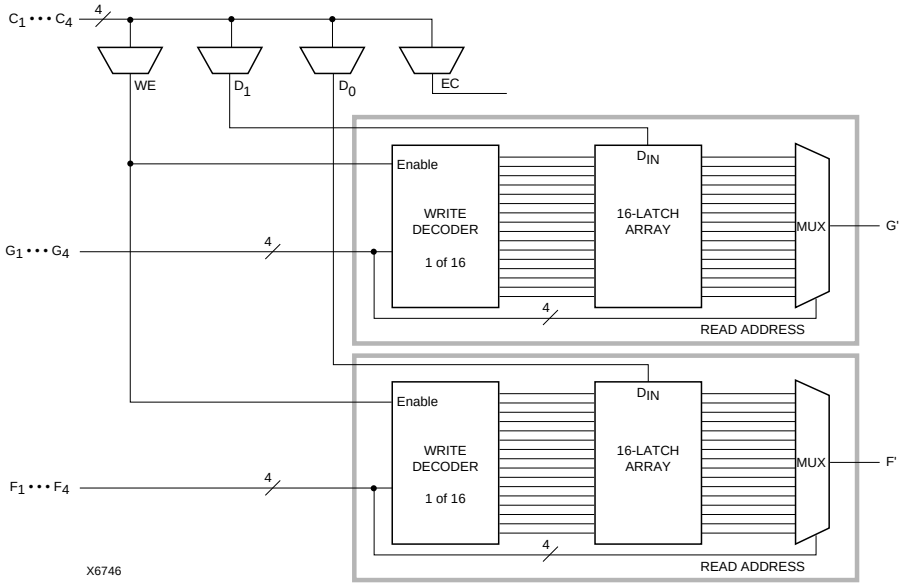


Figure 9: 16x2 (or 16x1) Level-Sensitive Single-Port RAM

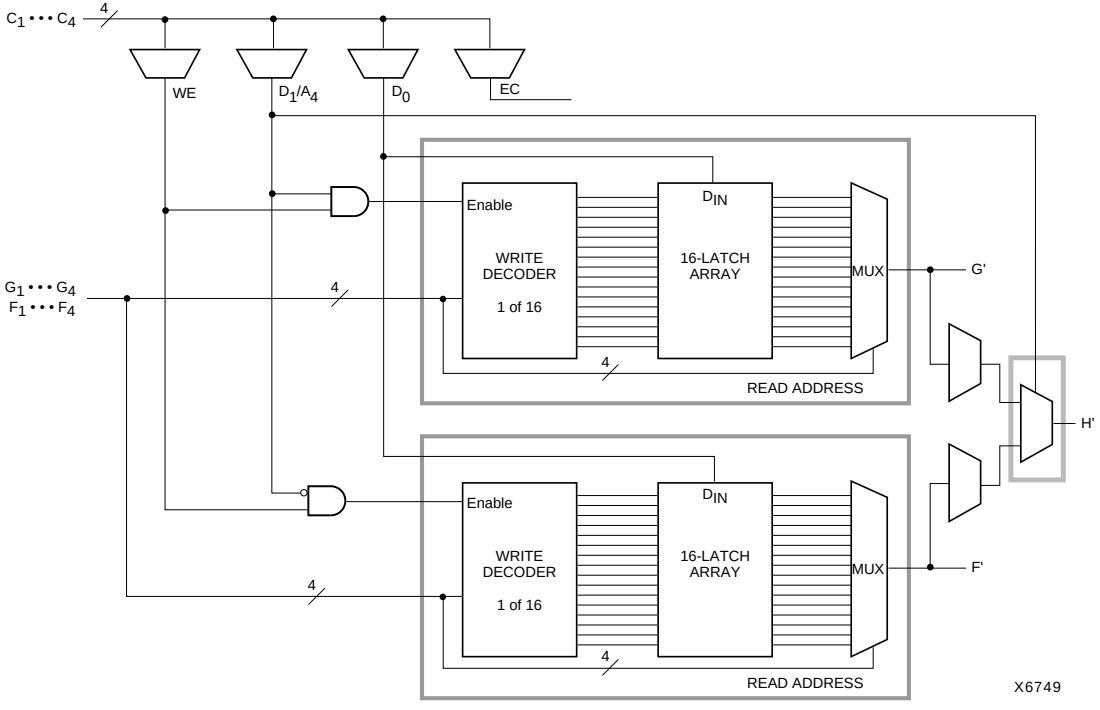


Figure 10: 32x1 Level-Sensitive Single-Port RAM (F and G addresses are identical)

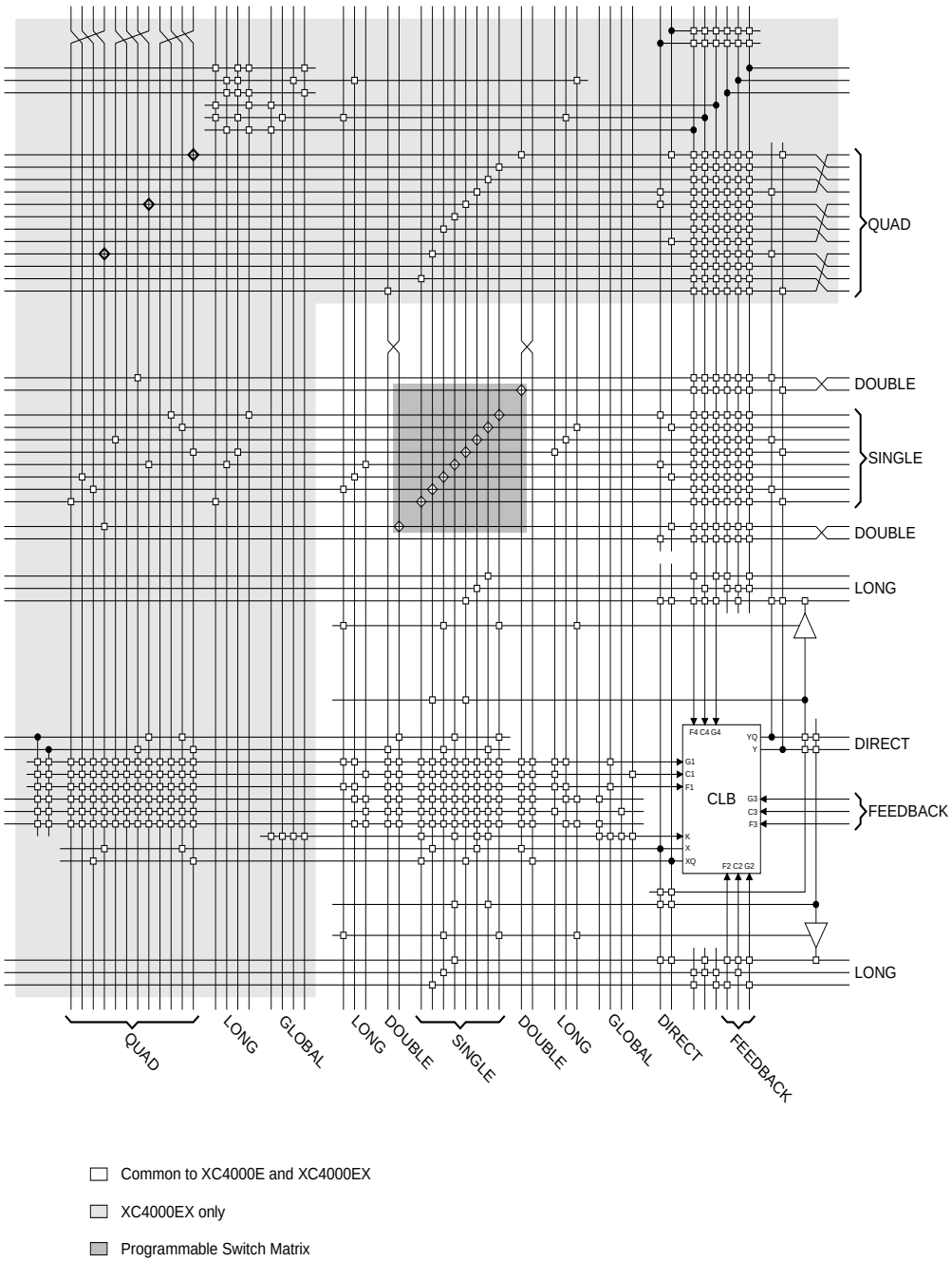


Figure 27: Detail of Programmable Interconnect Associated with XC4000-Series CLB

Global Nets and Buffers (XC4000EX only)

Eight vertical longlines in each CLB column are driven by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. The global lines are broken in the center of the array, to allow faster distribution and to minimize skew across the whole array. Each half-column global line has its own buffered multiplexer, as shown in Figure 36. The top and bottom global lines cannot be connected across the center of the device, as this connection might introduce unacceptable skew. The top and bottom halves of the global lines must be separately driven — although they can be driven by the same global buffer.

The eight global lines in each CLB column can be driven by either of two types of global buffers. They can also be driven by internal logic, because they can be accessed by single, double, and quad lines at the top, bottom, half, and quarter points. Consequently, the number of different clocks that can be used simultaneously in an XC4000EX device is very large.

There are four global lines feeding the IOBs at the left edge of the device. IOBs along the right edge have eight global lines. There is a single global line along the top and bottom edges with access to the IOBs. All IOB global lines are broken at the center. They cannot be connected across the center of the device, as this connection might introduce unacceptable skew.

IOB global lines can be driven from any of three types of global buffers, or from local interconnect. Alternatively, top and bottom IOBs can be clocked from the global lines in the adjacent CLB column.

Three different types of clock buffers are available in the XC4000EX:

- Global Low-Skew Buffers (BUFGLS)
- Global Early Buffers (BUFGE)
- FastCLK Buffers (BUFFCLK)

Global Low-Skew Buffers are the standard clock buffers. They should be used for most internal clocking, whenever a large portion of the device must be driven.

Global Early Buffers are designed to provide a faster clock access, but CLB access is limited to one-fourth of the device. They also facilitate a faster I/O interface.

FastCLK buffers are specifically designed to provide the fastest possible I/O clock. They have only the standard input access to CLBs, through local interconnect.

Figure 36 is a conceptual diagram of the global net structure in the XC4000EX.

Global Early buffers and Global Low-Skew buffers share a single pad. Therefore, the same IPAD symbol can drive one buffer of each type, in parallel. This configuration is particularly useful when using the Fast Capture latches, as described in "IOB Input Signals" on page 24. Paired Global Early and Global Low-Skew buffers share a common input; they cannot be driven by two different signals.

Choosing an XC4000EX Clock Buffer

The clocking structure of the XC4000EX provides a large variety of features. However, it can be simple to use, without understanding all the details. The software automatically handles clocks, along with all other routing, when the appropriate clock buffer is placed in the design. In fact, if a buffer symbol called BUFG is placed, rather than a specific type of buffer, the software even chooses the buffer most appropriate for the design. The detailed information in this section is provided for those users who want a finer level of control over their designs.

If fine control is desired, use the following summary and Table 17 on page 41 to choose an appropriate clock buffer.

- The simplest thing to do is to use a Global Low-Skew buffer.
- If a faster clock path is needed, try a BUFG. The software will first try to use a Global Low-Skew Buffer. If timing requirements are not met, a faster buffer will automatically be used.
- If a single quadrant of the chip is sufficient for the clocked logic, and the timing requires a faster clock than the Global Low-Skew buffer, use a Global Early buffer.
- In special cases, where both external and internal timing have been carefully studied, a FastCLK buffer can be used, for the fastest possible I/O clock path.

Global Low-Skew Buffers

Each corner of the XC4000EX device has two Global Low-Skew buffers. Any of the eight Global Low-Skew buffers can drive any of the eight vertical Global lines in a column of CLBs. In addition, any of the buffers can drive any of the four vertical lines accessing the IOBs on the left edge of the device, and any of the eight vertical lines accessing the IOBs on the right edge of the device. (See Figure 37 on page 44.)

IOBs at the top and bottom edges of the device are accessed through the vertical Global lines in the CLB array, as in the XC4000E. Any Global Low-Skew buffer can, therefore, access every IOB and CLB in the device.

The Global Low-Skew buffers can be driven by either semi-dedicated pads or internal logic.

To use a Global Low-Skew buffer, place a BUFGLS element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=T attribute or property to direct that a BUFGLS be placed in one of the two Global Low-Skew buffers on the top edge of the device, or a LOC=TR to indicate the Global Low-Skew buffer on the top edge of the device, on the right.

Configuration

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. XC4000-Series devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The XACT*step* development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Special Purpose Pins

Three configuration mode pins (M2, M1, M0) are sampled prior to configuration to determine the configuration mode. After configuration, these pins can be used as auxiliary connections. M2 and M0 can be used as inputs, and M1 can be used as an output. The XACT*step* development system does not use these resources unless they are explicitly specified in the design entry. This is done by placing a special pad symbol called MD2, MD1, or MD0 instead of the input or output pad symbol.

In XC4000-Series devices, the mode pins have weak pull-up resistors during configuration. With all three mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the mode pins can be left unconnected. (Note, however, that the internal pull-up resistor value can be as high as 100 kΩ.) After configuration, these pins can individually have weak pull-up or pull-down resistors, as specified in the design. A pull-down resistor value of 4.7 kΩ is recommended.

These pins are located in the lower left chip corner and are near the readback nets. This location allows convenient routing if compatibility with the XC2000 and XC3000 family conventions of M0/RT, M1/RD is desired.

Configuration Modes

XC4000E devices have six configuration modes. XC4000EX devices have the same six modes, plus an additional configuration mode. These modes are selected by a 3-bit input code applied to the M2, M1, and M0 inputs. There are three self-loading Master modes, two Peripheral modes, and a Serial Slave mode, which is used primarily for daisy-chained devices. The seventh mode, called Express mode, is an additional slave mode that allows high-speed parallel configuration of the high-capacity XC4000EX devices. The coding for mode selection is shown in Table 20.

Table 20: Configuration Modes

Mode	M2	M1	M0	CCLK	Data
Master Serial	0	0	0	output	Bit-Serial
Slave Serial	1	1	1	input	Bit-Serial
Master Parallel Up	1	0	0	output	Byte-Wide, increment from 00000
Master Parallel Down	1	1	0	output	Byte-Wide, decrement from 3FFFF
Peripheral Synchronous*	0	1	1	input	Byte-Wide
Peripheral Asynchronous	1	0	1	output	Byte-Wide
Express (XC4000EX only)	0	1	0	input	Byte-Wide
Reserved	0	0	1	—	—

Note: * Peripheral Synchronous can be considered byte-wide Slave Parallel

A detailed description of each configuration mode, with timing information, is included later in this data sheet. During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during configuration are shown in Table 24 on page 78.

Master Modes

The three Master modes use an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices. They also generate address and timing for external PROM(s) containing the configuration data.

Master Parallel (Up or Down) modes generate the CCLK signal and PROM addresses and receive byte parallel data. The data is internally serialized into the FPGA data-frame format. The up and down selection generates starting addresses at either zero or 3FFFF, for compatibility with different microprocessor addressing conventions. The Master Serial mode generates CCLK and receives the configuration data in serial form from a Xilinx serial-configuration PROM.

CCLK speed is selectable as either 1 MHz (default) or 8 MHz (up to 10% lower for low-voltage devices). Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is -50% to +25%.

Peripheral Modes

The two Peripheral modes accept byte-wide data from a bus. A RDY/$\overline{\text{BUSY}}$ status is available as a handshake signal. In Asynchronous Peripheral mode, the internal oscillator generates a CCLK burst signal that serializes the byte-wide data. CCLK can also drive slave devices. In the syn-

The XC4000 Series offers another start-up clocking option, UCLK_NOSYNC. The three events described above need not be triggered by CCLK. They can, as a configuration option, be triggered by a user clock. This means that the device can wake up in synchronism with the user system.

When the UCLK_SYNC option is enabled, the user can externally hold the open-drain DONE output Low, and thus stall all further progress in the start-up sequence until DONE is released and has gone High. This option can be used to force synchronization of several FPGAs to a common user clock, or to guarantee that all devices are successfully configured before any I/Os go active.

If either of these two options is selected, and no user clock is specified in the design or attached to the device, the chip could reach a point where the configuration of the device is complete and the Done pin is asserted, but the outputs do not become active. The solution is either to recreate the bitstream specifying the start-up clock as CCLK, or to supply the appropriate user clock.

Start-up Sequence

The Start-up sequence begins when the configuration memory is full, and the total number of configuration clocks received since $\overline{\text{INIT}}$ went High equals the loaded value of the length count.

The next rising clock edge sets a flip-flop Q0, shown in Figure 50. Q0 is the leading bit of a 5-bit shift register. The outputs of this register can be programmed to control three events.

- The release of the open-drain DONE output
- The change of configuration-related pins to the user function, activating all IOBs.
- The termination of the global Set/Reset initialization of all CLB and IOB storage elements.

The DONE pin can also be wire-ANDed with DONE pins of other FPGAs or with other external signals, and can then be used as input to bit Q3 of the start-up register. This is called “Start-up Timing Synchronous to Done In” and is selected by the CCLK_SYNC and UCLK_SYNC MakeBits options.

When DONE is not used as an input, the operation is called “Start-up Timing Not Synchronous to DONE In,” and is selected by the CCLK_NOSYNC and UCLK_NOSYNC MakeBits options.

As a configuration option, the start-up control register beyond Q0 can be clocked either by subsequent CCLK pulses or from an on-chip user net called STARTUP.CLK. These signals can be accessed by placing the STARTUP library symbol.

Start-up from CCLK

If CCLK is used to drive the start-up, Q0 through Q3 provide the timing. Heavy lines in Figure 49 show the default timing, which is compatible with XC2000 and XC3000 devices using early DONE and late Reset. The thin lines indicate all other possible timing options.

Start-up from a User Clock (STARTUP.CLK)

When, instead of CCLK, a user-supplied start-up clock is selected, Q1 is used to bridge the unknown phase relationship between CCLK and the user clock. This arbitration causes an unavoidable one-cycle uncertainty in the timing of the rest of the start-up sequence.

DONE Goes High to Signal End of Configuration

In all configuration modes except Express mode, XC4000-Series devices read the expected length count from the bitstream and store it in an internal register. The length count varies according to the number of devices and the composition of the daisy chain. Each device also counts the number of CCLKs during configuration.

Two conditions have to be met in order for the DONE pin to go high:

- the chip's internal memory must be full, and
- the configuration length count must be met, *exactly.*

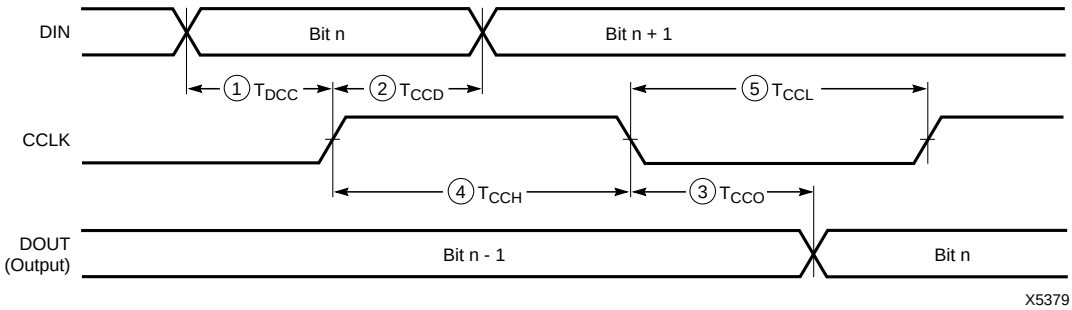
This is important because the counter that determines when the length count is met begins with the very first CCLK, not the first one after the preamble.

Therefore, if a stray bit is inserted before the preamble, or the data source is not ready at the time of the first CCLK, the internal counter that holds the number of CCLKs will be one ahead of the actual number of data bits read. At the end of configuration, the configuration memory will be full, but the number of bits in the internal counter will not match the expected length count.

As a consequence, a Master mode device will continue to send out CCLKs until the internal counter turns over to zero, and then reaches the correct length count a second time. This will take several seconds [$2^{24} * $ CCLK period] — which is sometimes interpreted as the device not configuring at all.

If it is not possible to have the data ready at the time of the first CCLK, the problem can be avoided by increasing the number in the length count by the appropriate value. The *XACT User Guide* includes detailed information about manually altering the length count.

In Express mode, there is no length count. The DONE pin for each device goes High when the device has received its quota of configuration data. Wiring the DONE pins of several devices together delays start-up of all devices until all are fully configured.



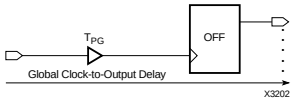
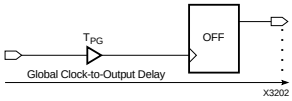
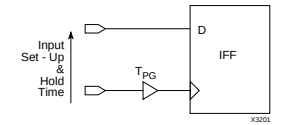
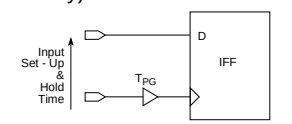
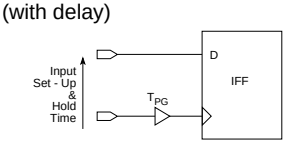
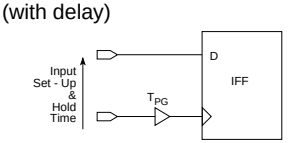
	Description	Symbol		Min	Max	Units
CCLK	DIN setup	1	T_{DCC}	20		ns
	DIN hold	2	T_{CCD}	0		ns
	DIN to DOUT	3	T_{CCO}		30	ns
	High time	4	T_{CCH}	45		ns
	Low time	5	T_{CCL}	45		ns
	Frequency		F_{CC}		10	MHz

Note: Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.

Figure 56: Slave Serial Mode Programming Switching Characteristics

XC4000E Guaranteed Input and Output Parameters (Pin-to-Pin, TTL I/O)

All values listed below are tested directly, and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The XACT delay calculator uses this indirect method. When there is a discrepancy between the two methods, the values listed below should be used, and the derived values must be ignored. All values are expressed in units of nanoseconds.

		Speed Grade	-4	-3	-2
Description	**Symbol**	**Device**			
Global Clock to Output (fast) using OFF 	T_{ICKOF} (Max)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	12.5 14.0 14.5 15.0 16.0 16.5 17.0 17.0	10.2 10.7 10.7 10.8 10.9 11.0 11.0 12.6	8.7 9.1 9.1 9.2 9.3 9.4 10.2 10.8
Global Clock to Output (slew-limited) using OFF 	T_{ICKO} (Max)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	16.5 18.0 18.5 19.0 20.0 20.5 21.0 21.0	14.0 14.7 14.7 14.8 14.9 15.0 15.1 15.3	11.5 12.0 12.0 12.1 12.2 12.8 12.8 13.0
Input Setup Time, using IFF (no delay) 	T_{PSUF} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	2.5 2.0 1.9 1.4 1.0 0.5 0 0	2.3 1.2 1.0 0.6 0.2 0 0 0	2.3 1.2 1.0 0.6 0.2 0 0 0
Input Hold Time, using IFF (no delay) 	T_{PHF} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	4.0 4.6 5.0 6.0 6.0 7.0 7.5 8.0	4.0 4.5 4.7 5.1 5.5 6.5 6.7 7.0	4.0 4.5 4.7 5.1 5.5 5.5 5.7 5.9
Input Setup Time, using IFF (with delay) 	T_{PSU} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	8.5 8.5 8.5 8.5 8.5 8.5 9.5 9.5	7.0 7.0 7.0 7.0 7.0 7.0 7.0 7.6	6.0 6.0 6.0 6.0 6.0 6.0 6.8 6.8
Input Hold Time, using IFF (with delay) 	T_{PH} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

OFF = Output Flip-Flop IFF = Input Flip-Flop or Latch **Preliminary**

XC4000E IOB Output Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2			
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Propagation Delays (TTL Output Levels)									
Clock (OK) to Pad, fast	T_{OKPOF}		7.5		6.5		4.5		
slew-rate limited	T_{OKPOS}		11.5		9.5		7.0		
Output (O) to Pad, fast	T_{OPF}		8.0		5.5		4.8		
slew-rate limited	T_{OPS}		12.0		8.5		7.3		
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}		5.0		4.2		3.8		
3-state to Pad active and valid, fast	T_{TSONF}		9.7		8.1		7.3		
slew-rate limited	T_{TSONS}		13.7		11.1		9.8		
Propagation Delays (CMOS Output Levels)									
Clock (OK) to Pad, fast	T_{OKPOFC}		9.5		7.8		7.0		
slew-rate limited	T_{OKPOSC}		13.5		11.6		10.4		
Output (O) to Pad, fast	T_{OPFC}		10.0		9.7		8.7		
slew-rate limited	T_{OPSC}		14.0		13.4		12.1		
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZC}		5.2		4.3		3.9		
3-state to Pad active and valid, fast	T_{TSONFC}		9.1		7.6		6.8		
slew-rate limited	T_{TSONSC}		13.1		11.4		10.2		
							Preliminary		

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the “Additional XC4000 Data” section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Device-Specific Pinout Tables

Pin Locations for XC4003E Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

XC4003E Pad Name	PC 84	PQ 100	VQ 100	PG 120	Bndry Scan
VCC	P2	P92	P89	G3	-
I/O (A8)	P3	P93	P90	G1	32
I/O (A9)	P4	P94	P91	F1	35
I/O	-	P95	P92	E1	38
I/O	-	P96	P93	F2	41
I/O (A10)	P5	P97	P94	F3	44
I/O (A11)	P6	P98	P95	D1	47
I/O (A12)	P7	P99	P96	C1	50
I/O (A13)	P8	P100	P97	D2	53
I/O (A14)	P9	P1	P98	C2	56
I/O, SGCK1 (A15)	P10	P2	P99	D3	59
VCC	P11	P3	P100	C3	-
GND	P12	P4	P1	C4	-
I/O, PGCK1 (A16)	P13	P5	P2	B2	62
I/O (A17)	P14	P6	P3	B3	65
I/O, TDI	P15	P7	P4	C5	68
I/O, TCK	P16	P8	P5	B4	71
I/O, TMS	P17	P9	P6	B5	74
I/O	P18	P10	P7	A4	77
I/O	-	-	-	C6	80
I/O	-	P11	P8	A5	83
I/O	P19	P12	P9	B6	86
I/O	P20	P13	P10	A6	89
GND	P21	P14	P11	B7	-
VCC	P22	P15	P12	C7	-
I/O	P23	P16	P13	A7	92
I/O	P24	P17	P14	A8	95
I/O	-	P18	P15	A9	98
I/O	-	-	-	B8	101
I/O	P25	P19	P16	C8	104
I/O	P26	P20	P17	A10	107
I/O	P27	P21	P18	B9	110
I/O	-	P22	P19	A11	113
I/O	P28	P23	P20	C9	116
I/O, SCGK2	P29	P24	P21	A12	119
O (M1)	P30	P25	P22	B11	122
GND	P31	P26	P23	C10	-
I (M0)	P32	P27	P24	C11	125
VCC	P33	P28	P25	D11	-
I (M2)	P34	P29	P26	B12	126
I/O, PGCK2	P35	P30	P27	C12	127
I/O (HDC)	P36	P31	P28	A13	130
I/O	-	P32	P29	D12	133
I/O ($\overline{\text{LDC}}$)	P37	P33	P30	C13	136
I/O	P38	P34	P31	E12	139
I/O	P39	P35	P32	D13	142
I/O	-	P36	P33	F11	145
I/O	-	P37	P34	E13	148
I/O	P40	P38	P35	F12	151
I/O ($\overline{\text{INIT}}$)	P41	P39	P36	F13	154
VCC	P42	P40	P37	G12	-
GND	P43	P41	P38	G11	-
I/O	P44	P42	P39	G13	157
I/O	P45	P43	P40	H13	160
I/O	-	P44	P41	J13	163
I/O	-	P45	P42	H12	166
I/O	P46	P46	P43	H11	169
I/O	P47	P47	P44	K13	172
I/O	P48	P48	P45	J12	175
I/O	P49	P49	P46	L13	178
I/O	P50	P50	P47	M13	181
I/O, SGCK3	P51	P51	P48	L12	184
GND	P52	P52	P49	K11	-
DONE	P53	P53	P50	L11	-
VCC	P54	P54	P51	L10	-
$\overline{\text{PROGRAM}}$	P55	P55	P52	M12	-
I/O (D7)	P56	P56	P53	M11	187
I/O, PGCK3	P57	P57	P54	N13	190
I/O (D6)	P58	P58	P55	M10	193
I/O	-	P59	P56	N11	196
I/O (D5)	P59	P60	P57	M9	199
I/O ($\overline{\text{CS0}}$)	P60	P61	P58	N10	202
I/O	-	P62	P59	L8	205
I/O	-	P63	P60	N9	208
I/O (D4)	P61	P64	P61	M8	211
I/O	P62	P65	P62	N8	214
VCC	P63	P66	P63	M7	-
GND	P64	P67	P64	L7	-
I/O (D3)	P65	P68	P65	N7	217
I/O ($\overline{\text{RS}}$)	P66	P69	P66	N6	220
I/O	-	P70	P67	N5	223
I/O	-	-	-	M6	226
I/O (D2)	P67	P71	P68	L6	229
I/O	P68	P72	P69	N4	232
I/O (D1)	P69	P73	P70	M5	235
I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	P70	P74	P71	N3	238
I/O (D0, DIN)	P71	P75	P72	N2	241
I/O, SGCK4 (DOUT)	P72	P76	P73	M3	244
CCLK	P73	P77	P74	L4	-
VCC	P74	P78	P75	L3	-
O, TDO	P75	P79	P76	M2	0
GND	P76	P80	P77	K3	-
I/O (A0, $\overline{\text{WS}}$)	P77	P81	P78	L2	2
I/O, PGCK4 (A1)	P78	P82	P79	N1	5
I/O (CS1, A2)	P79	P83	P80	K2	8
I/O (A3)	P80	P84	P81	L1	11
I/O (A4)	P81	P85	P82	J2	14
I/O (A5)	P82	P86	P83	K1	17
I/O	-	P87	P84	H3	20
I/O	-	P88	P85	J1	23
I/O (A6)	P83	P89	P86	H2	26
I/O (A7)	P84	P90	P87	H1	29
GND	P1	P91	P88	G2	-

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Additional No Connect (N.C.) Connections on PG120 Package

PG120	PG120	PG120	PG120	PG120
A1	B10	E11	L5	N12
A2	B13	J3	L9	
A3	E2	J11	M1	
B1	E3	K12	M4	

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Pin Locations for XC4005E/L Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

XC4005 E/L Pad Name	PC 84	PQ 100	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
VCC	P2	P92	P128	H3	P142	P183	-
I/O (A8)	P3	P93	P129	H1	P143	P184	44
I/O (A9)	P4	P94	P130	G1	P144	P185	47
I/O	-	P95	P131	G2	P145	P186	50
I/O	-	P96	P132	G3	P146	P187	53
I/O (A10)	P5	P97	P133	F1	P147	P190	56
I/O (A11)	P6	P98	P134	F2	P148	P191	59
I/O	-	-	P135	E1	P149	P192	62
I/O	-	-	P136	E2	P150	P193	65
GND	-	-	P137	F3	P151	P194	-
I/O (A12)	P7	P99	P138	E3	P154	P199	68
I/O (A13)	P8	P100	P139	C1	P155	P200	71
I/O	-	-	P140	C2	P156	P201	74
I/O	-	-	P141	D3	P157	P202	77
I/O (A14)	P9	P1	P142	B1	P158	P203	80
I/O, SGCK1 (A15)	P10	P2	P143	B2	P159	P204	83
VCC	P11	P3	P144	C3	P160	P205	-
GND	P12	P4	P1	C4	P1	P2	-
I/O, PGCK1 (A16)	P13	P5	P2	B3	P2	P4	86
I/O (A17)	P14	P6	P3	A1	P3	P5	89
I/O	-	-	P4	A2	P4	P6	92
I/O	-	-	P5	C5	P5	P7	95
I/O, TDI	P15	P7	P6	B4	P6	P8	98
I/O, TCK	P16	P8	P7	A3	P7	P9	101
GND	-	-	P8	C6	P10	P14	-
I/O	-	-	P9	B5	P11	P15	104
I/O	-	-	P10	B6	P12	P16	107
I/O, TMS	P17	P9	P11	A5	P13	P17	110
I/O	P18	P10	P12	C7	P14	P18	113
I/O	-	-	P13	B7	P15	P21	116
I/O	-	P11	P14	A6	P16	P22	119
I/O	P19	P12	P15	A7	P17	P23	122
I/O	P20	P13	P16	A8	P18	P24	125
GND	P21	P14	P17	C8	P19	P25	-
VCC	P22	P15	P18	B8	P20	P26	-
I/O	P23	P16	P19	C9	P21	P27	128
I/O	P24	P17	P20	B9	P22	P28	131
I/O	-	P18	P21	A9	P23	P29	134
I/O	-	-	P22	B10	P24	P30	137
I/O	P25	P19	P23	C10	P25	P33	140
I/O	P26	P20	P24	A10	P26	P34	143
I/O	-	-	P25	A11	P27	P35	146
I/O	-	-	P26	B11	P28	P36	149
GND	-	-	P27	C11	P29	P37	-
I/O	P27	P21	P28	B12	P32	P42	152
I/O	-	P22	P29	A13	P33	P43	155
I/O	-	-	P30	A14	P34	P44	158
I/O	-	-	P31	C12	P35	P45	161
I/O	P28	P23	P32	B13	P36	P46	164
I/O, SCGK2	P29	P24	P33	B14	P37	P47	167
O (M1)	P30	P25	P34	A15	P38	P48	170
GND	P31	P26	P35	C13	P39	P49	-
I (M0)	P32	P27	P36	A16	P40	P50	173
VCC	P33	P28	P37	C14	P41	P55	-
I (M2)	P34	P29	P38	B15	P42	P56	174
I/O, PGCK2	P35	P30	P39	B16	P43	P57	175
I/O (HDC)	P36	P31	P40	D14	P44	P58	178
I/O	-	-	P41	C15	P45	P59	181
I/O	-	-	P42	D15	P46	P60	184
I/O	-	P32	P43	E14	P47	P61	187
I/O ($\overline{\text{LDC}}$)	P37	P33	P44	C16	P48	P62	190
GND	-	-	P45	F14	P51	P67	-
I/O	-	-	P46	F15	P52	P68	193
I/O	-	-	P47	E16	P53	P69	196
I/O	P38	P34	P48	F16	P54	P70	199
I/O	P39	P35	P49	G14	P55	P71	202
I/O	-	P36	P50	G15	P56	P74	205
I/O	-	P37	P51	G16	P57	P75	208
I/O	P40	P38	P52	H16	P58	P76	211
I/O ($\overline{\text{INIT}}$)	P41	P39	P53	H15	P59	P77	214
VCC	P42	P40	P54	H14	P60	P78	-
GND	P43	P41	P55	J14	P61	P79	-
I/O	P44	P42	P56	J15	P62	P80	217
I/O	P45	P43	P57	J16	P63	P81	220
I/O	-	P44	P58	K16	P64	P82	223
I/O	-	P45	P59	K15	P65	P83	226
I/O	P46	P46	P60	K14	P66	P86	229
I/O	P47	P47	P61	L16	P67	P87	232
I/O	-	-	P62	M16	P68	P88	235
I/O	-	-	P63	L15	P69	P89	238
GND	-	-	P64	L14	P70	P90	-
I/O	P48	P48	P65	P16	P73	P95	241
I/O	P49	P49	P66	M14	P74	P96	244
I/O	-	-	P67	N15	P75	P97	247
I/O	-	-	P68	P15	P76	P98	250
I/O	P50	P50	P69	N14	P77	P99	253

Pin Locations for XC4025E, XC4028EX, & XC4028XL Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
VCC	P183	J4	P212	K1	P38	VCC*	-
I/O (A8)	P184	J3	P213	K2	P37	D14	98
I/O (A9)	P185	J2	P214	K3	P36	C14	101
I/O (A19)	P186	J1	P215	K5	P35	A15	104
I/O (A18)	P187	H1	P216	K4	P34	B15	107
I/O	P188	H2	P217	J1	P33	C15	110
I/O	P189	H3	P218	J2	P32	D15	113
I/O (A10)	P190	G1	P220	H1	P31	A16	116
I/O (A11)	P191	G2	P221	J3	P30	B16	119
GND	-	-	-	-	-	GND*	-
I/O	-	-	-	J4	P29	C16	122
I/O	-	-	-	J5	P28	B17	125
I/O	-	-	-	H2	P27	C17	128
I/O	-	-	-	G1	P26	B18	131
VCC	-	-	P222	E1	P25	VCC*	-
I/O	-	H4	P223	H3	P23	C18	134
I/O	-	G4	P224	G2	P22	D17	137
I/O	P192	F1	P225	H4	P21	A20	140
I/O	P193	E1	P226	F2	P20	B19	143
GND	P194	G3	P227	F1	P19	GND*	-
I/O	-	-	-	H5	P18	C19	146
I/O	-	-	-	G3	P17	D18	149
I/O	P195	F2	P228	D1	P16	A21	152
I/O	P196	D1	P229	G4	P15	B20	155
I/O	P197	C1	P230	E2	P14	C20	158
I/O	P198	E2	P231	F3	P13	B21	161
I/O (A12)	P199	F3	P232	G5	P12	B22	164
I/O (A13)	P200	D2	P233	C1	P10	C21	167
GND	-	-	-	-	-	GND*	-
VCC	-	-	-	-	-	VCC*	-
I/O	-	-	-	F4	P9	D20	170
I/O	-	-	-	E3	P8	A23	173
I/O	-	F4	P234	D2	P7	D21	176
I/O	-	E4	P235	C2	P6	C22	179
I/O	P201	B1	P236	F5	P5	B24	182
I/O	P202	E3	P237	E4	P4	C23	185
I/O (A14)	P203	C2	P238	D3	P3	D22	188
I/O, SGCK1, GCK8 (A15)	P204	B2	P239	C3	P2	C24	191
VCC	P205	D3	P240	A2	P1	VCC*	-
GND	P2	D4	P1	B1	P304	GND*	-
I/O, PGCK1, GCK1 (A16)	P4	C3	P2	D4	P303	D23	194
I/O (A17)	P5	C4	P3	B2	P302	C25	197

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
I/O	P6	B3	P4	B3	P301	D24	200
I/O	P7	C5	P5	E6	P300	E23	203
I/O, TDI	P8	A2	P6	D5	P299	C26	206
I/O, TCK	P9	B4	P7	C4	P298	E24	209
I/O	-	-	-	A3	P297	F24	212
I/O	-	-	-	D6	P296	E25	215
VCC	-	-	-	-	-	VCC*	-
GND	-	-	-	-	-	GND*	-
I/O	P10	C6	P8	E7	P295	D26	218
I/O	P11	A3	P9	B4	P294	G24	221
I/O	P12	B5	P10	C5	P293	F25	224
I/O	P13	B6	P11	A4	P292	F26	227
I/O	-	D5	P12	D7	P291	H23	230
I/O	-	D6	P13	C6	P290	H24	233
I/O	-	-	-	E8	P289	G25	236
I/O	-	-	-	B5	P288	G26	239
GND	P14	C7	P14	A5	P287	GND*	-
I/O, FCLK1	P15	A4	P15	B6	P286	J23	242
I/O	P16	A5	P16	D8	P285	J24	245
I/O, TMS	P17	B7	P17	C7	P284	H25	248
I/O	P18	A6	P18	B7	P283	K23	251
VCC	-	-	P19	A6	P282	VCC*	-
I/O	-	D7	P20	C8	P280	K24	254
I/O	-	D8	P21	E9	P279	J25	257
I/O	-	-	-	A7	P278	L24	260
I/O	-	-	-	D9	P277	K25	263
GND‡	-	-	P22	-	-	GND*	-
I/O	-	-	-	B8	P276	L25	266
I/O	-	-	-	A8	P275	L26	269
I/O	P19	C8	P23	C9	P274	M23	272
I/O	P20	A7	P24	B9	P273	M24	275
I/O	P21	B8	P25	E10	P272	M25	278
I/O	P22	A8	P26	A9	P271	M26	281
I/O	P23	B9	P27	D10	P270	N24	284
I/O	P24	C9	P28	C10	P269	N25	287
GND	P25	D9	P29	A10	P268	GND*	-
VCC	P26	D10	P30	A11	P267	VCC*	-
I/O	P27	C10	P31	B10	P266	N26	290
I/O	P28	B10	P32	B11	P265	P25	293
I/O	P29	A9	P33	C11	P264	P23	296
I/O	P30	A10	P34	E11	P263	P24	299
I/O	P31	A11	P35	D11	P262	R26	302
I/O	P32	C11	P36	A12	P261	R25	305
I/O	-	-	-	B12	P260	R24	308
I/O	-	-	-	A13	P259	R23	311
GND‡	-	-	P37	-	-	GND*	-
I/O	-	-	-	C12	P258	T26	314
I/O	-	-	-	D12	P257	T25	317
I/O	-	D11	P38	E12	P256	T23	320
I/O	-	D12	P39	B13	P255	V26	323
VCC	-	-	P40	A16	P253	VCC*	-

Additional No Connect, Vcc & Ground Connections on BG352 Package

N.C.	VCC	GND
A18	A10	A1
A24	A17	A2
B4	B2	A5
B10	B25	A8
B23	D7	A14
C1	D13	A19
C5	D19	A22
C8	G23	A25
C11	H4	A26
D1	K1	B1
D16	K26	B26
D25	N23	E1
F23	P4	E26
J26	U1	H1
K2	U26	H26
L4	W23	N1
L23	Y4	P26
T3	AC8	W1
T4	AC14	W26
T24	AC20	AB1
U25	AE2	AB26
AB3	AE25	AE1
AC2	AF10	AE26
AC6	AF17	AF1
AC11		AF2
AC16		AF5
AC21		AF8
AC25		AF13
AD16		AF19
AD21		AF22
AD26		AF25
AE4		AF26
AE10		

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XC4052XL Pad Name	PG411	BG432	Bndry Scan
I/O	AE39	AH13	703
I/O	AM36	AL12	706
I/O	AC35	AK12	709
I/O	AL35	AJ12	712
I/O	AF38	AK11	715
GND	GND*	GND*	-
I/O	AG39	AH12	718
I/O	AG37	AJ11	721
VCC	VCC*	VCC*	-
I/O	AD34	AL10	724
I/O	AN39	AK10	727
I/O	AE35	AJ10	730
I/O	AH38	AK9	733
GND	GND*	GND*	-
I/O	AJ37	AL8	736
I/O	AG35	AH10	739
I/O	AF34	AJ9	742
I/O	AH36	AK8	745
GND	GND*	GND*	-
I/O	AK38	AJ8	748
I/O	AP38	AH9	751
I/O	AK36	AK7	754
I/O	AM34	AL6	757
I/O	AH34	AJ7	760
I/O	AJ35	AH8	763
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	AL37	AK6	766
I/O	AT38	AL5	769
I/O	AM38	AH7	772
I/O	AN37	AJ6	775
I/O	AK34	AK5	778
I/O	AR39	AL4	781
GND	GND*	GND*	-
I/O	AR37	AH6	784
I/O	AU37	AJ5	787
I/O	AN35	AK4	790
I/O	AL33	AH5	793
I/O	AV38	AK3	796
I/O, GCK4	AT36	AJ4	799
GND	GND*	GND*	-
DONE	AR35	AH4	-
VCC	VCC*	VCC*	-
$\overline{\text{PROGRAM}}$	AN33	AH3	-
I/O (D7)	AM32	AJ2	802
I/O, GCK5	AP34	AG4	805
I/O	AW39	AG3	808
I/O	AN31	AH2	811

XC4052XL Pad Name	PG411	BG432	Bndry Scan
I/O	AV36	AH1	814
I/O	AR33	AF4	817
GND	GND*	GND*	-
I/O	AP32	AF3	820
I/O	AU35	AG2	823
I/O	AV34	AG1	826
I/O	AW35	AE4	829
I/O	AW33	AE3	832
I/O	AU33	AF2	835
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O (D6)	AV32	AF1	838
I/O	AU31	AD4	841
I/O	AR31	AD3	844
I/O	AP28	AE2	847
I/O	AP30	AD2	850
I/O	AT30	AC4	853
GND	GND*	GND*	-
I/O	AT32	AC3	856
I/O	AV30	AD1	859
I/O	AR29	AC2	862
I/O	AP26	AB4	865
GND	GND*	GND*	-
I/O	AU29	AB3	868
I/O	AV28	AB2	871
I/O, FCLK3	AT28	AB1	874
I/O	AR25	AA3	877
VCC	VCC*	VCC*	-
I/O (D5)	AP24	AA2	880
I/O ($\overline{\text{CS0}}$)	AU27	Y2	883
GND	GND*	GND*	-
I/O	AR27	Y4	886
I/O	AW27	Y3	889
I/O	AU25	Y1	892
I/O	AV26	W1	895
I/O	AT24	W4	898
I/O	AR23	W3	901
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	AW25	W2	904
I/O	AW23	V2	907
I/O	AP22	V4	910
I/O	AV24	V3	913
I/O	AU23	U1	916
I/O	AT22	U2	919
GND	GND*	GND*	-
I/O	AR21	U4	922
I/O	AV22	U3	925

Additional Vcc & Ground Connections on PG411 Package

VCC	GND
A3	A9
A11	A19
A21	A29
A31	A37
C39	C1
D6	D14
F36	D20
J1	D26
L39	D34
W1	F4
AA39	J39
AJ1	L1
AL39	P4
AP4	P36
AT34	W39
AU1	Y4
AW9	Y36
AW19	AA1
AW29	AF4
AW37	AF36
	AJ39
	AL1
	AP36
	AT6
	AT14
	AT20
	AT26
	AU39
	AW3
	AW11
	AW21
	AW31

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Additional No Connect, Vcc & Ground Connections on BG432 Package

N.C.	VCC	GND
C8	A1	A2
	A11	A3
	A21	A7
	A31	A9
	C3	A14
	C29	A18
	D11	A23
	D21	A25
	L1	A29
	L4	A30
	L28	B1
	L31	B2
	AA1	B30
	AA4	B31
	AA28	C1
	AA31	C31
	AH11	D16
	AH21	G1
	AJ3	G31
	AJ29	J1
	AL1	J31
	AL11	P1
	AL21	P31
	AL31	T4
		T28
		V1
		V31
		AC1
		AC31
		AE1
		AE31
		AH16
		AJ1
		AJ31
		AK1
		AK2
		AK30
		AK31
		AL2
		AL3
		AL7
		AL9
		AL14
		AL18
		AL23
		AL25
		AL29
		AL30

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Package-Specific Pinout Tables

PC84 Package Pinouts

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

Pin	XC4003E	XC4005E XC4005L	XC4006E	XC4008E	XC4010E XC4010L
P1	GND	GND	GND	GND	GND
P2	VCC	VCC	VCC	VCC	VCC
P3	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)
P4	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)
P5	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)
P6	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)
P7	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)
P8	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)
P9	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)
P10	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
P11	VCC	VCC	VCC	VCC	VCC
P12	GND	GND	GND	GND	GND
P13	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
P14	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)
P15	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI
P16	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK
P17	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS
P18	I/O	I/O	I/O	I/O	I/O
P19	I/O	I/O	I/O	I/O	I/O
P20	I/O	I/O	I/O	I/O	I/O
P21	GND	GND	GND	GND	GND
P22	VCC	VCC	VCC	VCC	VCC
P23	I/O	I/O	I/O	I/O	I/O
P24	I/O	I/O	I/O	I/O	I/O
P25	I/O	I/O	I/O	I/O	I/O
P26	I/O	I/O	I/O	I/O	I/O
P27	I/O	I/O	I/O	I/O	I/O
P28	I/O	I/O	I/O	I/O	I/O
P29	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2
P30	O (M1)	O (M1)	O (M1)	O (M1)	O (M1)
P31	GND	GND	GND	GND	GND
P32	I (M0)	I (M0)	I (M0)	I (M0)	I (M0)
P33	VCC	VCC	VCC	VCC	VCC
P34	I (M2)	I (M2)	I (M2)	I (M2)	I (M2)
P35	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2
P36	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)
P37	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
P38	I/O	I/O	I/O	I/O	I/O
P39	I/O	I/O	I/O	I/O	I/O
P40	I/O	I/O	I/O	I/O	I/O
P41	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
P42	VCC	VCC	VCC	VCC	VCC
P43	GND	GND	GND	GND	GND
P44	I/O	I/O	I/O	I/O	I/O
P45	I/O	I/O	I/O	I/O	I/O
P46	I/O	I/O	I/O	I/O	I/O
P47	I/O	I/O	I/O	I/O	I/O
P48	I/O	I/O	I/O	I/O	I/O
P49	I/O	I/O	I/O	I/O	I/O
P50	I/O	I/O	I/O	I/O	I/O
P51	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3
P52	GND	GND	GND	GND	GND
P53	DONE	DONE	DONE	DONE	DONE
P54	VCC	VCC	VCC	VCC	VCC
P55	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$
P56	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)
P57	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3
P58	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)
P59	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)
P60	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)
P61	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)
P62	I/O	I/O	I/O	I/O	I/O
P63	VCC	VCC	VCC	VCC	VCC
P64	GND	GND	GND	GND	GND
P65	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
P66	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)
P67	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)
P68	I/O	I/O	I/O	I/O	I/O
P69	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)
P70	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)
P71	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)
P72	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
P73	CCLK	CCLK	CCLK	CCLK	CCLK
P74	VCC	VCC	VCC	VCC	VCC
P75	O, TDO	O, TDO	O, TDO	O, TDO	O, TDO
P76	GND	GND	GND	GND	GND
P77	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)
P78	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
P79	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)
P80	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)
P81	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)
P82	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)
P83	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)
P84	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)

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PQ240/ HQ240 Pin	XC4013E XC4013L	XC4020E	XC4025E	XC4028EX XC4028XL
P86	I/O	I/O	I/O	I/O
P87	I/O	I/O	I/O	I/O
P88	I/O	I/O	I/O	I/O
P89	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
P90	VCC	VCC	VCC	VCC
P91	GND	GND	GND	GND
P92	I/O	I/O	I/O	I/O
P93	I/O	I/O	I/O	I/O
P94	I/O	I/O	I/O	I/O
P95	I/O	I/O	I/O	I/O
P96	I/O	I/O	I/O	I/O
P97	I/O	I/O	I/O	I/O
P98	N.C.‡	N.C.‡	N.C.‡	GND‡
P99	I/O	I/O	I/O	I/O
P100	I/O	I/O	I/O	I/O
P101	VCC	VCC	VCC	VCC
P102	I/O	I/O	I/O	I/O
P103	I/O	I/O	I/O	I/O
P104	I/O	I/O	I/O	I/O
P105	I/O	I/O	I/O	I/O
P106	GND	GND	GND	GND
P107	I/O	I/O	I/O	I/O
P108	I/O	I/O	I/O	I/O
P109	I/O	I/O	I/O	I/O
P110	I/O	I/O	I/O	I/O
P111	I/O	I/O	I/O	I/O
P112	I/O	I/O	I/O	I/O
P113	I/O	I/O	I/O	I/O
P114	I/O	I/O	I/O	I/O
P115	I/O	I/O	I/O	I/O
P116	I/O	I/O	I/O	I/O
P117	I/O	I/O	I/O	I/O
P118	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, GCK4
P119	GND	GND	GND	GND
P120	DONE	DONE	DONE	DONE
P121	VCC	VCC	VCC	VCC
P122	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$
P123	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)
P124	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, GCK5
P125	I/O	I/O	I/O	I/O
P126	I/O	I/O	I/O	I/O
P127	I/O	I/O	I/O	I/O
P128	I/O	I/O	I/O	I/O
P129	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)

PQ240/ HQ240 Pin	XC4013E XC4013L	XC4020E	XC4025E	XC4028EX XC4028XL
P130	I/O	I/O	I/O	I/O
P131	I/O	I/O	I/O	I/O
P132	I/O	I/O	I/O	I/O
P133	I/O	I/O	I/O	I/O
P134	I/O	I/O	I/O	I/O
P135	GND	GND	GND	GND
P136	I/O	I/O	I/O	I/O
P137	I/O	I/O	I/O	I/O
P138	I/O	I/O	I/O	I/O, FCLK3
P139	I/O	I/O	I/O	I/O
P140	VCC	VCC	VCC	VCC
P141	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)
P142	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)
P143	N.C.‡	N.C.‡	N.C.‡	GND‡
P144	I/O	I/O	I/O	I/O
P145	I/O	I/O	I/O	I/O
P146	I/O	I/O	I/O	I/O
P147	I/O	I/O	I/O	I/O
P148	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)
P149	I/O	I/O	I/O	I/O
P150	VCC	VCC	VCC	VCC
P151	GND	GND	GND	GND
P152	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
P153	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)
P154	I/O	I/O	I/O	I/O
P155	I/O	I/O	I/O	I/O
P156	I/O	I/O	I/O	I/O
P157	I/O	I/O	I/O	I/O
P158	N.C.‡	N.C.‡	N.C.‡	GND‡
P159	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)
P160	I/O	I/O	I/O	I/O
P161	VCC	VCC	VCC	VCC
P162	I/O	I/O	I/O	I/O
P163	I/O	I/O	I/O	I/O, FCLK4
P164	I/O	I/O	I/O	I/O
P165	I/O	I/O	I/O	I/O
P166	GND	GND	GND	GND
P167	I/O	I/O	I/O	I/O
P168	I/O	I/O	I/O	I/O
P169	I/O	I/O	I/O	I/O
P170	I/O	I/O	I/O	I/O
P171	I/O	I/O	I/O	I/O
P172	I/O	I/O	I/O	I/O
P173	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)

PG299 Pin	XC4025E	XC4028EX/XL
E7	I/O	I/O
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	I/O	I/O
E14	I/O	I/O
E15	I/O	I/O
E16	GND	GND
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	GND	GND
D1	I/O	I/O
D2	I/O	I/O
D3	I/O (A14)	I/O (A14)
D4	I/O, PGCK1 (A16)	I/O, GCK1 (A16)
D5	I/O, TDI	I/O, TDI
D6	I/O	I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	I/O
D13	I/O	I/O, FCLK2
D14	I/O	I/O
D15	I/O	I/O
D16	I/O	I/O
D17	I (M2)	I (M2)
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
C1	I/O (A13)	I/O (A13)
C2	I/O	I/O
C3	I/O, SGCK1 (A15)	I/O, GCK8 (A15)
C4	I/O, TCK	I/O, TCK
C5	I/O	I/O
C6	I/O	I/O
C7	I/O, TMS	I/O, TMS
C8	I/O	I/O
C9	I/O	I/O
C10	I/O	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	I/O	I/O
C14	I/O	I/O
C15	I/O	I/O
C16	I/O	I/O
C17	I/O, SGCK2	I/O, GCK2
C18	I (M0)	I (M0)
C19	I/O (HDC)	I/O (HDC)
C20	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
B1	GND	GND
B2	I/O (A17)	I/O (A17)
B3	I/O	I/O
B4	I/O	I/O
B5	I/O	I/O
B6	I/O	I/O, FCLK1
B7	I/O	I/O
B8	I/O	I/O
B9	I/O	I/O
B10	I/O	I/O
B11	I/O	I/O
B12	I/O	I/O
B13	I/O	I/O
B14	I/O	I/O
B15	I/O	I/O
B16	I/O	I/O
B17	I/O	I/O
B18	I/O	I/O
B19	I/O, PGCK2	I/O, GCK3
B20	VCC	VCC
A2	VCC	VCC
A3	I/O	I/O
A4	I/O	I/O
A5	GND	GND
A6	VCC	VCC
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	GND	GND
A11	VCC	VCC
A12	I/O	I/O
A13	I/O	I/O
A14	I/O	I/O
A15	GND	GND
A16	VCC	VCC
A17	I/O	I/O
A18	I/O	I/O
A19	GND	GND
A20	O (M1)	O (M1)

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Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.