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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	196
Number of Logic Elements/Cells	466
Total RAM Bits	6272
Number of I/O	77
Number of Gates	5000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc4005l-5pq100c

Using Function Generators as RAM

Optional modes for each CLB make the memory look-up tables in the F' and G' function generators usable as an array of Read/Write memory cells. Available modes are level-sensitive (similar to the XC4000/A/H families), edge-triggered, and dual-port edge-triggered. Depending on the selected mode, a single CLB can be configured as either a 16x2, 32x1, or 16x1 bit array.

Supported CLB memory configurations and timing modes for single- and dual-port modes are shown in Table 5.

XC4000-Series devices are the first programmable logic devices with edge-triggered (synchronous) and dual-port RAM accessible to the user. Edge-triggered RAM simplifies system timing. Dual-port RAM doubles the effective throughput of FIFO applications. These features can be individually programmed in any XC4000-Series CLB.

Advantages of On-Chip and Edge-Triggered RAM

The on-chip RAM is extremely fast. The read access time is the same as the logic delay. The write access time is slightly slower. Both access times are much faster than any off-chip solution, because they avoid I/O delays.

Edge-triggered RAM, also called synchronous RAM, is a feature never before available in a Field Programmable Gate Array. The simplicity of designing with edge-triggered RAM, and the markedly higher achievable performance, add up to a significant improvement over existing devices with on-chip RAM.

Three application notes are available from Xilinx that discuss edge-triggered RAM: "*XC4000E Edge-Triggered and Dual-Port RAM Capability,*" "*Implementing FIFOs in XC4000E RAM,*" and "*Synchronous and Asynchronous FIFO Designs*." All three application notes apply to both XC4000E and XC4000EX RAM.

Table 5: Supported RAM Modes

	16 x 1	16 x 2	32 x 1	Edge-Triggered Timing	Level-Sensitive Timing
Single-Port	√	√	√	√	√
Dual-Port	√			√	

RAM Configuration Options

The function generators in any CLB can be configured as RAM arrays in the following sizes:

- Two 16x1 RAMs: two data inputs and two data outputs with identical or, if preferred, different addressing for each RAM
- One 32x1 RAM: one data input and one data output.

One F or G function generator can be configured as a 16x1 RAM while the other function generators are used to implement any function of up to 5 inputs.

Additionally, the XC4000-Series RAM may have either of two timing modes:

- Edge-Triggered (Synchronous): data written by the designated edge of the CLB clock. WE acts as a true clock enable.
- Level-Sensitive (Asynchronous): an external WE signal acts as the write strobe.

The selected timing mode applies to both function generators within a CLB when both are configured as RAM.

The number of read ports is also programmable:

- Single Port: each function generator has a common read and write port
- Dual Port: both function generators are configured together as a single 16x1 dual-port RAM with one write port and two read ports. Simultaneous read and write operations to the same or different addresses are supported.

RAM configuration options are selected by placing the appropriate library symbol.

Choosing a RAM Configuration Mode

The appropriate choice of RAM mode for a given design should be based on timing and resource requirements, desired functionality, and the simplicity of the design process. Recommended usage is shown in Table 6.

The difference between level-sensitive, edge-triggered, and dual-port RAM is only in the write operation. Read operation and timing is identical for all modes of operation.

Table 6: RAM Mode Selection

	Level-Sensitive	Edge-Triggered	Dual-Port Edge-Triggered
Use for New Designs?	No	Yes	Yes
Size (16x1, Registered)	1/2 CLB	1/2 CLB	1 CLB
Simultaneous Read/Write	No	No	Yes
Relative Performance	X	2X	2X (4X effective)

Fast Carry Logic

Each CLB F and G function generator contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources.

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level.

This fast carry logic is one of the more significant features of the XC4000 Series, speeding up arithmetic and counting into the 70 MHz range.

The carry chain in XC4000E devices can run either up or down. At the top and bottom of the columns where there are no CLBs above and below, the carry is propagated to the right. (See Figure 11.) In order to improve speed in the high-capacity XC4000EX devices, which can potentially have very long carry chains, the carry chain travels upward only, as shown in Figure 12. This restriction should have little impact, because the smallest XC4000EX device, the XC4028EX, can accommodate a 64-bit carry chain in a single column. Additionally, standard interconnect can be used to route a carry signal in the downward direction.

Figure 13 on page 22 shows an XC4000E CLB with dedicated fast carry logic. The carry logic in the XC4000EX is similar, except that COUT exits at the top only, and the signal CINDOWN does not exist. As shown in Figure 13, the carry logic shares operand and control inputs with the function generators. The carry outputs connect to the function generators, where they are combined with the operands to form the sums.

Figure 14 and Figure 15 on page 23 show the details of the carry logic for the XC4000E and the XC4000EX respectively. These diagrams show the contents of the box labeled “CARRY LOGIC” in Figure 13. As shown, the XC4000EX carry logic eliminated a multiplexer to reduce delay on the pass-through carry chain. Additionally, the multiplexer on the G4 path now has a memory-programmable input, which permits G4 to directly connect to COUT. G4 thus becomes an additional high-speed initialization path for carry-in.

The dedicated carry logic is discussed in detail in Xilinx document XAPP 013: “*Using the Dedicated Carry Logic in XC4000*.” This discussion also applies to XC4000E devices, and to XC4000EX devices when the minor logic changes are taken into account.

The fast carry logic can be accessed by placing special library symbols, or by using Xilinx Relationally Placed Macros (RPMs) that already include these symbols.

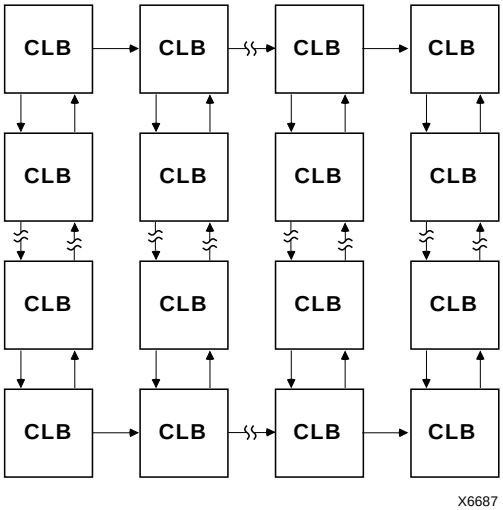


Figure 11: Available XC4000E Carry Propagation Paths

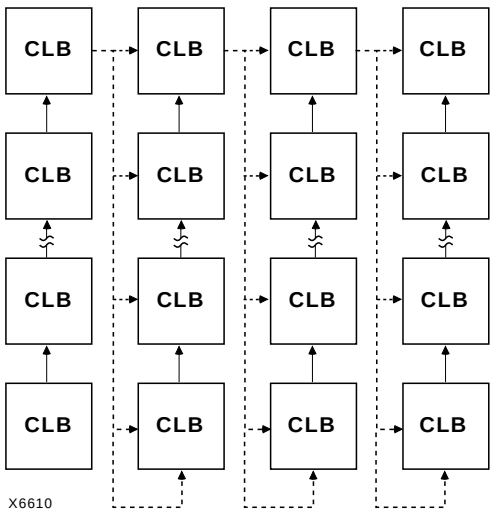


Figure 12: Available XC4000EX Carry Propagation Paths (dotted lines use general interconnect)

Table 18: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
TDO	O	O	If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed. This pin can be user output only when called out by special schematic definitions. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.
TDI, TCK, TMS	I	I/O or I (JTAG)	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special schematic definitions. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used.
HDC	O	I/O	High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin.
$\overline{\text{LDC}}$	O	I/O	Low During Configuration ($\overline{\text{LDC}}$) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, $\overline{\text{LDC}}$ is a user-programmable I/O pin.
$\overline{\text{INIT}}$	I/O	I/O	Before and during configuration, $\overline{\text{INIT}}$ is a bidirectional signal. A 1 kΩ - 10 kΩ external pull-up resistor is recommended. As an active-Low open-drain output, $\overline{\text{INIT}}$ is held Low during the power stabilization and internal clearing of the configuration memory. As an active-Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 µs after $\overline{\text{INIT}}$ has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, $\overline{\text{INIT}}$ is a user-programmable I/O pin.
PGCK1 - PGCK4 (XC4000E only)	Weak Pull-up	I or I/O	Four Primary Global inputs each drive a dedicated internal global net with short delay and minimal skew. If not used to drive a global buffer, any of these pins is a user-programmable I/O. The PGCK1-PGCK4 pins drive the four Primary Global Buffers. Any input pad symbol connected directly to the input of a BUFGP symbol is automatically placed on one of these pins.
SGCK1 - SGCK4 (XC4000E only)	Weak Pull-up	I or I/O	Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.
GCK1 - GCK8 (XC4000EX only)	Weak Pull-up	I or I/O	Eight inputs can each drive a Global Low-Skew buffer. In addition, each can drive a Global Early buffer. Each pair of global buffers can also be driven from internal logic, but must share an input signal. If not used to drive a global buffer, any of these pins is a user-programmable I/O. Any input pad symbol connected directly to the input of a BUFGLS or BUFGE symbol is automatically placed on one of these pins.
FCLK1 - FCLK4 (XC4000EX only)	Weak Pull-up	I or I/O	Four FCLK inputs can each drive a FastCLK buffer. The FastCLK buffers cannot be driven from internal logic. If not used to drive a global buffer, any of these pins is a user-programmable I/O. Any input pad symbol connected directly to the input of a BUFFCLK symbol is automatically placed on one of these pins.

Table 23: XC4000EX Program Data

Device	XC4028EX/XL	XC4036EX/XL	XC4044EX/XL	XC4052XL	XC4062XL
Max Logic Gates	28,000	36,000	44,000	52,000	62,000
CLBs (Row x Col.)	1,024 (32 x 32)	1,296 (36 x 36)	1,600 (40 x 40)	1,936 (44 x 44)	2,304 (48 x 48)
IOBs	256	288	320	352	384
Flip-Flops	2,560	3,168	3,840	4,576	5,376
Horizontal Longlines	192	216	240	264	288
TBUFs per Longline	34	38	42	46	50
Bits per Frame	421	469	517	565	613
Frames	1587	1775	1963	2151	2,339
Program Data	668,127	832,483	1,014,879	1,215,323	1,433,807
PROM Size (bits)	668,167	832,523	1,014,919	1,215,363	1,433,847

Notes:
1. Bits per Frame = (12 x number of rows) + 8 for the top + 16 for the bottom + 8 + 1 start bit + 4 error check bits
   Number of Frames = (47 x number of columns) + 27 for the left edge + 52 for the right edge + 4
   Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits
   PROM Size = Program Data + 40
2. The user can add more “one” bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra “one” bits, even for extra leading ones at the beginning of the header.
3. Express mode bitfiles are slightly larger (see Table 21).

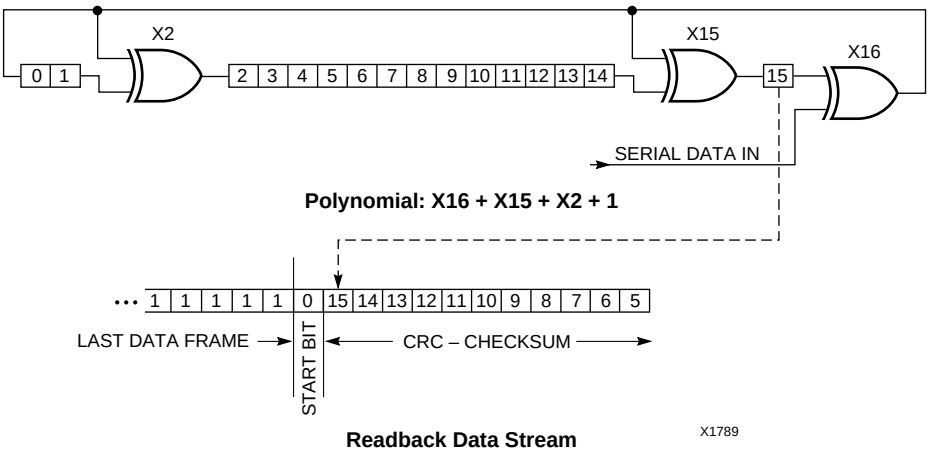


Figure 47: Circuit for Generating CRC-16

Configuration Timing

The seven configuration modes are discussed in detail in this section. Timing specifications are included.

Master Serial Mode

In Master Serial mode, the CCLK output of the lead FPGA drives a Xilinx Serial PROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The lead FPGA accepts this data on the subsequent rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In MakeBits, the user can specify Fast ConfigRate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight. The value increases from between 0.5 and 1.25 MHz, to a value between 4 and 10 MHz. (For low-voltage devices, the frequency can be up to 10% lower.) Be sure that the serial PROM and slaves are fast enough to support this data rate. XC2000, XC3000/A, and XC3100A devices do not support the Fast ConfigRate option.

The SPROM CE input can be driven from either $\overline{LDC}$ or DONE. Using $\overline{LDC}$ avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but $\overline{LDC}$ is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the early DONE option is invoked.

Figure 53 shows a full master/slave system. The leftmost device is in Master Serial mode.

Master Serial mode is selected by a <000> on the mode pins (M2, M1, M0).

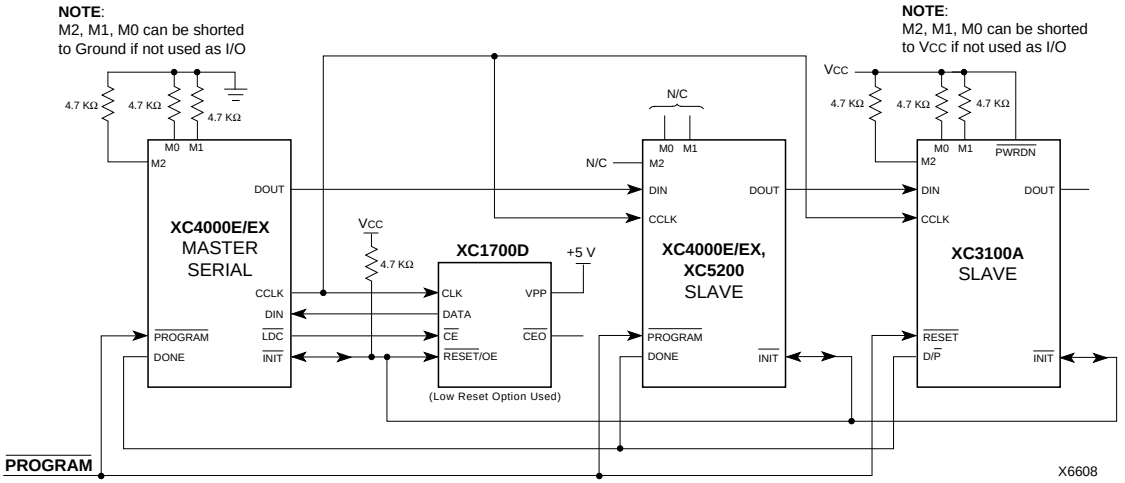
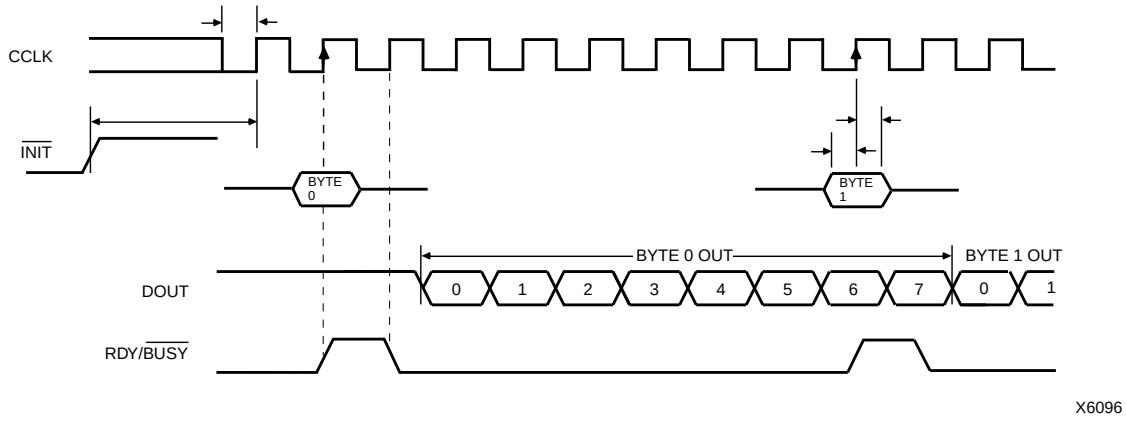


Figure 53: Master Serial Mode Circuit Diagram



	Description	Symbol	Min	Max	Units
CCLK	$\overline{INIT}$ (High) setup time	T_{IC}	5		µs
	D0 - D7 setup time	T_{DC}	60		ns
	D0 - D7 hold time	T_{CD}	0		ns
	CCLK High time	T_{CCH}	50		ns
	CCLK Low time	T_{CCL}	60		ns
	CCLK Frequency	F_{CC}		8	MHz

Notes:
1. Peripheral Synchronous mode can be considered Slave Parallel mode. An external CCLK provides timing, clocking in the **first** data byte on the **second** rising edge of CCLK after $\overline{INIT}$ goes High. Subsequent data bytes are clocked in on every eighth consecutive rising edge of CCLK.
2. The RDY/$\overline{BUSY}$ line goes High for one CCLK period after data has been clocked in, although synchronous operation does not require such a response.
3. The pin name RDY/$\overline{BUSY}$ is a misnomer. In Synchronous Peripheral mode this is really an ACKNOWLEDGE signal.
4. Note that data starts to shift out serially on the DOUT pin 0.5 CCLK periods after it was loaded in parallel. Therefore, additional CCLK pulses are clearly required after the last byte has been loaded.

Figure 60: Synchronous Peripheral Mode Programming Switching Characteristics

Asynchronous Peripheral Mode

Write to FPGA

Asynchronous Peripheral mode uses the trailing edge of the logic AND condition of $\overline{WS}$ and $\overline{CS0}$ being Low and $\overline{RS}$ and CS1 being High to accept byte-wide data from a microprocessor bus. In the lead FPGA, this data is loaded into a double-buffered UART-like parallel-to-serial converter and is serially shifted into the internal logic.

The lead FPGA presents the preamble data (and all data that overflows the lead device) on its DOUT pin. The RDY/$\overline{BUSY}$ output from the lead FPGA acts as a handshake signal to the microprocessor. RDY/$\overline{BUSY}$ goes Low when a byte has been received, and goes High again when the byte-wide input buffer has transferred its information into the shift register, and the buffer is ready to receive new data. A new write may be started immediately, as soon as the RDY/$\overline{BUSY}$ output has gone Low, acknowledging receipt of the previous data. Write may not be terminated until RDY/$\overline{BUSY}$ is High again for one CCLK period. Note that RDY/$\overline{BUSY}$ is pulled High with a high-impedance pull-up prior to $\overline{INIT}$ going High.

The length of the $\overline{BUSY}$ signal depends on the activity in the UART. If the shift register was empty when the new byte was received, the $\overline{BUSY}$ signal lasts for only two CCLK periods. If the shift register was still full when the new byte was received, the $\overline{BUSY}$ signal can be as long as nine CCLK periods.

Note that after the last byte has been entered, only seven of its bits are shifted out. CCLK remains High with DOUT equal to bit 6 (the next-to-last bit) of the last byte entered.

The READY/$\overline{BUSY}$ handshake can be ignored if the delay from any one Write to the end of the next Write is guaranteed to be longer than 10 CCLK periods.

Status Read

The logic AND condition of the $\overline{CS0}$, CS1and $\overline{RS}$ inputs puts the device status on the Data bus.

- D7 High indicates Ready
- D7 Low indicates Busy
- D0 through D6 go unconditionally High

It is mandatory that the whole start-up sequence be started and completed by one byte-wide input. Otherwise, the pins used as Write Strobe or Chip Enable might become active outputs and interfere with the final byte transfer. If this transfer does not occur, the start-up sequence is not completed all the way to the finish (point F in Figure 49 on page 61).

In this case, at worst, the internal reset is not released. At best, Readback and Boundary Scan are inhibited. The length-count value, as generated by MakeBits and MakePROM, ensures that these problems never occur.

Although RDY/$\overline{BUSY}$ is brought out as a separate signal, microprocessors can more easily read this information on one of the data lines. For this purpose, D7 represents the RDY/$\overline{BUSY}$ status when $\overline{RS}$ is Low, $\overline{WS}$ is High, and the two chip select lines are both active.

Asynchronous Peripheral mode is selected by a <101> on the mode pins (M2, M1, M0).

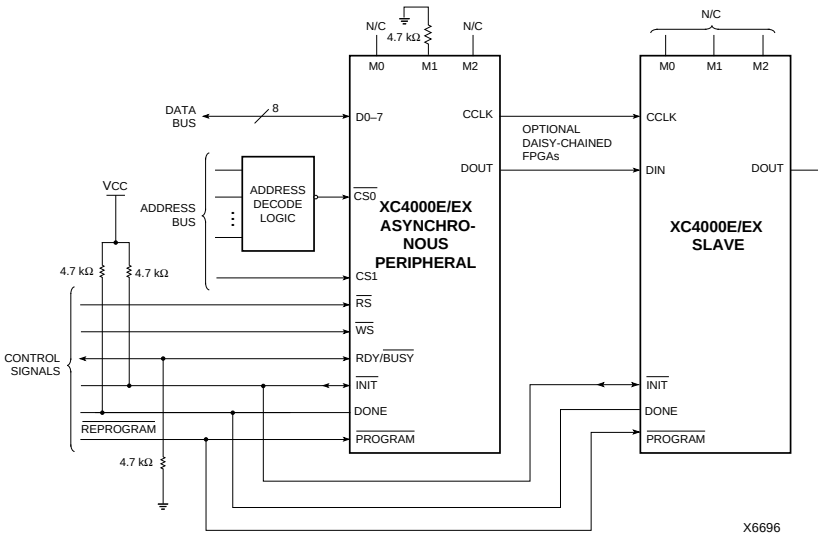


Figure 61: Asynchronous Peripheral Mode Circuit Diagram

Express Mode (XC4000EX only)

Express mode is similar to Slave Serial mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers. A CCLK frequency of 1 MHz is equivalent to a 8 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not support CRC error checking, but does support constant-field error checking.

In Express mode, an external signal drives the CCLK input of the FPGA device. The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge.

Express mode is only supported by the XC4000EX and XC5200 families. It may not be used, therefore, when an XC4000EX or XC5200 device is daisy-chained with devices from other Xilinx families.

If the first device is configured in Express mode, additional devices may be daisy-chained only if every device in the chain is also configured in Express mode. CCLK pins are tied together and D0-D7 pins are tied together for all devices along the chain. A status signal is passed from DOUT to CS1 of successive devices along the chain. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pullup). Frame data is accepted only when CS1 is High and the device's configuration memory is not already full. The status pin DOUT is pulled Low two internal-oscillator cycles after $\overline{\text{INIT}}$ is recognized as High, and remains Low until the device's configuration memory is full. DOUT is then pulled High to signal the next device in the chain to accept the configuration data on the D0-D7 bus.

The DONE pins of all devices in the chain should be tied together, with one or more active internal pull-ups. If a large number of devices are included in the chain, deactivate some of the internal pull-ups, since the Low-driving DONE pin of the last device in the chain must sink the current from all pull-ups in the chain. The DONE pull-up is activated by default. It can be deactivated using a MakeBits option.

XC4000EX devices in Express mode are always synchronized to DONE. The device becomes active after DONE goes High. DONE is an open-drain output. With the DONE pins tied together, therefore, the external DONE signal stays low until all devices are configured, then all devices in the daisy chain become active simultaneously. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured. XC5200 devices in the chain should be configured as synchronized to DONE (MakeBits option CCLK_SYNC or UCLK_SYNC), and their DONE pins wired together with those of the XC4000EX devices.

Express mode must be specified as an option to the MakeBits program, which generates the bitstream. The Express mode bitstream is not compatible with the other six configuration modes.

Express mode is selected by a <010> on the mode pins (M2, M1, M0).

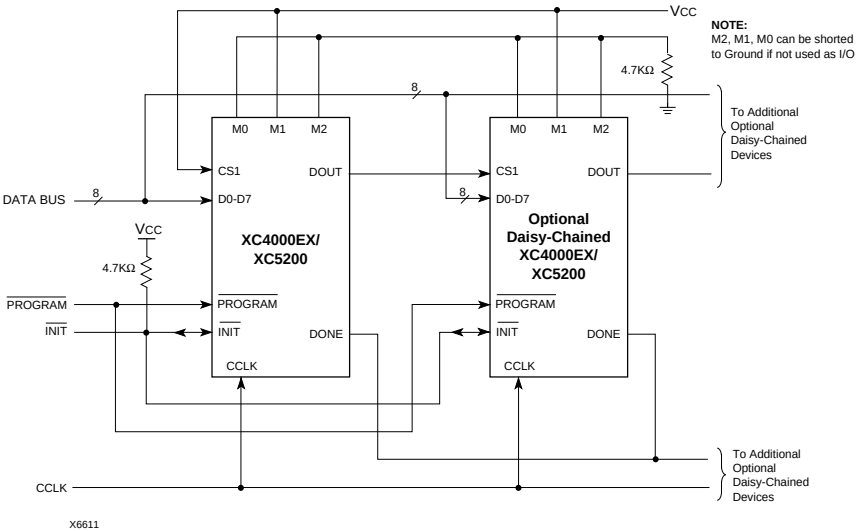
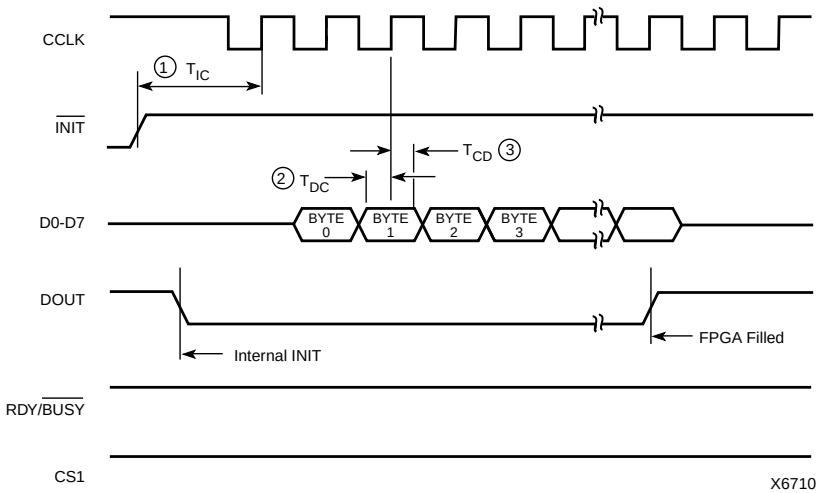


Figure 63: Express Mode Circuit Diagram

	Description	Symbol	Min	Max	Units
CCLK	$\overline{INIT}$ (High) setup time	T_{IC}	-		µs
	D0 - D7 setup time	T_{DC}	-		ns
	D0 - D7 hold time	T_{CD}	0		ns
	CCLK High time	T_{CCH}	-		ns
	CCLK Low time	T_{CCL}	-		ns
	CCLK Frequency	F_{CC}		-	MHz
			Preliminary		



Note: If not driven by the preceding DOUT, CS1 *must* remain High until the device is fully configured.

Figure 64: Express Mode Programming Switching Characteristics

Table 24: Pin Functions During Configuration

CONFIGURATION MODE <M2:M1:M0>							
SLAVE SERIAL <1:1:1>	**MASTER SERIAL <0:0:0>**	**SYNCH. PERIPH-ERAL <0:1:1>**	**ASYNCH. PERIPH-ERAL <1:0:1>**	**MASTER PARALLEL DOWN <1:1:0>**	**MASTER PARALLEL UP <1:0:0>**	**EXPRESS <0:1:0>**	**USER OPERATION**
M2(HIGH) (I)	M2(LOW) (I)	M2(LOW) (I)	M2(HIGH) (I)	M2(HIGH) (I)	M2(HIGH) (I)	M2(LOW) (I)	(I)
M1(HIGH) (I)	M1(LOW) (I)	M1(HIGH) (I)	M1(LOW) (I)	M1(HIGH) (I)	M1(LOW) (I)	M1(HIGH) (I)	(O)
M0(HIGH) (I)	M0(LOW) (I)	M0(HIGH) (I)	M0(HIGH) (I)	M0(LOW) (I)	M0(LOW) (I)	M0(HIGH) (I)	(I)
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	I/O
$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (O)	CCLK (O)	CCLK (O)	CCLK (I)	CCLK (I)
		RDY/$\overline{\text{BUSY}}$ (O)	RDY/$\overline{\text{BUSY}}$ (O)	$\overline{\text{RCLK}}$ (O)	$\overline{\text{RCLK}}$ (O)		I/O
			$\overline{\text{RS}}$ (I)				I/O
			$\overline{\text{CS0}}$ (I)				I/O
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	I/O
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	I/O
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	I/O
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	I/O
		DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	SGCK4-GCK5-I/O
TDI	TDI	TDI	TDI	TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK	TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS	TMS	TMS	TMS	TMS-I/O
TDO	TDO	TDO	TDO	TDO	TDO	TDO	TDO-(O)
			$\overline{\text{WS}}$ (I)	A0	A0		I/O
				A1	A1		PGCK4-GCK6-I/O
			CS1	A2	A2		I/O
				A3	A3		I/O
				A4	A4		I/O
				A5	A5		I/O
				A6	A6		I/O
				A7	A7		I/O
				A8	A8		I/O
				A9	A9		I/O
				A10	A10		I/O
				A11	A11		I/O
				A12	A12		I/O
				A13	A13		I/O
				A14	A14		I/O
				A15	A15		SGCK1-GCK7-I/O
				A16	A16		PGCK1-GCK8-I/O
				A17	A17		I/O
				A18*	A18*		I/O
				A19*	A19*		I/O
				A20*	A20*		I/O
				A21*	A21*		I/O
							ALL OTHERS

* XC4000EX only

Notes 1. A shaded table cell represents a 50 kΩ - 100 kΩ pull-up before and during configuration.
2. (I) represents an input; (O) represents an output.
3. $\overline{\text{INIT}}$ is an open-drain output during configuration.

XC4000E Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, not for production.
Preliminary: Based on preliminary characterization. Further changes are not expected.
Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.[1]

XC4000E Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = -0 °C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	4.5	5.5	V
	Supply voltage relative to GND, T_C = -55°C to +125°C	Military	4.5	5.5	V
V_{IH}	High-level input voltage	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time (Note 2)			250	ns

Note 1: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
Note 2: Typical value only. Not tested or characterized.
Note 3: Input and output measurement thresholds for TTL are 1.5 V. Input and output measurement thresholds for CMOS are 2.5 V.

XC4000E DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0mA, V_{CC} min	TTL outputs	2.4		V
	High-level output voltage @ I_{OH} = -1.0mA, V_{CC} min	CMOS outputs	V_{CC}-0.5		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0mA, V_{CC} min (Note 1)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 2)	TTL input levels		10	mA
		CMOS input levels		1	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	PQFP and MQFP packages		10	pF
		Other packages		16	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	0.25	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.2	2.5	mA

Note 1: With 50% of the outputs simultaneously sinking 12mA, up to a maximum of 64 pins.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND, and the FPGA configured with a MakeBits Tie option.

1. Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

XC4000E CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2			
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Combinatorial Delays									
F/G inputs to X/Y outputs	T_{ILO}		2.7		2.0		1.6		
F/G inputs via H' to X/Y outputs	T_{IHO}		4.7		4.3		2.7		
C inputs via SR through H' to X/Y outputs	T_{HH0O}		4.1		3.3		2.4		
C inputs via H' to X/Y outputs	T_{HH1O}		3.7		3.6		2.2		
C inputs via DIN through H' to X/Y outputs	T_{HH2O}		4.5		3.6		2.6		
CLB Fast Carry Logic									
Operand inputs (F1, F2, G1, G4) to COUT	T_{OPCY}		3.2		2.6		2.1		
Add/Subtract input (F3) to COUT	T_{ASCY}		5.5		4.4		3.7		
Initialization inputs (F1, F3) to COUT	T_{INCY}		1.7		1.7		1.4		
CIN through function generators to X/Y outputs	T_{SUM}		3.8		3.3		2.6		
CIN to COUT, bypass function generators	T_{BYP}		1.0		0.7		0.6		
Sequential Delays									
Clock K to outputs Q	T_{CKO}		3.7		2.8		2.8		
Setup Time before Clock K									
F/G inputs	T_{ICK}	4.0		3.0		2.4			
F/G inputs via H'	T_{IHCK}	6.1		4.6		3.9			
C inputs via H0 through H'	T_{HH0CK}	4.5		3.6		3.5			
C inputs via H1 through H'	T_{HH1CK}	5.0		4.1		3.3			
C inputs via H2 through H'	T_{HH2CK}	4.8		3.8		3.7			
C inputs via DIN	T_{DICK}	3.0		2.4		2.0			
C inputs via EC	T_{ECCK}	4.0		3.0		2.6			
C inputs via S/R, going Low (inactive)	T_{RCK}	4.2		4.0		4.0			
C_{IN} input via F'/G'	T_{CCK}								
C_{IN} input via F'/G' and H'	T_{CHCK}								
						Preliminary			

Pin Locations for XC4010E/L Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

XC4010E/L Pad Name	PC 84	PQ 160	TQ 176	PG 191	PQ/ HQ 208	BG 225	Bndry Scan
VCC	P2	P142	P155	J4	P183	D8	-
I/O (A8)	P3	P143	P156	J3	P184	E8	62
I/O (A9)	P4	P144	P157	J2	P185	B7	65
I/O	-	P145	P158	J1	P186	A7	68
I/O	-	P146	P159	H1	P187	C7	71
I/O	-	-	P160	H2	P188	D7	74
I/O	-	-	P161	H3	P189	E7	77
I/O (A10)	P5	P147	P162	G1	P190	A6	80
I/O (A11)	P6	P148	P163	G2	P191	B6	83
I/O	-	P149	P164	F1	P192	A5	86
I/O	-	P150	P165	E1	P193	B5	89
GND	-	P151	P166	G3	P194	GND*	-
I/O	-	-	-	F2	P195	D6	92
I/O	-	-	P167	D1	P196	C5	95
I/O	-	P152	P168	C1	P197	A4	98
I/O	-	P153	P169	E2	P198	E6	101
I/O (A12)	P7	P154	P170	F3	P199	B4	104
I/O (A13)	P8	P155	P171	D2	P200	D5	107
I/O	-	P156	P172	B1	P201	B3	110
I/O	-	P157	P173	E3	P202	F6	113
I/O (A14)	P9	P158	P174	C2	P203	A2	116
I/O, SGCK1 (A15)	P10	P159	P175	B2	P204	C3	119
VCC	P11	P160	P176	D3	P205	B2	-
GND	P12	P1	P1	D4	P2	A1	-
I/O, PGCK1 (A16)	P13	P2	P2	C3	P4	D4	122
I/O (A17)	P14	P3	P3	C4	P5	B1	125
I/O	-	P4	P4	B3	P6	C2	128
I/O	-	P5	P5	C5	P7	E5	131
I/O, TDI	P15	P6	P6	A2	P8	D3	134
I/O, TCK	P16	P7	P7	B4	P9	C1	137
I/O	-	P8	P8	C6	P10	D2	140
I/O	-	P9	P9	A3	P11	G6	143
I/O	-	-	-	B5	P12	E4	146
I/O	-	-	-	B6	P13	D1	149
GND	-	P10	P10	C7	P14	GND*	-
I/O	-	P11	P11	A4	P15	F5	152
I/O	-	P12	P12	A5	P16	E1	155
I/O, TMS	P17	P13	P13	B7	P17	F4	158
I/O	P18	P14	P14	A6	P18	F3	161
I/O	-	-	P15	C8	P19	G4	164
I/O	-	-	P16	A7	P20	G3	167
I/O	-	P15	P17	B8	P21	G2	170
I/O	-	P16	P18	A8	P22	G1	173
I/O	P19	P17	P19	B9	P23	G5	176
I/O	P20	P18	P20	C9	P24	H3	179
GND	P21	P19	P21	D9	P25	H2	-
VCC	P22	P20	P22	D10	P26	H1	-
I/O	P23	P21	P23	C10	P27	H4	182
I/O	P24	P22	P24	B10	P28	H5	185
I/O	-	P23	P25	A9	P29	J2	188
I/O	-	P24	P26	A10	P30	J1	191
I/O	-	-	P27	A11	P31	J3	194
I/O	-	-	P28	C11	P32	J4	197
I/O	P25	P25	P29	B11	P33	K2	200
I/O	P26	P26	P30	A12	P34	K3	203
I/O	-	P27	P31	B12	P35	J6	206
I/O	-	P28	P32	A13	P36	L1	209
GND	-	P29	P33	C12	P37	GND*	-
I/O	-	-	-	B13	P38	L3	212
I/O	-	-	-	A14	P39	M1	215
I/O	-	P30	P34	A15	P40	K5	218
I/O	-	P31	P35	C13	P41	M2	221
I/O	P27	P32	P36	B14	P42	L4	224
I/O	-	P33	P37	A16	P43	N1	227
I/O	-	P34	P38	B15	P44	M3	230
I/O	-	P35	P39	C14	P45	N2	233
I/O	P28	P36	P40	A17	P46	K6	236
I/O, SCGK2	P29	P37	P41	B16	P47	P1	239
O (M1)	P30	P38	P42	C15	P48	N3	242
GND	P31	P39	P43	D15	P49	GND*	-
I (M0)	P32	P40	P44	A18	P50	P2	245
VCC	P33	P41	P45	D16	P55	R1	-
I (M2)	P34	P42	P46	C16	P56	M4	246
I/O, PGCK2	P35	P43	P47	B17	P57	R2	247
I/O (HDC)	P36	P44	P48	E16	P58	P3	250
I/O	-	P45	P49	C17	P59	L5	253
I/O	-	P46	P50	D17	P60	N4	256
I/O	-	P47	P51	B18	P61	R3	259
I/O ($\overline{\text{LDC}}$)	P37	P48	P52	E17	P62	P4	262
I/O	-	P49	P53	F16	P63	K7	265
I/O	-	P50	P54	C18	P64	M5	268
I/O	-	-	-	D18	P65	R4	271
I/O	-	-	-	F17	P66	N5	274
GND	-	P51	P55	G16	P67	GND*	-
I/O	-	P52	P56	E18	P68	R5	277

XC4013E/L Pad Name	PQ 160	PQ/ HQ 208	PG 223	BG 225	PQ/ HQ 240	Bndry Scan
I/O	-	-	E15	P5	P73	325
I/O	-	-	F15	L6	P74	328
GND	P51	P67	G16	GND*	P75	-
I/O	P52	P68	E18	R5	P76	331
I/O	P53	P69	F18	M6	P77	334
I/O	P54	P70	G17	N6	P78	337
I/O	P55	P71	G18	P6	P79	340
VCC	-	-	-	VCC*	P80	-
I/O	-	P72	H16	R6	P81	343
I/O	-	P73	H17	M7	P82	346
I/O	-	-	G15	N7	P84	349
I/O	-	-	H15	P7	P85	352
I/O	P56	P74	H18	R7	P86	355
I/O	P57	P75	J18	L7	P87	358
I/O	P58	P76	J17	N8	P88	361
I/O ($\overline{\text{INIT}}$)	P59	P77	J16	P8	P89	364
VCC	P60	P78	J15	R8	P90	-
GND	P61	P79	K15	M8	P91	-
I/O	P62	P80	K16	L8	P92	367
I/O	P63	P81	K17	P9	P93	370
I/O	P64	P82	K18	R9	P94	373
I/O	P65	P83	L18	N9	P95	376
I/O	-	P84	L17	M9	P96	379
I/O	-	P85	L16	L9	P97	382
I/O	-	-	L15	R10	P99	385
I/O	-	-	M15	P10	P100	388
VCC	-	-	-	VCC*	P101	-
I/O	P66	P86	M18	N10	P102	391
I/O	P67	P87	M17	K9	P103	394
I/O	P68	P88	N18	R11	P104	397
I/O	P69	P89	P18	P11	P105	400
GND	P70	P90	M16	GND*	P106	-
I/O	-	-	N15	M10	P107	403
I/O	-	-	P15	N11	P108	406
I/O	-	P91	N17	R12	P109	409
I/O	-	P92	R18	L10	P110	412
I/O	P71	P93	T18	P12	P111	415
I/O	P72	P94	P17	M11	P112	418
I/O	P73	P95	N16	R13	P113	421
I/O	P74	P96	T17	N12	P114	424
I/O	P75	P97	R17	P13	P115	427
I/O	P76	P98	P16	K10	P116	430
I/O	P77	P99	U18	R14	P117	433
I/O, SGCK3	P78	P100	T16	N13	P118	436
GND	P79	P101	R16	GND*	P119	-
DONE	P80	P103	U17	P14	P120	-
VCC	P81	P106	R15	R15	P121	-
$\overline{\text{PROGRAM}}$	P82	P108	V18	M12	P122	-
I/O (D7)	P83	P109	T15	P15	P123	439
I/O, PGCK3	P84	P110	U16	N14	P124	442
I/O	P85	P111	T14	L11	P125	445
I/O	P86	P112	U15	M13	P126	448
I/O	-	-	R14	N15	P127	451

XC4013E/L Pad Name	PQ 160	PQ/ HQ 208	PG 223	BG 225	PQ/ HQ 240	Bndry Scan
I/O	-	-	R13	M14	P128	454
I/O (D6)	P87	P113	V17	J10	P129	457
I/O	P88	P114	V16	L12	P130	460
I/O	P89	P115	T13	M15	P131	463
I/O	P90	P116	U14	L13	P132	466
I/O	-	P117	V15	L14	P133	469
I/O	-	P118	V14	K11	P134	472
GND	P91	P119	T12	GND*	P135	-
I/O	-	-	R12	L15	P136	475
I/O	-	-	R11	K12	P137	478
I/O	P92	P120	U13	K13	P138	481
I/O	P93	P121	V13	K14	P139	484
VCC	-	-	-	VCC*	P140	-
I/O (D5)	P94	P122	U12	K15	P141	487
I/O ($\overline{\text{CS0}}$)	P95	P123	V12	J12	P142	490
I/O	-	P124	T11	J13	P144	493
I/O	-	P125	U11	J14	P145	496
I/O	P96	P126	V11	J15	P146	499
I/O	P97	P127	V10	J11	P147	502
I/O (D4)	P98	P128	U10	H13	P148	505
I/O	P99	P129	T10	H14	P149	508
VCC	P100	P130	R10	H15	P150	-
GND	P101	P131	R9	GND*	P151	-
I/O (D3)	P102	P132	T9	H12	P152	511
I/O ($\overline{\text{RS}}$)	P103	P133	U9	H11	P153	514
I/O	P104	P134	V9	G14	P154	517
I/O	P105	P135	V8	G15	P155	520
I/O	-	P136	U8	G13	P156	523
I/O	-	P137	T8	G12	P157	526
I/O (D2)	P106	P138	V7	G11	P159	529
I/O	P107	P139	U7	F15	P160	532
VCC	-	-	-	VCC*	P161	-
I/O	P108	P140	V6	F14	P162	535
I/O	P109	P141	U6	F13	P163	538
I/O	-	-	R8	G10	P164	541
I/O	-	-	R7	E15	P165	544
GND	P110	P142	T7	GND*	P166	-
I/O	-	-	R6	E14	P167	547
I/O	-	-	R5	F12	P168	550
I/O	-	P143	V5	E13	P169	553
I/O	-	P144	V4	D15	P170	556
I/O	P111	P145	U5	F11	P171	559
I/O	P112	P146	T6	D14	P172	562
I/O (D1)	P113	P147	V3	E12	P173	565
I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	P114	P148	V2	C15	P174	568
I/O	P115	P149	U4	D13	P175	571
I/O	P116	P150	T5	C14	P176	574
I/O (D0, DIN)	P117	P151	U3	F10	P177	577
I/O, SGCK4 (DOUT)	P118	P152	T4	B15	P178	580
CCLK	P119	P153	V1	C13	P179	-
VCC	P120	P154	R4	B14	P180	-

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
I/O, GCK5	P149	AP34	AG4	658
I/O	P148	AW39	AG3	661
I/O	P147	AN31	AH2	664
I/O	-	AV36	AH1	667
I/O	-	AR33	AF4	670
I/O	P146	AP32	AF3	673
I/O	P145	AU35	AG2	676
I/O	P144	AW33	AE3	679
I/O	P143	AU33	AF2	682
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O (D6)	P142	AV32	AF1	685
I/O	P141	AU31	AD4	688
I/O	P140	AR31	AD3	691
I/O	P139	AP28	AE2	694
I/O	P138	AT32	AC3	697
I/O	P137	AV30	AD1	700
I/O	P136	AR29	AC2	703
I/O	P135	AP26	AB4	706
GND	P134	GND*	GND*	-
I/O	P133	AU29	AB3	709
I/O	P132	AV28	AB2	712
I/O, FCLK3	P131	AT28	AB1	715
I/O	P130	AR25	AA3	718
VCC	P129	VCC*	VCC*	-
I/O (D5)	P127	AP24	AA2	721
I/O ($\overline{CS0}$)	P126	AU27	Y2	724
I/O	-	AR27	Y4	727
I/O	-	AW27	Y3	730
I/O	P125	AT24	W4	733
I/O	P124	AR23	W3	736
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O	P123	AP22	V4	739
I/O	P122	AV24	V3	742
I/O	P121	AU23	U1	745
I/O	P120	AT22	U2	748
I/O	P119	AR21	U4	751
I/O	P118	AV22	U3	754
I/O (D4)	P117	AP20	T1	757
I/O	P116	AU21	T2	760
VCC	P115	VCC*	VCC*	-
GND	P114	GND*	GND*	-
I/O (D3)	P113	AU19	T3	763
I/O ($\overline{RS}$)	P112	AV20	R1	766
I/O	P111	AV18	R2	769
I/O	P110	AR19	R4	772

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
I/O	P109	AT18	R3	775
I/O	P108	AW17	P2	778
I/O	P107	AV16	P3	781
I/O	P106	AP18	P4	784
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O	P105	AR17	N3	787
I/O	P104	AT16	N4	790
I/O	-	AV14	M1	793
I/O	-	AW13	M2	796
I/O (D2)	P103	AR15	L2	799
I/O	P102	AP16	L3	802
VCC	P101	VCC*	VCC*	-
I/O	P99	AV12	K1	805
I/O, FCLK4	P98	AR13	K2	808
I/O	P97	AU11	K3	811
I/O	P96	AT12	K4	814
GND	P95	GND*	GND*	-
I/O	P94	AP14	J2	817
I/O	P93	AR11	J3	820
I/O	P92	AV10	J4	823
I/O	P91	AT8	H1	826
I/O	P90	AT10	H2	829
I/O	P89	AP10	H3	832
I/O	P88	AP12	H4	835
I/O	P87	AR9	G2	838
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O (D1)	P86	AU7	G4	841
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	P85	AW7	F2	844
I/O	-	AW5	F3	847
I/O	-	AV6	E1	850
I/O	P84	AR7	E3	853
I/O	P83	AV4	D1	856
I/O	P82	AN9	E4	859
I/O	P81	AW1	D2	862
I/O (D0, DIN)	P80	AP6	C2	865
I/O, GCK6 (DOUT)	P79	AU3	D3	868
CCLK	P78	AR5	D4	-
VCC	P77	VCC*	VCC*	-
O, TDO	P76	AN7	C4	0
GND	P75	GND*	GND*	-
I/O (A0, $\overline{WS}$)	P74	AT4	B3	2
I/O, GCK7 (A1)	P73	AV2	D5	5
I/O	P72	AM8	B4	8
I/O	P71	AL7	C5	11

PG156 Pin	XC4005E	XC4006E
F1	I/O (A10)	I/O (A10)
F2	I/O (A11)	I/O (A11)
F3	GND	GND
F14	GND	GND
F15	I/O	I/O
F16	I/O	I/O
E1	I/O	I/O
E2	I/O	I/O
E3	I/O (A12)	I/O (A12)
E14	I/O	I/O
E15	N.C.	I/O
E16	I/O	I/O
D1	N.C.	I/O
D2	N.C.	I/O
D3	I/O	I/O
D14	I/O (HDC)	I/O (HDC)
D15	I/O	I/O
D16	N.C.	I/O
C1	I/O (A13)	I/O (A13)
C2	I/O	I/O
C3	VCC	VCC
C4	GND	GND
C5	I/O	I/O
C6	GND	GND
C7	I/O	I/O
C8	GND	GND
C9	I/O	I/O
C10	I/O	I/O
C11	GND	GND
C12	I/O	I/O
C13	GND	GND
C14	VCC	VCC
C15	I/O	I/O
C16	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
B1	I/O (A14)	I/O (A14)
B2	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
B3	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
B4	I/O, TDI	I/O, TDI
B5	I/O	I/O
B6	I/O	I/O
B7	I/O	I/O
B8	VCC	VCC
B9	I/O	I/O
B10	I/O	I/O
B11	I/O	I/O
B12	I/O	I/O
B13	I/O	I/O
B14	I/O, SCGK2	I/O, SCGK2
B15	I (M2)	I (M2)
B16	I/O, PGCK2	I/O, PGCK2
A1	I/O (A17)	I/O (A17)
A2	I/O	I/O
A3	I/O, TCK	I/O, TCK
A4	N.C.	I/O
A5	I/O, TMS	I/O, TMS
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	I/O	I/O
A12	N.C.	I/O
A13	I/O	I/O
A14	I/O	I/O
A15	O (M1)	O (M1)
A16	I (M0)	I (M0)

2/28/96

Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

PQ160 Package Pinouts

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

PQ 160 Pin	XC4005E	XC4006E	XC4008E	XC4010E	XC4013E
P1	GND	GND	GND	GND	GND
P2	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
P3	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)
P4	I/O	I/O	I/O	I/O	I/O
P5	I/O	I/O	I/O	I/O	I/O
P6	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI
P7	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK
P8	N.C.	I/O	I/O	I/O	I/O
P9	N.C.	I/O	I/O	I/O	I/O
P10	GND	GND	GND	GND	GND
P11	I/O	I/O	I/O	I/O	I/O
P12	I/O	I/O	I/O	I/O	I/O
P13	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS
P14	I/O	I/O	I/O	I/O	I/O
P15	I/O	I/O	I/O	I/O	I/O
P16	I/O	I/O	I/O	I/O	I/O
P17	I/O	I/O	I/O	I/O	I/O
P18	I/O	I/O	I/O	I/O	I/O
P19	GND	GND	GND	GND	GND
P20	VCC	VCC	VCC	VCC	VCC
P21	I/O	I/O	I/O	I/O	I/O
P22	I/O	I/O	I/O	I/O	I/O
P23	I/O	I/O	I/O	I/O	I/O
P24	I/O	I/O	I/O	I/O	I/O
P25	I/O	I/O	I/O	I/O	I/O
P26	I/O	I/O	I/O	I/O	I/O
P27	I/O	I/O	I/O	I/O	I/O
P28	I/O	I/O	I/O	I/O	I/O
P29	GND	GND	GND	GND	GND
P30	N.C.	I/O	I/O	I/O	I/O
P31	N.C.	I/O	I/O	I/O	I/O
P32	I/O	I/O	I/O	I/O	I/O
P33	I/O	I/O	I/O	I/O	I/O
P34	I/O	I/O	I/O	I/O	I/O
P35	I/O	I/O	I/O	I/O	I/O
P36	I/O	I/O	I/O	I/O	I/O
P37	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2
P38	O (M1)	O (M1)	O (M1)	O (M1)	O (M1)
P39	GND	GND	GND	GND	GND
P40	I (M0)	I (M0)	I (M0)	I (M0)	I (M0)
P41	VCC	VCC	VCC	VCC	VCC
P42	I (M2)	I (M2)	I (M2)	I (M2)	I (M2)
P43	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2
P44	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)
P45	I/O	I/O	I/O	I/O	I/O
P46	I/O	I/O	I/O	I/O	I/O
P47	I/O	I/O	I/O	I/O	I/O
P48	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
P49	N.C.	I/O	I/O	I/O	I/O
P50	N.C.	I/O	I/O	I/O	I/O
P51	GND	GND	GND	GND	GND
P52	I/O	I/O	I/O	I/O	I/O
P53	I/O	I/O	I/O	I/O	I/O
P54	I/O	I/O	I/O	I/O	I/O
P55	I/O	I/O	I/O	I/O	I/O
P56	I/O	I/O	I/O	I/O	I/O
P57	I/O	I/O	I/O	I/O	I/O
P58	I/O	I/O	I/O	I/O	I/O
P59	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
P60	VCC	VCC	VCC	VCC	VCC
P61	GND	GND	GND	GND	GND
P62	I/O	I/O	I/O	I/O	I/O
P63	I/O	I/O	I/O	I/O	I/O
P64	I/O	I/O	I/O	I/O	I/O
P65	I/O	I/O	I/O	I/O	I/O
P66	I/O	I/O	I/O	I/O	I/O
P67	I/O	I/O	I/O	I/O	I/O
P68	I/O	I/O	I/O	I/O	I/O
P69	I/O	I/O	I/O	I/O	I/O
P70	GND	GND	GND	GND	GND
P71	N.C.	I/O	I/O	I/O	I/O
P72	N.C.	I/O	I/O	I/O	I/O
P73	I/O	I/O	I/O	I/O	I/O
P74	I/O	I/O	I/O	I/O	I/O
P75	I/O	I/O	I/O	I/O	I/O
P76	I/O	I/O	I/O	I/O	I/O
P77	I/O	I/O	I/O	I/O	I/O
P78	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3
P79	GND	GND	GND	GND	GND
P80	DONE	DONE	DONE	DONE	DONE
P81	VCC	VCC	VCC	VCC	VCC
P82	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$
P83	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)
P84	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3
P85	I/O	I/O	I/O	I/O	I/O
P86	I/O	I/O	I/O	I/O	I/O
P87	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)
P88	I/O	I/O	I/O	I/O	I/O
P89	N.C.	I/O	I/O	I/O	I/O
P90	N.C.	I/O	I/O	I/O	I/O

TQ176 Package Pinouts

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

TQ176 Pin	XC4010L
P1	GND
P2	I/O, PGCK1 (A16)
P3	I/O (A17)
P4	I/O
P5	I/O
P6	I/O, TDI
P7	I/O, TCK
P8	I/O
P9	I/O
P10	GND
P11	I/O
P12	I/O
P13	I/O, TMS
P14	I/O
P15	I/O
P16	I/O
P17	I/O
P18	I/O
P19	I/O
P20	I/O
P21	GND
P22	VCC
P23	I/O
P24	I/O
P25	I/O
P26	I/O
P27	I/O
P28	I/O
P29	I/O
P30	I/O
P31	I/O
P32	I/O
P33	GND
P34	I/O
P35	I/O
P36	I/O
P37	I/O
P38	I/O
P39	I/O
P40	I/O
P41	I/O, SCGK2
P42	O (M1)
P43	GND
P44	I (M0)
P45	VCC
P46	I (M2)
P47	I/O, PGCK2
P48	I/O (HDC)
P49	I/O
P50	I/O
P51	I/O
P52	I/O ($\overline{\text{LDC}}$)
P53	I/O
P54	I/O
P55	GND
P56	I/O
P57	I/O
P58	I/O
P59	I/O
P60	I/O
P61	I/O
P62	I/O
P63	I/O
P64	I/O
P65	I/O ($\overline{\text{INIT}}$)
P66	VCC
P67	GND
P68	I/O
P69	I/O
P70	I/O
P71	I/O
P72	I/O
P73	I/O
P74	I/O
P75	I/O
P76	I/O
P77	I/O
P78	GND
P79	I/O
P80	I/O
P81	I/O
P82	I/O
P83	I/O
P84	I/O
P85	I/O
P86	I/O, SGCK3
P87	GND
P88	DONE
P89	VCC
P90	$\overline{\text{PROGRAM}}$

PG299 Package Pinouts

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

PG299 Pin	XC4025E	XC4028EX/XL
X1	I/O, SGCK4 (DOUT)	I/O, GCK6 (DOUT)
X2	GND	GND
X3	I/O	I/O
X4	I/O	I/O
X5	VCC	VCC
X6	GND	GND
X7	I/O	I/O
X8	I/O	I/O
X9	I/O	I/O
X10	VCC	VCC
X11	GND	GND
X12	I/O	I/O
X13	I/O	I/O
X14	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)
X15	VCC	VCC
X16	GND	GND
X17	I/O	I/O
X18	I/O	I/O
X19	VCC	VCC
X20	I/O, SGCK3	I/O, GCK4
W1	VCC	VCC
W2	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W6	I/O	I/O
W7	I/O	I/O, FCLK4
W8	I/O (D2)	I/O (D2)
W9	I/O	I/O
W10	I/O (D3)	I/O (D3)
W11	I/O	I/O
W12	I/O	I/O
W13	I/O	I/O
W14	I/O	I/O, FCLK3
W15	I/O	I/O
W16	I/O	I/O
W17	I/O (D6)	I/O (D6)
W18	I/O, PGCK3	I/O, GCK5
W19	I/O (D7)	I/O (D7)
W20	GND	GND
V1	I/O (A3)	I/O (A3)
V2	I/O, PGCK4 (A1)	I/O, GCK7 (A1)
V3	CCLK	CCLK
V4	I/O (D0, DIN)	I/O (D0, DIN)
V5	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
V6	I/O	I/O
V7	I/O	I/O
V8	I/O	I/O
V9	I/O	I/O
V10	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
V11	I/O (D4)	I/O (D4)
V12	I/O	I/O
V13	I/O	I/O
V14	I/O	I/O
V15	I/O	I/O
V16	I/O	I/O
V17	I/O	I/O
V18	DONE	DONE
V19	I/O	I/O
V20	I/O	I/O
U1	I/O	I/O
U2	I/O	I/O
U3	I/O (CS1, A2)	I/O (CS1, A2)
U4	O, TDO	O, TDO
U5	I/O	I/O
U6	I/O (D1)	I/O (D1)
U7	I/O	I/O
U8	I/O	I/O
U9	I/O	I/O
U10	I/O	I/O
U11	I/O	I/O
U12	I/O	I/O
U13	I/O	I/O
U14	I/O	I/O
U15	I/O	I/O
U16	I/O	I/O
U17	$\overline{PROGRAM}$	$\overline{PROGRAM}$
U18	I/O	I/O
U19	I/O	I/O
U20	I/O	I/O
T1	GND	GND
T2	I/O	I/O
T3	I/O	I/O
T4	I/O	I/O
T5	GND	GND
T6	I/O	I/O
T7	I/O	I/O
T8	I/O	I/O
T9	I/O	I/O
T10	I/O	I/O
T11	I/O	I/O
T12	I/O (D5)	I/O (D5)
T13	I/O	I/O
T14	I/O	I/O
T15	I/O	I/O
T16	VCC	VCC
T17	I/O	I/O
T18	I/O	I/O
T19	I/O	I/O
T20	VCC	VCC

PG299 Pin	XC4025E	XC4028EX/XL
E7	I/O	I/O
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	I/O	I/O
E14	I/O	I/O
E15	I/O	I/O
E16	GND	GND
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	GND	GND
D1	I/O	I/O
D2	I/O	I/O
D3	I/O (A14)	I/O (A14)
D4	I/O, PGCK1 (A16)	I/O, GCK1 (A16)
D5	I/O, TDI	I/O, TDI
D6	I/O	I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	I/O
D13	I/O	I/O, FCLK2
D14	I/O	I/O
D15	I/O	I/O
D16	I/O	I/O
D17	I (M2)	I (M2)
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
C1	I/O (A13)	I/O (A13)
C2	I/O	I/O
C3	I/O, SGCK1 (A15)	I/O, GCK8 (A15)
C4	I/O, TCK	I/O, TCK
C5	I/O	I/O
C6	I/O	I/O
C7	I/O, TMS	I/O, TMS
C8	I/O	I/O
C9	I/O	I/O
C10	I/O	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	I/O	I/O
C14	I/O	I/O
C15	I/O	I/O
C16	I/O	I/O
C17	I/O, SGCK2	I/O, GCK2
C18	I (M0)	I (M0)
C19	I/O (HDC)	I/O (HDC)
C20	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
B1	GND	GND
B2	I/O (A17)	I/O (A17)
B3	I/O	I/O
B4	I/O	I/O
B5	I/O	I/O
B6	I/O	I/O, FCLK1
B7	I/O	I/O
B8	I/O	I/O
B9	I/O	I/O
B10	I/O	I/O
B11	I/O	I/O
B12	I/O	I/O
B13	I/O	I/O
B14	I/O	I/O
B15	I/O	I/O
B16	I/O	I/O
B17	I/O	I/O
B18	I/O	I/O
B19	I/O, PGCK2	I/O, GCK3
B20	VCC	VCC
A2	VCC	VCC
A3	I/O	I/O
A4	I/O	I/O
A5	GND	GND
A6	VCC	VCC
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	GND	GND
A11	VCC	VCC
A12	I/O	I/O
A13	I/O	I/O
A14	I/O	I/O
A15	GND	GND
A16	VCC	VCC
A17	I/O	I/O
A18	I/O	I/O
A19	GND	GND
A20	O (M1)	O (M1)

3/18/96

Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.