AMD Xilinx - XC4005L-5PQ208C Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	196
Number of Logic Elements/Cells	466
Total RAM Bits	6272
Number of I/O	112
Number of Gates	5000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc4005l-5pq208c

Detailed Functional Description

XC4000-Series devices achieve high speed through advanced semiconductor technology and improved architecture. The XC4000E and XC4000EX support system clock rates of up to 66 MHz and internal performance in excess of 150 MHz. Compared to older Xilinx FPGA families, XC4000-Series devices are more powerful. They offer on-chip edge-triggered and dual-port RAM, clock enables on I/O flip-flops, and wide-input decoders. They are more versatile in many applications, especially those involving RAM. Design cycles are faster due to a combination of increased routing resources and more sophisticated software.

Basic Building Blocks

Xilinx user-programmable gate arrays include two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing the user's logic.
- IOBs provide the interface between the package pins and internal signal lines.

Three other types of circuits are also available:

- 3-State buffers (TBUFs) driving horizontal longlines are associated with each CLB.
- Wide edge decoders are available around the periphery of each device.
- An on-chip oscillator is provided.

Programmable interconnect resources provide routing paths to connect the inputs and outputs of these configurable elements to the appropriate networks.

The functionality of each circuit block is customized during configuration by programming internal static memory cells. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA.

Each of these available circuits is described in this section.

Configurable Logic Blocks (CLBs)

Configurable Logic Blocks implement most of the logic in an FPGA. The principal CLB elements are shown in Figure 1. The number of CLBs needed to implement selected soft macros is shown in Table 3.

Two 4-input function generators (F and G) offer unrestricted versatility. Most combinatorial logic functions need four or fewer inputs. However, a third function generator (H) is provided. The H function generator has three inputs. Either zero, one, or both of these inputs can be the outputs of F and G; the other input(s) are from outside the CLB. The CLB can, therefore, implement certain functions of up to nine variables, like parity check or expandable-identity comparison of two sets of four inputs.

Each CLB contains two storage elements that can be used to store the function generator outputs. However, the storage elements and function generators can also be used independently. These storage elements can be configured as flip-flops in both XC4000E and XC4000EX devices; in the XC4000EX they can optionally be configured as latches. DIN can be used as a direct input to either of the two storage elements. H1 can drive the other through the H function generator. Function generator outputs can also drive two outputs independent of the storage element outputs. This versatility increases logic capacity and simplifies routing.

Thirteen CLB inputs and four CLB outputs provide access to the function generators and storage elements. These inputs and outputs connect to the programmable interconnect resources outside the block.

Function Generators

Four independent inputs are provided to each of two function generators (F1 - F4 and G1 - G4). These function generators, with outputs labeled F' and G', are each capable of implementing any arbitrarily defined Boolean function of four inputs. The function generators are implemented as memory look-up tables. The propagation delay is therefore independent of the function implemented.

A third function generator, labeled H', can implement any Boolean function of its three inputs. Two of these inputs can optionally be the F' and G' functional generator outputs. Alternatively, one or both of these inputs can come from outside the CLB (H2, H0). The third input must come from outside the block (H1).

Signals from the function generators can exit the CLB on two outputs. F' or H' can be connected to the X output. G' or H' can be connected to the Y output.

A CLB can be used to implement any of the following functions:

- any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables[1]
- any single function of five variables
- any function of four variables together with some functions of six variables
- some functions of up to nine variables.

1. When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.

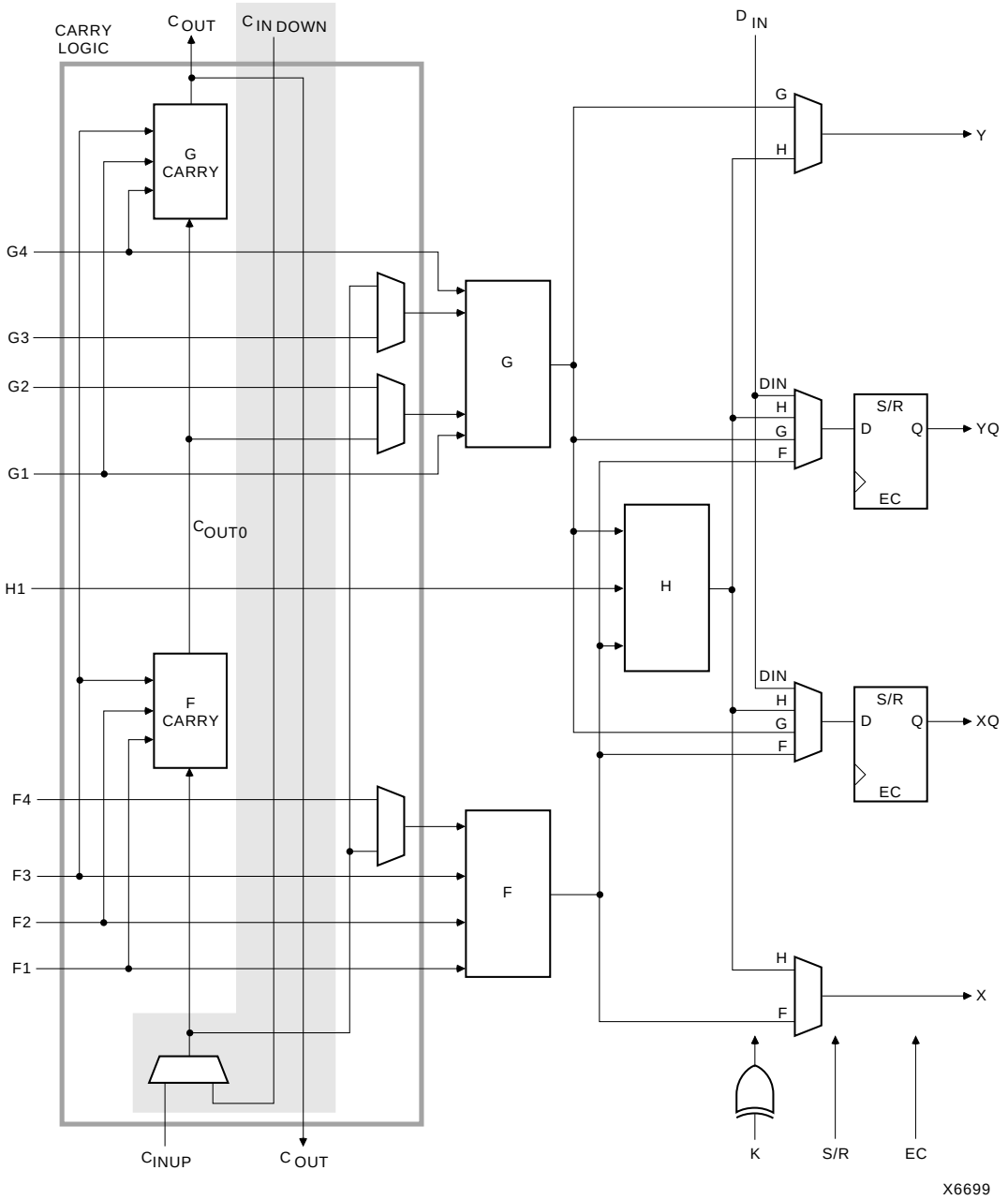


Figure 13: Fast Carry Logic in XC4000E CLB (shaded area not present in XC4000EX)

Optional Delay Guarantees Zero Hold Time

The data input to the register can optionally be delayed by several nanoseconds. With the delay enabled, the setup time of the input flip-flop is increased so that normal clock routing does not result in a positive hold-time requirement. A positive hold time requirement can lead to unreliable, temperature- or processing-dependent operation.

The input flip-flop setup time is defined between the data measured at the device I/O pin and the clock input at the IOB (not at the clock pin). Any routing delay from the device clock pin to the clock input of the IOB must, therefore, be subtracted from this setup time to arrive at the real setup time requirement relative to the device pins. A short specified setup time might, therefore, result in a negative setup time at the device pins, i.e., a positive hold-time requirement.

When a delay is inserted on the data line, more clock delay can be tolerated without causing a positive hold-time requirement. Sufficient delay eliminates the possibility of a data hold-time requirement at the external pin. The maximum delay is therefore inserted as the default.

The XC4000E IOB has a one-tap delay element: either the delay is inserted (default), or it is not. The delay guarantees a zero hold time with respect to clocks routed through any of the XC4000E global clock buffers. (See "Global Nets and Buffers (XC4000E only)" on page 41 for a description of the global clock buffers in the XC4000E.) For a shorter input register setup time, with non-zero hold, attach a NODELAY attribute or property to the flip-flop.

The XC4000EX IOB has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The attributes or properties used to select the desired delay are shown in Table 12. The choices are no added attribute, MEDDELAY, and NODELAY. The default setting, with no added attribute, ensures no hold time with respect to any of the XC4000EX clock buffers, including the Global Low-Skew buffers. MEDDELAY ensures no hold time with respect to the Global Early and FastCLK buffers. Inputs with NODELAY may have a positive hold time with respect to all clock buffers, including the FastCLK buffers. For a description of each of these buffers, see "Global Nets and Buffers (XC4000EX only)" on page 43.

Table 12: XC4000EX IOB Input Delay Element

Value	When to Use
full delay (default, no attribute added)	Zero Hold with respect to Global Low-Skew Buffer, Global Early Buffer, or FastCLK Buffer
MEDDELAY	Zero Hold with respect to Global Early Buffer or FastCLK Buffer
NODELAY	Short Setup, positive Hold time

Additional Input Latch for Fast Capture (XC4000EX only)

The XC4000EX IOB has an additional optional latch on the input. This latch, as shown in Figure 17, is clocked by the output clock — the clock used for the output flip-flop — rather than the input clock. Therefore, two different clocks can be used to clock the two input storage elements. This additional latch allows the very fast capture of input data, which is then synchronized to the internal clock by the IOB flip-flop or latch.

To use this Fast Capture technique, drive the output clock pin (the Fast Capture latching signal) from the output of one of the Global Early or FastCLK buffers supplied in the XC4000EX. The second storage element should be clocked by a Global Low-Skew buffer, to synchronize the incoming data to the internal logic. (See Figure 18.) These special buffers are described in "Global Nets and Buffers (XC4000EX only)" on page 43.

The Fast Capture latch is designed primarily for use with a Global Early buffer. For Fast Capture, a single clock signal is routed through both a Global Early buffer and a Global Low-Skew buffer. (The two buffers share an input pad.) The Fast Capture latch is clocked by the Global Early buffer, and the standard IOB flip-flop or latch is clocked by the Global Low-Skew buffer. This mode is the safest way to use the Fast Capture latch, because the clock buffers on both storage elements are driven by the same pad. There is no external skew between clock pads to create potential problems.

Alternatively, a FastCLK buffer can be used to minimize the setup time of device inputs, if a positive hold time is acceptable. Use the FastCLK buffer to clock the Fast Capture latch, and a slower clock buffer to clock the standard IOB flip-flop or latch. Either the Global Early buffer or the Global Low-Skew buffer can be used for the second storage ele-

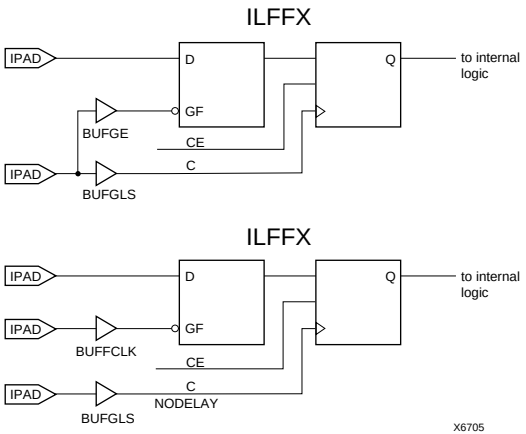


Figure 18: Examples Using XC4000EX Fast Capture Latch

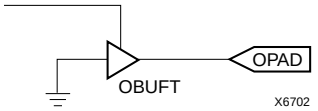


Figure 19: Open-Drain Output

An output can be configured as open-drain (open-collector) by placing an OBUFT symbol in a schematic or HDL code, then tying the 3-state pin (T) to the output signal, and the input pin (I) to Ground. (See Figure 19.)

Output Slew Rate

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop.

For XC4000E devices, maximum total capacitive load for simultaneous fast mode switching in the same direction is 200 pF for all package pins between each Power/Ground pin pair. For XC4000EX devices, additional internal Power/Ground pin pairs are connected to special Power and Ground planes within the packages, to reduce ground bounce. Therefore, the maximum total capacitive load is 300 pF between each external Power/Ground pin pair. Maximum loading may vary for the low-voltage devices.

For slew-rate limited outputs this total is two times larger for each device type: 400 pF for XC4000E devices and 600 pF for XC4000EX devices. This maximum capacitive load should not be exceeded, as it can result in ground bounce of greater than 1.5 V amplitude and more than 5 ns duration. This level of ground bounce may cause undesired transient behavior on an output, or in the internal logic. This restriction is common to all high-speed digital ICs, and is not particular to Xilinx or the XC4000 Series.

XC4000-Series devices have a feature called “Soft Start-up,” designed to reduce ground bounce when all outputs are turned on simultaneously at the end of configuration. When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. Immediately following the initial activation of the I/O, the slew rate of the individual outputs is determined by the individual configuration option for each IOB.

Global Three-State

A separate Global 3-State line (not shown in Figure 16 or Figure 17) forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. This global net (GTS) does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-State signal. Using GTS is similar to GSR. See Figure 2 on page 13 for details.

Alternatively, GTS can be driven from any internal node.

Output Multiplexer/2-Input Function Generator (XC4000EX only)

As shown in Figure 17 on page 25, the output path in the XC4000EX IOB contains an additional multiplexer not available in the XC4000E IOB. The multiplexer can also be configured as a 2-input function generator, implementing a pass-gate, AND-gate, OR-gate, or XOR-gate, with 0, 1, or 2 inverted inputs. The logic used to implement these functions is shown in the upper gray area of Figure 17.

When configured as a multiplexer, this feature allows two output signals to time-share the same output pad; effectively doubling the number of device outputs without requiring a larger, more expensive package.

When the MUX is configured as a 2-input function generator, logic can be implemented within the IOB itself. Combined with either a FastCLK or Global Early buffer, this arrangement allows very high-speed gating of a single signal. For example, a wide decoder can be implemented in CLBs, and its output gated with a Read or Write Strobe driven by a FastCLK buffer, as shown in Figure 20. The critical-path pin-to-pin delay of this circuit is less than 6 nanoseconds. (This value may not be achievable in XC4000XL devices.)

As shown in Figure 17, the IOB input pins Out, Output Clock, and Clock Enable have different delays and different flexibilities regarding polarity. Additionally, Output Clock sources are more limited than the other inputs. Therefore, the Xilinx software does not move logic into the IOB function generators unless explicitly directed to do so.

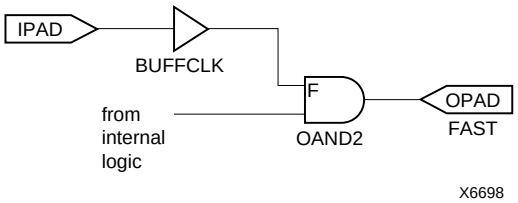


Figure 20: Fast Pin-to-Pin Path in XC4000E

Longlines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array. Longlines are intended for high fan-out, time-critical signal nets, or nets that are distributed over long distances. In XC4000EX devices, quad lines are preferred for critical nets, because the buffered switch matrices make them faster for high fan-out nets.

Two horizontal longlines per CLB can be driven by 3-state or open-drain drivers (TBUFs). They can therefore implement unidirectional or bidirectional buses, wide multiplexers, or wired-AND functions. (See "Three-State Buffers" on page 29 for more details.)

Each horizontal longline driven by TBUFs has either two (XC4000E) or eight (XC4000EX) pull-up resistors. To activate these resistors, attach a PULLUP symbol to the longline net. The software automatically activates the appropriate number of pull-ups. There is also a weak keeper at each end of these two horizontal longlines. This circuit prevents undefined floating levels. However, it is overridden by any driver, even a pull-up resistor.

Each XC4000E longline has a programmable splitter switch at its center, as does each XC4000EX longline driven by TBUFs. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Each XC4000EX longline not driven by TBUFs has a buffered programmable splitter switch at the 1/4, 1/2, and 3/4 points of the array. Due to the buffering, XC4000EX longline performance does not deteriorate with the larger array sizes. If the longline is split, the resulting partial longlines are independent.

Routing connectivity of the longlines is shown in Figure 27 on page 34.

Direct Interconnect (XC4000EX only)

The XC4000EX offers two direct, efficient and fast connections between adjacent CLBs. These nets facilitate a data flow from the left to the right side of the device, or from the top to the bottom, as shown in Figure 31. Signals routed on the direct interconnect exhibit minimum interconnect propagation delay and use no general routing resources.

The direct interconnect is also present between CLBs and adjacent IOBs. Each IOB on the left and top device edges has a direct path to the nearest CLB. Each CLB on the right and bottom edges of the array has a direct path to the nearest two IOBs, since there are two IOBs for each row or column of CLBs.

The place and route software uses direct interconnect whenever possible, to maximize routing resources and minimize interconnect delays.

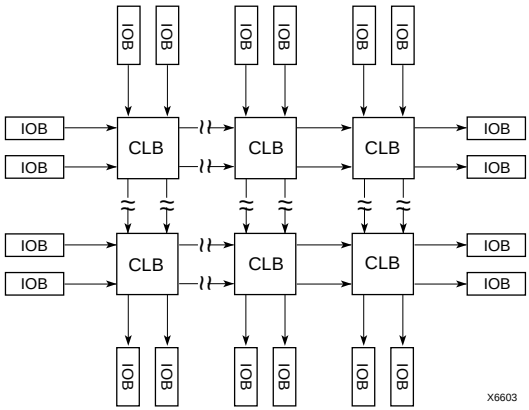


Figure 31: XC4000EX Direct Interconnect

Octal I/O Routing (XC4000EX only)

Between the XC4000EX CLB array and the pad ring, eight interconnect tracks provide for versatility in pin assignment and fixed pinout flexibility. (See Figure 34.)

These routing tracks are called octals, because they can be broken every eight CLBs (sixteen IOBs) by a programmable buffer that also functions as a splitter switch. The buffers are staggered, so each line goes through a buffer at every eighth CLB location around the device edge.

The octal lines bend around the corners of the device. The lines cross at the corners in such a way that the segment most recently buffered before the turn has the farthest distance to travel before the next buffer, as shown in Figure 34.

IOB inputs and outputs interface with the octal lines via the single-length interconnect lines. Single-length lines are also used for communication between the octals and double-length lines, quads, and longlines within the CLB array.

Segmentation into buffered octals was found to be optimal for distributing signals over long distances around the device.

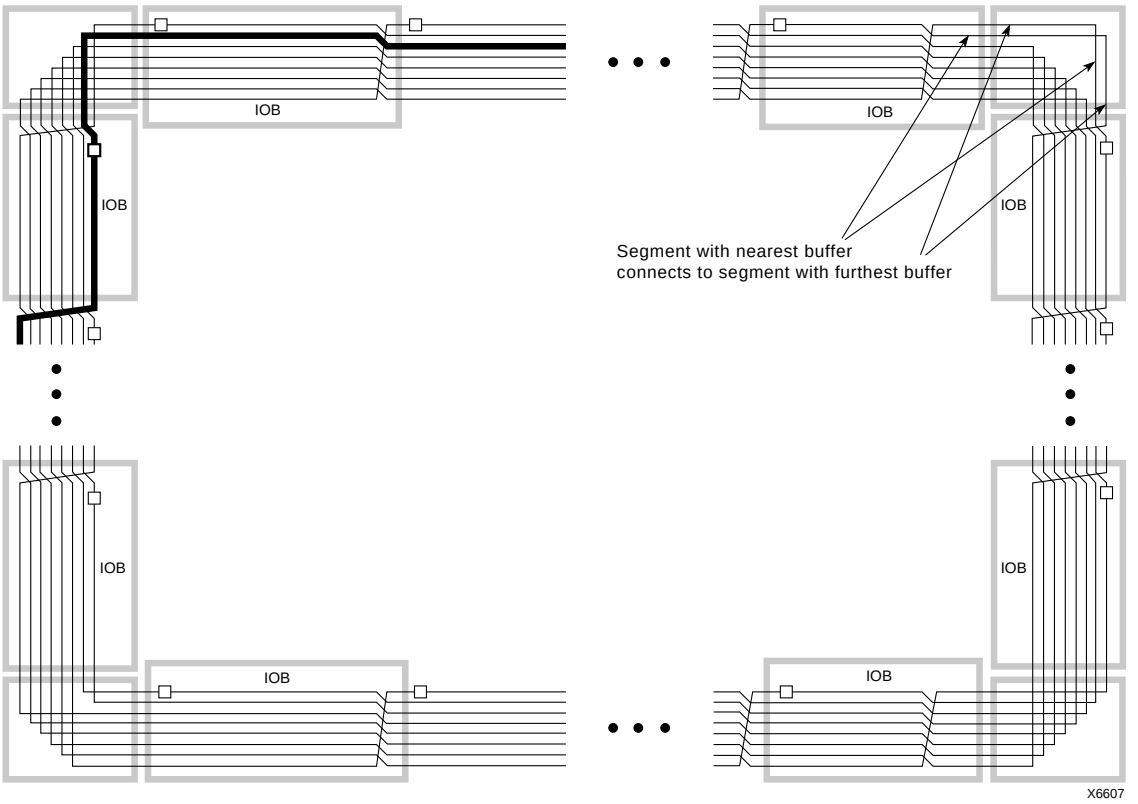


Figure 34: XC4000EX Octal I/O Routing

Power Distribution

Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated Vcc and Ground ring surrounding the logic array provides power to the I/O drivers, as shown in Figure 41. An independent matrix of Vcc and Ground lines supplies the interior logic of the device.

This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically, a 0.1 µF capacitor connected near the Vcc and Ground pins of the package will provide adequate decoupling.

Output buffers capable of driving/sinking the specified 12 mA (XC4000E) or 24 mA (XC4000EX) loads under specified worst-case conditions may be capable of driving/sinking up to 10 times as much current under best case conditions.

Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the Ground pads. The I/O Block output buffers have a slew-rate limited mode (default) which should be used where output rise and fall times are not speed-critical.

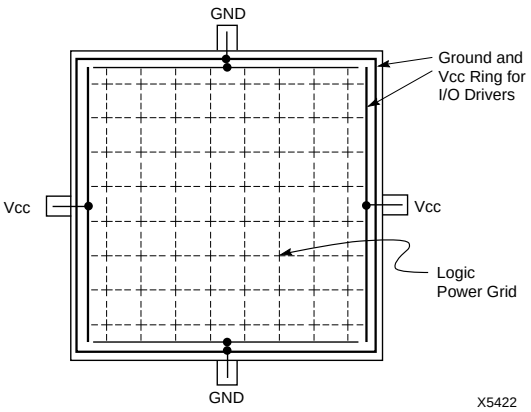


Figure 41: XC4000-Series Power Distribution

Pin Descriptions

There are three types of pins in the XC4000-Series devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with a 50 kΩ - 100 kΩ pull-up resistor.

After configuration, if an IOB is unused it is configured as an input with a 50 kΩ - 100 kΩ pull-up resistor.

XC4000-Series devices have no dedicated Reset input. Any user I/O can be configured to drive the Global Set/Reset net, GSR. See “Global Set/Reset” on page 13 for more information on GSR.

XC4000-Series devices have no Powerdown control input, as the XC3000 and XC2000 families do. The XC3000/XC2000 Powerdown control also 3-stated all of the device I/O pins. For XC4000-Series devices, use the global 3-state net, GTS, instead. This net 3-states all outputs, but does not place the device in low-power mode. See “IOB Output Signals” on page 27 for more information on GTS.

Device pins for XC4000-Series devices are described in Table 18. Pin functions during configuration for each of the seven configuration modes are summarized in Table 24 on page 78, in the “Configuration Timing” section.

Configuration Timing

The seven configuration modes are discussed in detail in this section. Timing specifications are included.

Master Serial Mode

In Master Serial mode, the CCLK output of the lead FPGA drives a Xilinx Serial PROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The lead FPGA accepts this data on the subsequent rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In MakeBits, the user can specify Fast ConfigRate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight. The value increases from between 0.5 and 1.25 MHz, to a value between 4 and 10 MHz. (For low-voltage devices, the frequency can be up to 10% lower.) Be sure that the serial PROM and slaves are fast enough to support this data rate. XC2000, XC3000/A, and XC3100A devices do not support the Fast ConfigRate option.

The SPROM CE input can be driven from either $\overline{LDC}$ or DONE. Using $\overline{LDC}$ avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but $\overline{LDC}$ is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the early DONE option is invoked.

Figure 53 shows a full master/slave system. The leftmost device is in Master Serial mode.

Master Serial mode is selected by a <000> on the mode pins (M2, M1, M0).

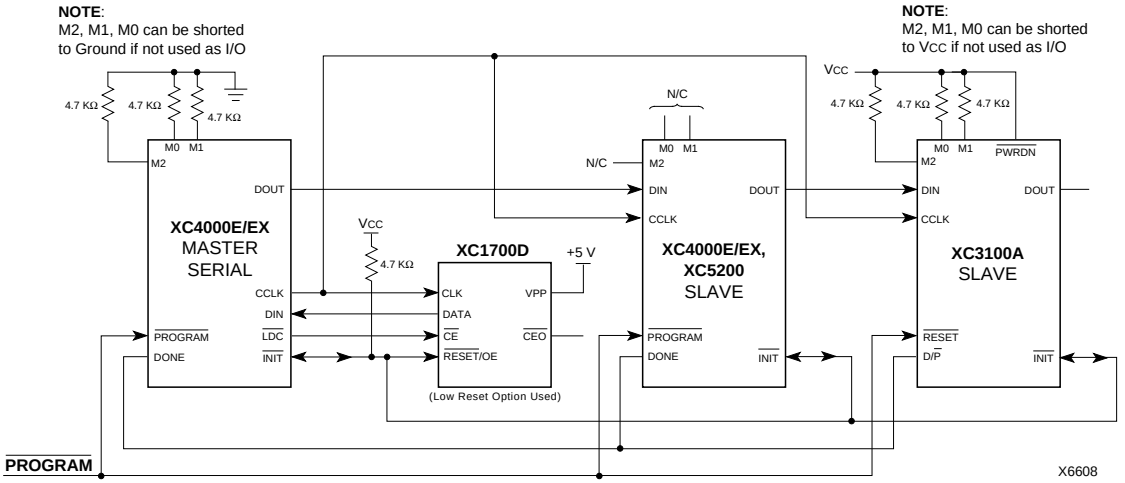


Figure 53: Master Serial Mode Circuit Diagram

Synchronous Peripheral Mode

Synchronous Peripheral mode can also be considered Slave Parallel mode. An external signal drives the CCLK input(s) of the FPGA(s). The first byte of parallel configuration data must be available at the Data inputs of the lead FPGA a short setup time before the rising CCLK edge. Subsequent data bytes are clocked in on every eighth consecutive rising CCLK edge.

The same CCLK edge that accepts data, also causes the RDY/$\overline{\text{BUSY}}$ output to go High for one CCLK period. The pin name is a misnomer. In Synchronous Peripheral mode it is really an ACKNOWLEDGE signal. Synchronous operation does not require this response, but it is a meaningful signal for test purposes. Note that RDY/$\overline{\text{BUSY}}$ is pulled High with a high-impedance pullup prior to $\overline{\text{INIT}}$ going High.

The lead FPGA serializes the data and presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In order to complete the serial shift operation, 10 additional CCLK rising edges are required after the last data byte has been loaded, plus one more CCLK cycle for each daisy-chained device.

Synchronous Peripheral mode is selected by a <011> on the mode pins (M2, M1, M0).

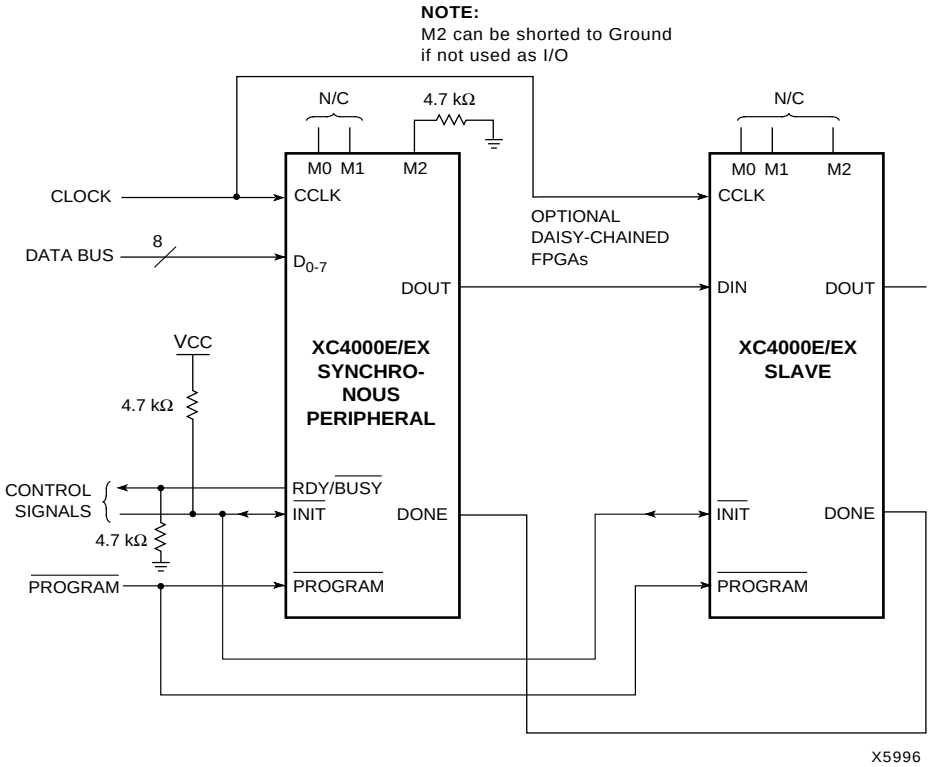
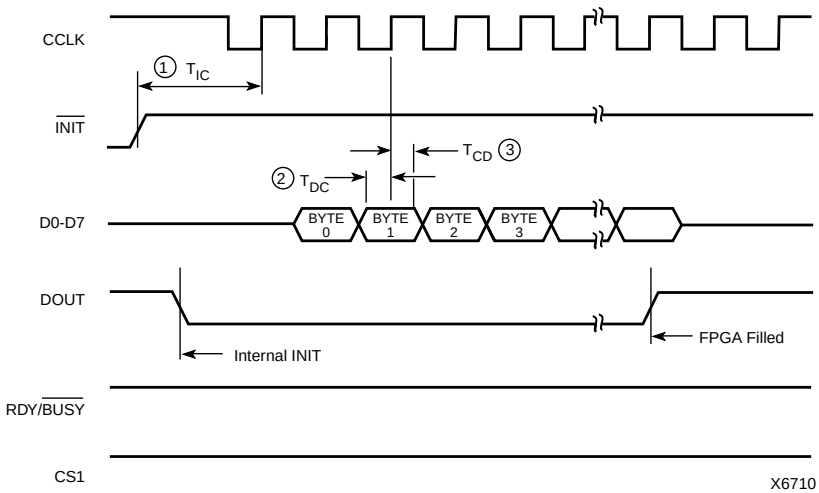


Figure 59: Synchronous Peripheral Mode Circuit Diagram

	Description	Symbol	Min	Max	Units
CCLK	$\overline{INIT}$ (High) setup time	T_{IC}	-		µs
	D0 - D7 setup time	T_{DC}	-		ns
	D0 - D7 hold time	T_{CD}	0		ns
	CCLK High time	T_{CCH}	-		ns
	CCLK Low time	T_{CCL}	-		ns
	CCLK Frequency	F_{CC}		-	MHz
			Preliminary		



Note: If not driven by the preceding DOUT, CS1 *must* remain High until the device is fully configured.

Figure 64: Express Mode Programming Switching Characteristics

XC4000E Absolute Maximum Ratings

Symbol	Description			Units
V_{CC}	Supply voltage relative to GND		-0.5 to +7.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

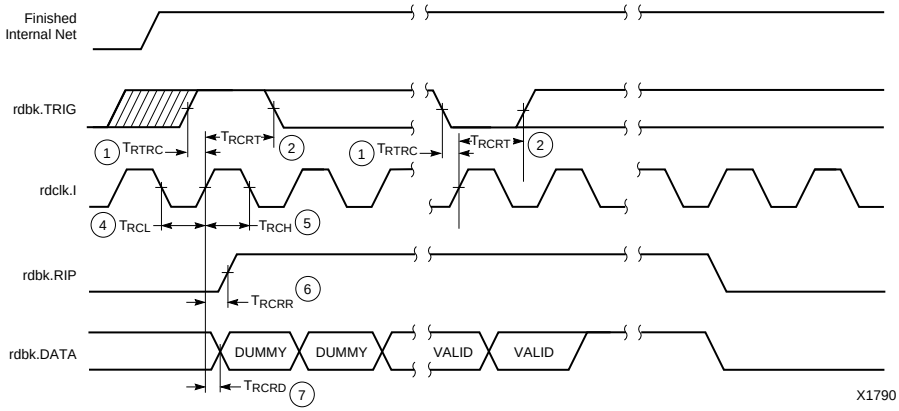
Note 1: Maximum DC overshoot or undershoot above Vcc or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to Vcc + 2.0 V, provided this over- or undershoot lasts less than 20 ns.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC4000E Program Readback Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements.

The following guidelines reflect worst-case values over the recommended operating conditions.



	Description	Symbol		Min	Max	Units
rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	1	T_{RTRC}	200	-	ns
	rdbk.TRIG hold to initiate and abort Readback	2	T_{RCRT}	50	-	ns
rdclk.1	rdbk.DATA delay	7	T_{RCRD}	-	250	ns
	rdbk.RIP delay	6	T_{RCRR}	-	250	ns
	High time	5	T_{RCH}	250	500	ns
	Low time	4	T_{RCL}	250	500	ns

Note 1: Timing parameters apply to all speed grades.

Note 2: If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

XC4000E Global Buffer Switching Characteristic Guidelines

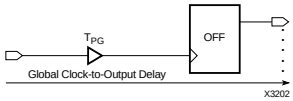
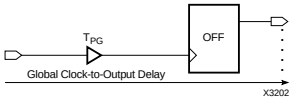
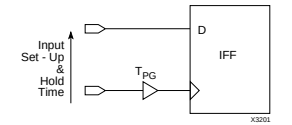
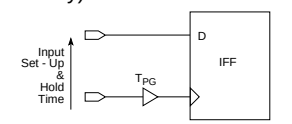
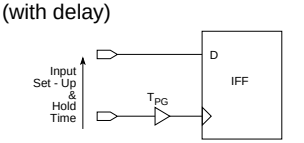
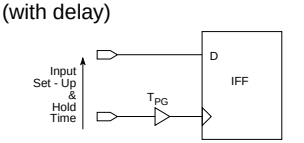
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	-3	-2		
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**		**Units**
From pad through Primary buffer, to any clock K	T_{PG}	XC4003E	7.0	4.7	4.0		ns
		XC4005E	7.0	4.7	4.3		ns
		XC4006E	7.5	5.3	5.2		ns
		XC4008E	8.0	6.1	5.2		ns
		XC4010E	11.0	6.3	5.4		ns
		XC4013E	11.5	6.8	5.8		ns
		XC4020E	12.0	7.0	6.4		ns
		XC4025E	12.5	7.2	6.9		ns
From pad through Secondary buffer, to any clock K	T_{SG}	XC4003E	7.5	5.2	4.4		ns
		XC4005E	7.5	5.2	4.7		ns
		XC4006E	8.0	5.8	5.6		ns
		XC4008E	8.5	6.6	5.6		ns
		XC4010E	11.5	6.8	5.8		ns
		XC4013E	12.0	7.3	6.2		ns
		XC4020E	12.5	7.5	6.7		ns
		XC4025E	13.0	7.7	7.2		ns
					Preliminary		

XC4000E Guaranteed Input and Output Parameters (Pin-to-Pin, TTL I/O)

All values listed below are tested directly, and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The XACT delay calculator uses this indirect method. When there is a discrepancy between the two methods, the values listed below should be used, and the derived values must be ignored. All values are expressed in units of nanoseconds.

		Speed Grade	-4	-3	-2
Description	**Symbol**	**Device**			
Global Clock to Output (fast) using OFF 	T_{ICKOF} (Max)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	12.5 14.0 14.5 15.0 16.0 16.5 17.0 17.0	10.2 10.7 10.7 10.8 10.9 11.0 11.0 12.6	8.7 9.1 9.1 9.2 9.3 9.4 10.2 10.8
Global Clock to Output (slew-limited) using OFF 	T_{ICKO} (Max)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	16.5 18.0 18.5 19.0 20.0 20.5 21.0 21.0	14.0 14.7 14.7 14.8 14.9 15.0 15.1 15.3	11.5 12.0 12.0 12.1 12.2 12.8 12.8 13.0
Input Setup Time, using IFF (no delay) 	T_{PSUF} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	2.5 2.0 1.9 1.4 1.0 0.5 0 0	2.3 1.2 1.0 0.6 0.2 0 0 0	2.3 1.2 1.0 0.6 0.2 0 0 0
Input Hold Time, using IFF (no delay) 	T_{PHF} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	4.0 4.6 5.0 6.0 6.0 7.0 7.5 8.0	4.0 4.5 4.7 5.1 5.5 6.5 6.7 7.0	4.0 4.5 4.7 5.1 5.5 5.5 5.7 5.9
Input Setup Time, using IFF (with delay) 	T_{PSU} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	8.5 8.5 8.5 8.5 8.5 8.5 9.5 9.5	7.0 7.0 7.0 7.0 7.0 7.0 7.0 7.6	6.0 6.0 6.0 6.0 6.0 6.0 6.8 6.8
Input Hold Time, using IFF (with delay) 	T_{PH} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

OFF = Output Flip-Flop IFF = Input Flip-Flop or Latch **Preliminary**

XC4020E Pad Name	HQ 208	PG 223	HQ 240	Bndry Scan
VCC	P55	D16	P61	-
I (M2)	P56	C16	P62	342
I/O, PGCK2	P57	B17	P63	343
I/O (HDC)	P58	E16	P64	346
I/O	P59	C17	P65	349
I/O	P60	D17	P66	352
I/O	P61	B18	P67	355
I/O ($\overline{\text{LDC}}$)	P62	E17	P68	358
I/O	-	-	-	361
I/O	-	-	-	364
I/O	P63	F16	P69	367
I/O	P64	C18	P70	370
I/O	P65	D18	P71	373
I/O	P66	F17	P72	376
I/O	-	E15	P73	379
I/O	-	F15	P74	382
GND	P67	G16	P75	-
I/O	P68	E18	P76	385
I/O	P69	F18	P77	388
I/O	P70	G17	P78	391
I/O	P71	G18	P79	394
VCC	-	-	P80	-
I/O	P72	H16	P81	397
I/O	P73	H17	P82	400
I/O	-	-	-	403
I/O	-	-	-	406
I/O	-	G15	P84	409
I/O	-	H15	P85	412
I/O	P74	H18	P86	415
I/O	P75	J18	P87	418
I/O	P76	J17	P88	421
I/O ($\overline{\text{INIT}}$)	P77	J16	P89	424
VCC	P78	J15	P90	-
GND	P79	K15	P91	-
I/O	P80	K16	P92	427
I/O	P81	K17	P93	430
I/O	P82	K18	P94	433
I/O	P83	L18	P95	436
I/O	P84	L17	P96	439
I/O	P85	L16	P97	442
I/O	-	-	-	445
I/O	-	-	-	448
I/O	-	L15	P99	451
I/O	-	M15	P100	454
VCC	-	-	P101	-
I/O	P86	M18	P102	457
I/O	P87	M17	P103	460
I/O	P88	N18	P104	463
I/O	P89	P18	P105	466
GND	P90	M16	P106	-
I/O	-	N15	P107	469
I/O	-	P15	P108	472

XC4020E Pad Name	HQ 208	PG 223	HQ 240	Bndry Scan
I/O	P91	N17	P109	475
I/O	P92	R18	P110	478
I/O	P93	T18	P111	481
I/O	P94	P17	P112	484
I/O	-	-	-	487
I/O	-	-	-	490
I/O	P95	N16	P113	493
I/O	P96	T17	P114	496
I/O	P97	R17	P115	499
I/O	P98	P16	P116	502
I/O	P99	U18	P117	505
I/O, SGCK3	P100	T16	P118	508
GND	P101	R16	P119	-
DONE	P103	U17	P120	-
VCC	P106	R15	P121	-
$\overline{\text{PROGRAM}}$	P108	V18	P122	-
I/O (D7)	P109	T15	P123	511
I/O, PGCK3	P110	U16	P124	514
I/O	P111	T14	P125	517
I/O	P112	U15	P126	520
I/O	-	R14	P127	523
I/O	-	R13	P128	526
I/O	-	-	-	529
I/O	-	-	-	532
I/O (D6)	P113	V17	P129	535
I/O	P114	V16	P130	538
I/O	P115	T13	P131	541
I/O	P116	U14	P132	544
I/O	P117	V15	P133	547
I/O	P118	V14	P134	550
GND	P119	T12	P135	-
I/O	-	R12	P136	553
I/O	-	R11	P137	556
I/O	P120	U13	P138	559
I/O	P121	V13	P139	562
VCC	-	-	P140	-
I/O (D5)	P122	U12	P141	565
I/O ($\overline{\text{CS0}}$)	P123	V12	P142	568
I/O	-	-	-	571
I/O	-	-	-	574
I/O	P124	T11	P144	577
I/O	P125	U11	P145	580
I/O	P126	V11	P146	583
I/O	P127	V10	P147	586
I/O (D4)	P128	U10	P148	589
I/O	P129	T10	P149	592
VCC	P130	R10	P150	-
GND	P131	R9	P151	-
I/O (D3)	P132	T9	P152	595
I/O ($\overline{\text{RS}}$)	P133	U9	P153	598
I/O	P134	V9	P154	601
I/O	P135	V8	P155	604

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
I/O	P33	B11	P41	A14	P252	U24	326
I/O	P34	A12	P42	C13	P251	V25	329
I/O	P35	B12	P43	B14	P250	V24	332
I/O, FCLK2	P36	A13	P44	D13	P249	U23	335
GND	P37	C12	P45	A15	P248	GND*	-
I/O	-	-	-	B15	P247	Y26	338
I/O	-	-	-	E13	P246	W25	341
I/O	-	D13	P46	C14	P245	W24	344
I/O	-	D14	P47	A17	P244	V23	347
I/O	P38	B13	P48	D14	P243	AA26	350
I/O	P39	A14	P49	B16	P242	Y25	353
I/O	P40	A15	P50	C15	P241	Y24	356
I/O	P41	C13	P51	E14	P240	AA25	359
GND	-	-	-	-	-	GND*	-
VCC	-	-	-	-	-	VCC*	-
I/O	-	-	-	A18	P239	AB25	362
I/O	-	-	-	D15	P238	AA24	365
I/O	P42	B14	P52	C16	P237	Y23	368
I/O	P43	A16	P53	B17	P236	AC26	371
I/O	P44	B15	P54	B18	P235	AA23	374
I/O	P45	C14	P55	E15	P234	AB24	377
I/O	P46	A17	P56	D16	P233	AD25	380
I/O, SGCK2, GCK2	P47	B16	P57	C17	P232	AC24	383
O (M1)	P48	C15	P58	A20	P231	AB23	386
GND	P49	D15	P59	A19	P230	GND*	-
I (M0)	P50	A18	P60	C18	P229	AD24	389
VCC	P55	D16	P61	B20	P228	VCC*	-
I (M2)	P56	C16	P62	D17	P227	AC23	390
I/O, PGCK2, GCK3	P57	B17	P63	B19	P226	AE24	391
I/O (HDC)	P58	E16	P64	C19	P225	AD23	394
I/O	P59	C17	P65	F16	P224	AC22	397
I/O	P60	D17	P66	E17	P223	AF24	400
I/O	P61	B18	P67	D18	P222	AD22	403
I/O ($\overline{\text{LDC}}$)	P62	E17	P68	C20	P221	AE23	406
I/O	-	-	-	F17	P220	AE22	409
I/O	-	-	-	G16	P219	AF23	412
VCC	-	-	-	-	-	VCC*	-
GND	-	-	-	-	-	GND*	-
I/O	P63	F16	P69	D19	P218	AD20	415
I/O	P64	C18	P70	E18	P217	AE21	418
I/O	P65	D18	P71	D20	P216	AF21	421
I/O	P66	F17	P72	G17	P215	AC19	424
I/O	-	E15	P73	F18	P214	AD19	427
I/O	-	F15	P74	H16	P213	AE20	430
I/O	-	-	-	E19	P212	AF20	433
I/O	-	-	-	F19	P211	AC18	436
GND	P67	G16	P75	E20	P210	GND*	-
I/O	P68	E18	P76	H17	P209	AD18	439
I/O	P69	F18	P77	G18	P208	AE19	442

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
I/O	P70	G17	P78	G19	P207	AC17	445
I/O	P71	G18	P79	H18	P206	AD17	448
VCC	-	-	P80	F20	P204	VCC*	-
I/O	P72	H16	P81	J16	P203	AE18	451
I/O	P73	H17	P82	G20	P202	AF18	454
I/O	-	-	-	J17	P201	AE17	457
I/O	-	-	-	H19	P200	AE16	460
GND‡	-	-	P83	-	-	GND*	-
I/O	-	-	-	H20	P199	AF16	463
I/O	-	-	-	J18	P198	AC15	466
I/O	-	G15	P84	J19	P197	AD15	469
I/O	-	H15	P85	K16	P196	AE15	472
I/O	P74	H18	P86	J20	P195	AF15	475
I/O	P75	J18	P87	K17	P194	AD14	478
I/O	P76	J17	P88	K18	P193	AE14	481
I/O ($\overline{\text{INIT}}$)	P77	J16	P89	K19	P192	AF14	484
VCC	P78	J15	P90	L20	P191	VCC*	-
GND	P79	K15	P91	K20	P190	GND*	-
I/O	P80	K16	P92	L19	P189	AE13	487
I/O	P81	K17	P93	L18	P188	AC13	490
I/O	P82	K18	P94	L16	P187	AD13	493
I/O	P83	L18	P95	L17	P186	AF12	496
I/O	P84	L17	P96	M20	P185	AE12	499
I/O	P85	L16	P97	M19	P184	AD12	502
I/O	-	-	-	N20	P183	AC12	505
I/O	-	-	-	M18	P182	AF11	508
GND‡	-	-	P98	-	-	GND*	-
I/O	-	-	-	M17	P181	AE11	511
I/O	-	-	-	M16	P180	AD11	514
I/O	-	L15	P99	N19	P179	AF9	517
I/O	-	M15	P100	P20	P178	AD10	520
VCC	-	-	P101	T20	P177	VCC*	-
I/O	P86	M18	P102	N18	P175	AE9	523
I/O	P87	M17	P103	P19	P174	AD9	526
I/O	P88	N18	P104	N17	P173	AC10	529
I/O	P89	P18	P105	R19	P172	AF7	532
GND	P90	M16	P106	R20	P171	GND*	-
I/O	-	-	-	N16	P170	AE8	535
I/O	-	-	-	P18	P169	AD8	538
I/O	-	N15	P107	U20	P168	AC9	541
I/O	-	P15	P108	P17	P167	AF6	544
I/O	P91	N17	P109	T19	P166	AE7	547
I/O	P92	R18	P110	R18	P165	AD7	550
I/O	P93	T18	P111	P16	P164	AE6	553
I/O	P94	P17	P112	V20	P163	AE5	556
GND	-	-	-	-	-	GND*	-
VCC	-	-	-	-	-	VCC*	-
I/O	-	-	-	R17	P162	AD6	559
I/O	-	-	-	T18	P161	AC7	562
I/O	P95	N16	P113	U19	P160	AF4	565
I/O	P96	T17	P114	V19	P159	AF3	568

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
I (M0)	P229	E35	AH28	437
VCC	P228	VCC*	VCC*	-
I (M2)	P227	G33	AJ28	438
I/O, GCK3	P226	D36	AK29	439
I/O (HDC)	P225	C37	AH27	442
I/O	P224	F34	AK28	445
I/O	P223	J33	AJ27	448
I/O	P222	D38	AL28	451
I/O ($\overline{\text{LDC}}$)	P221	G35	AH26	454
I/O	-	E39	AL27	457
I/O	-	K34	AH25	460
I/O	P220	F38	AK26	463
I/O	P219	G37	AL26	466
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O	P218	H38	AH24	469
I/O	P217	J37	AJ25	472
I/O	P216	G39	AK25	475
I/O	P215	M34	AJ24	478
I/O	P214	N35	AL24	481
I/O	P213	P34	AH22	484
I/O	P212	J35	AJ23	487
I/O	P211	L37	AK23	490
GND	P210	GND*	GND*	-
I/O	P209	M38	AJ22	493
I/O	P208	R35	AK22	496
I/O	P207	H36	AL22	499
I/O	P206	T34	AJ21	502
VCC	P204	VCC*	VCC*	-
I/O	P203	N37	AH20	505
I/O	P202	N39	AK21	508
I/O	-	U35	AK20	511
I/O	-	R39	AJ19	514
I/O	P201	M36	AL20	517
I/O	P200	V34	AH18	520
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O	P199	R37	AK19	523
I/O	P198	T38	AJ18	526
I/O	P197	T36	AL19	529
I/O	P196	V36	AK18	532
I/O	P195	U37	AH17	535
I/O	P194	U39	AJ17	538
I/O	P193	V38	AJ16	541
I/O ($\overline{\text{INIT}}$)	P192	W37	AK16	544
VCC	P191	VCC*	VCC*	-
GND	P190	GND*	GND*	-

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
I/O	P189	Y34	AL16	547
I/O	P188	AC37	AH15	550
I/O	P187	AB38	AK15	553
I/O	P186	AD36	AJ14	556
I/O	P185	AA35	AH14	559
I/O	P184	AE37	AK14	562
I/O	P183	AB36	AL13	565
I/O	P182	AD38	AK13	568
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O	P181	AB34	AJ13	571
I/O	P180	AE39	AH13	574
I/O	-	AM36	AL12	577
I/O	-	AC35	AK12	580
I/O	P179	AG39	AH12	583
I/O	P178	AG37	AJ11	586
VCC	P177	VCC*	VCC*	-
I/O	P175	AD34	AL10	589
I/O	P174	AN39	AK10	592
I/O	P173	AE35	AJ10	595
I/O	P172	AH38	AK9	598
GND	P171	GND*	GND*	-
I/O	P170	AJ37	AL8	601
I/O	P169	AG35	AH10	604
I/O	P168	AF34	AJ9	607
I/O	P167	AH36	AK8	610
I/O	P166	AK36	AK7	613
I/O	P165	AM34	AL6	616
I/O	P164	AH34	AJ7	619
I/O	P163	AJ35	AH8	622
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O	P162	AL37	AK6	625
I/O	P161	AT38	AL5	628
I/O	P160	AM38	AH7	631
I/O	P159	AN37	AJ6	634
I/O	-	AK34	AK5	637
I/O	-	AR39	AL4	640
I/O	P158	AN35	AK4	643
I/O	P157	AL33	AH5	646
I/O	P156	AV38	AK3	649
I/O, GCK4	P155	AT36	AJ4	652
GND	P154	GND*	GND*	-
DONE	P153	AR35	AH4	-
VCC	P152	VCC*	VCC*	-
$\overline{\text{PROGRAM}}$	P151	AN33	AH3	-
I/O (D7)	P150	AM32	AJ2	655

PQ100 Package Pinouts

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

PQ100 Pin	XC4003E	XC4005E
P1	I/O (A14)	I/O (A14)
P2	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
P3	VCC	VCC
P4	GND	GND
P5	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
P6	I/O (A17)	I/O (A17)
P7	I/O, TDI	I/O, TDI
P8	I/O, TCK	I/O, TCK
P9	I/O, TMS	I/O, TMS
P10	I/O	I/O
P11	I/O	I/O
P12	I/O	I/O
P13	I/O	I/O
P14	GND	GND
P15	VCC	VCC
P16	I/O	I/O
P17	I/O	I/O
P18	I/O	I/O
P19	I/O	I/O
P20	I/O	I/O
P21	I/O	I/O
P22	I/O	I/O
P23	I/O	I/O
P24	I/O, SCGK2	I/O, SCGK2
P25	O (M1)	O (M1)
P26	GND	GND
P27	I (M0)	I (M0)
P28	VCC	VCC
P29	I (M2)	I (M2)
P30	I/O, PGCK2	I/O, PGCK2
P31	I/O (HDC)	I/O (HDC)
P32	I/O	I/O
P33	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
P34	I/O	I/O
P35	I/O	I/O
P36	I/O	I/O
P37	I/O	I/O
P38	I/O	I/O
P39	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
P40	VCC	VCC
P41	GND	GND
P42	I/O	I/O
P43	I/O	I/O
P44	I/O	I/O
P45	I/O	I/O
P46	I/O	I/O
P47	I/O	I/O
P48	I/O	I/O
P49	I/O	I/O
P50	I/O	I/O
P51	I/O, SGCK3	I/O, SGCK3
P52	GND	GND
P53	DONE	DONE
P54	VCC	VCC
P55	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
P56	I/O (D7)	I/O (D7)
P57	I/O, PGCK3	I/O, PGCK3
P58	I/O (D6)	I/O (D6)
P59	I/O	I/O
P60	I/O (D5)	I/O (D5)
P61	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)
P62	I/O	I/O
P63	I/O	I/O
P64	I/O (D4)	I/O (D4)
P65	I/O	I/O
P66	VCC	VCC
P67	GND	GND
P68	I/O (D3)	I/O (D3)
P69	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)
P70	I/O	I/O
P71	I/O (D2)	I/O (D2)
P72	I/O	I/O
P73	I/O (D1)	I/O (D1)
P74	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)
P75	I/O (D0, DIN)	I/O (D0, DIN)
P76	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
P77	CCLK	CCLK
P78	VCC	VCC
P79	O, TDO	O, TDO
P80	GND	GND
P81	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)
P82	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
P83	I/O (CS1, A2)	I/O (CS1, A2)
P84	I/O (A3)	I/O (A3)
P85	I/O (A4)	I/O (A4)
P86	I/O (A5)	I/O (A5)
P87	I/O	I/O
P88	I/O	I/O
P89	I/O (A6)	I/O (A6)
P90	I/O (A7)	I/O (A7)
P91	GND	GND
P92	VCC	VCC
P93	I/O (A8)	I/O (A8)
P94	I/O (A9)	I/O (A9)
P95	I/O	I/O
P96	I/O	I/O
P97	I/O (A10)	I/O (A10)
P98	I/O (A11)	I/O (A11)
P99	I/O (A12)	I/O (A12)
P100	I/O (A13)	I/O (A13)

2/28/96

PQ 208 Pin	XC 4005 E/L	XC 4006 E	XC 4008 E	XC 4010 E/L	XC 4013 E/L	XC 4020 E	XC 4028 EX/XL
P88	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P89	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P90	GND	GND	GND	GND	GND	GND	GND
P91	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P92	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P93	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P94	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P95	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P96	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P97	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P98	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P99	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P100	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, GCK4
P101	GND	GND	GND	GND	GND	GND	GND
P102	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P103	DONE	DONE	DONE	DONE	DONE	DONE	DONE
P104	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P105	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P106	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P107	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P108	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
P109	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)
P110	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, GCK5
P111	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P112	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P113	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)
P114	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P115	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P116	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P117	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P118	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P119	GND	GND	GND	GND	GND	GND	GND
P120	I/O	I/O	I/O	I/O	I/O	I/O	I/O, FCLK3
P121	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P122	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)
P123	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)
P124	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P125	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P126	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P127	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P128	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)
P129	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P130	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P131	GND	GND	GND	GND	GND	GND	GND
P132	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
P133	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)

PQ 208 Pin	XC 4005 E/L	XC 4006 E	XC 4008 E	XC 4010 E/L	XC 4013 E/L	XC 4020 E	XC 4028 EX/XL
P134	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P135	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P136	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P137	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P138	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)
P139	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P140	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P141	I/O	I/O	I/O	I/O	I/O	I/O	I/O, FCLK4
P142	GND	GND	GND	GND	GND	GND	GND
P143	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P144	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P145	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P146	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P147	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)
P148	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)
P149	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P150	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P151	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)
P152	I/O, SGCK (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, GCK6 (DOUT)
P153	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK
P154	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P155	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P156	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P157	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P158	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P159	O, TDO	O, TDO	O, TDO	O, TDO	O, TDO	O, TDO	O, TDO
P160	GND	GND	GND	GND	GND	GND	GND
P161	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)
P162	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, GCK7 (A1)
P163	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P164	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P165	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)
P166	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)
P167	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P168	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P169	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P170	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P171	GND	GND	GND	GND	GND	GND	GND
P172	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P173	I/O	I/O	I/O	I/O	I/O	I/O	I/O

PQ240/ HQ240 Pin	XC4013E XC4013L	XC4020E	XC4025E	XC4028EX XC4028XL
P86	I/O	I/O	I/O	I/O
P87	I/O	I/O	I/O	I/O
P88	I/O	I/O	I/O	I/O
P89	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
P90	VCC	VCC	VCC	VCC
P91	GND	GND	GND	GND
P92	I/O	I/O	I/O	I/O
P93	I/O	I/O	I/O	I/O
P94	I/O	I/O	I/O	I/O
P95	I/O	I/O	I/O	I/O
P96	I/O	I/O	I/O	I/O
P97	I/O	I/O	I/O	I/O
P98	N.C.‡	N.C.‡	N.C.‡	GND‡
P99	I/O	I/O	I/O	I/O
P100	I/O	I/O	I/O	I/O
P101	VCC	VCC	VCC	VCC
P102	I/O	I/O	I/O	I/O
P103	I/O	I/O	I/O	I/O
P104	I/O	I/O	I/O	I/O
P105	I/O	I/O	I/O	I/O
P106	GND	GND	GND	GND
P107	I/O	I/O	I/O	I/O
P108	I/O	I/O	I/O	I/O
P109	I/O	I/O	I/O	I/O
P110	I/O	I/O	I/O	I/O
P111	I/O	I/O	I/O	I/O
P112	I/O	I/O	I/O	I/O
P113	I/O	I/O	I/O	I/O
P114	I/O	I/O	I/O	I/O
P115	I/O	I/O	I/O	I/O
P116	I/O	I/O	I/O	I/O
P117	I/O	I/O	I/O	I/O
P118	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, GCK4
P119	GND	GND	GND	GND
P120	DONE	DONE	DONE	DONE
P121	VCC	VCC	VCC	VCC
P122	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$	$\overline{\text{PRO-GRAM}}$
P123	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)
P124	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, GCK5
P125	I/O	I/O	I/O	I/O
P126	I/O	I/O	I/O	I/O
P127	I/O	I/O	I/O	I/O
P128	I/O	I/O	I/O	I/O
P129	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)

PQ240/ HQ240 Pin	XC4013E XC4013L	XC4020E	XC4025E	XC4028EX XC4028XL
P130	I/O	I/O	I/O	I/O
P131	I/O	I/O	I/O	I/O
P132	I/O	I/O	I/O	I/O
P133	I/O	I/O	I/O	I/O
P134	I/O	I/O	I/O	I/O
P135	GND	GND	GND	GND
P136	I/O	I/O	I/O	I/O
P137	I/O	I/O	I/O	I/O
P138	I/O	I/O	I/O	I/O, FCLK3
P139	I/O	I/O	I/O	I/O
P140	VCC	VCC	VCC	VCC
P141	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)
P142	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)
P143	N.C.‡	N.C.‡	N.C.‡	GND‡
P144	I/O	I/O	I/O	I/O
P145	I/O	I/O	I/O	I/O
P146	I/O	I/O	I/O	I/O
P147	I/O	I/O	I/O	I/O
P148	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)
P149	I/O	I/O	I/O	I/O
P150	VCC	VCC	VCC	VCC
P151	GND	GND	GND	GND
P152	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
P153	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)
P154	I/O	I/O	I/O	I/O
P155	I/O	I/O	I/O	I/O
P156	I/O	I/O	I/O	I/O
P157	I/O	I/O	I/O	I/O
P158	N.C.‡	N.C.‡	N.C.‡	GND‡
P159	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)
P160	I/O	I/O	I/O	I/O
P161	VCC	VCC	VCC	VCC
P162	I/O	I/O	I/O	I/O
P163	I/O	I/O	I/O	I/O, FCLK4
P164	I/O	I/O	I/O	I/O
P165	I/O	I/O	I/O	I/O
P166	GND	GND	GND	GND
P167	I/O	I/O	I/O	I/O
P168	I/O	I/O	I/O	I/O
P169	I/O	I/O	I/O	I/O
P170	I/O	I/O	I/O	I/O
P171	I/O	I/O	I/O	I/O
P172	I/O	I/O	I/O	I/O
P173	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)

PG411 Pin	XC4036EX/XL	XC4044EX/XL	XC4052XL
Y38	N.C.	I/O	I/O
W1	VCC	VCC	VCC
W3	I/O (A8)	I/O (A8)	I/O (A8)
W5	N.C.	I/O	I/O
W35	N.C.	I/O	I/O
W37	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)
W39	GND	GND	GND
V2	N.C.	I/O	I/O
V4	I/O (A19)	I/O (A19)	I/O (A19)
V6	I/O	I/O	I/O
V34	I/O	I/O	I/O
V36	I/O	I/O	I/O
V38	I/O	I/O	I/O
U1	I/O	I/O	I/O
U3	I/O (A10)	I/O (A10)	I/O (A10)
U5	I/O	I/O	I/O
U35	I/O	I/O	I/O
U37	I/O	I/O	I/O
U39	I/O	I/O	I/O
T2	I/O (A18)	I/O (A18)	I/O (A18)
T4	I/O	I/O	I/O
T6	I/O	I/O	I/O
T34	I/O	I/O	I/O
T36	I/O	I/O	I/O
T38	I/O	I/O	I/O
R1	I/O (A11)	I/O (A11)	I/O (A11)
R3	N.C.	N.C.	I/O
R5	I/O	I/O	I/O
R35	I/O	I/O	I/O
R37	I/O	I/O	I/O
R39	I/O	I/O	I/O
P2	I/O	I/O	I/O
P4	GND	GND	GND
P6	I/O	I/O	I/O
P34	I/O	I/O	I/O
P36	GND	GND	GND
P38	N.C.	N.C.	I/O
N1	I/O	I/O	I/O
N3	N.C.	N.C.	I/O
N5	I/O	I/O	I/O
N35	I/O	I/O	I/O
N37	I/O	I/O	I/O
N39	I/O	I/O	I/O
M2	I/O	I/O	I/O
M4	I/O	I/O	I/O
M6	I/O	I/O	I/O
M34	I/O	I/O	I/O
M36	I/O	I/O	I/O
M38	I/O	I/O	I/O
L1	GND	GND	GND
L3	I/O	I/O	I/O
L5	N.C.	I/O	I/O
L35	N.C.	N.C.	I/O
L37	I/O	I/O	I/O

PG411 Pin	XC4036EX/XL	XC4044EX/XL	XC4052XL
L39	VCC	VCC	VCC
K2	I/O	I/O	I/O
K4	I/O	I/O	I/O
K6	I/O	I/O	I/O
K34	I/O	I/O	I/O
K36	N.C.	I/O	I/O
K38	N.C.	I/O	I/O
J1	VCC	VCC	VCC
J3	I/O	I/O	I/O
J5	N.C.	I/O	I/O
J7	I/O	I/O	I/O
J33	I/O	I/O	I/O
J35	I/O	I/O	I/O
J37	I/O	I/O	I/O
J39	GND	GND	GND
H2	I/O	I/O	I/O
H4	I/O (A12)	I/O (A12)	I/O (A12)
H6	I/O	I/O	I/O
H8	I/O, GCK1 (A16)	I/O, GCK1 (A16)	I/O, GCK1 (A16)
H32	I/O	I/O	I/O
H34	N.C.	N.C.	I/O
H36	I/O	I/O	I/O
H38	I/O	I/O	I/O
G1	I/O	I/O	I/O
G3	I/O (A13)	I/O (A13)	I/O (A13)
G5	N.C.	N.C.	I/O
G7	I/O, GCK8 (A15)	I/O, GCK8 (A15)	I/O, GCK8 (A15)
G9	I/O, TCK	I/O, TCK	I/O, TCK
G31	I/O	I/O	I/O
G33	I (M2)	I (M2)	I (M2)
G35	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)
G37	I/O	I/O	I/O
G39	I/O	I/O	I/O
F2	N.C.	N.C.	I/O
F4	GND	GND	GND
F6	I/O (A17)	i/O (A17)	i/O (A17)
F8	I/O	I/O	I/O
F10	I/O	I/O	I/O
F12	I/O	I/O	I/O
F14	I/O	I/O	I/O
F16	I/O	I/O	I/O
F18	N.C.	I/O	I/O
F20	I/O	I/O	I/O
F22	N.C.	I/O	I/O
F24	I/O	I/O	I/O
F26	I/O	I/O	I/O
F28	I/O	I/O	I/O
F30	I/O	I/O	I/O
F32	I/O	I/O	I/O
F34	I/O	I/O	I/O
F36	VCC	VCC	VCC
F38	I/O	I/O	I/O
E1	I/O	I/O	I/O
E3	I/O	I/O	I/O